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Research Article

Signal Integrity Analysis in Carbon Nanotube Based Through-Silicon Via

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Development of a reliable 3D integrated system is largely dependent on the choice of filler materials used in through-silicon vias (TSVs). This research paper presents carbon nanotube (CNT) bundles as prospective filler materials for TSVs and provides an analysis of signal integrity for different single- (SWCNT), double- (DWCNT), and multi-walled CNT (MWCNT) bundle based TSVs. Depending on the physical configuration of a pair of TSVs, an equivalent electrical model is employed to analyze the in-phase and out-phase delays. It is observed that, using an MWCNT bundle (with number of shells = 10), the overall in-phase delays are reduced by 96.86%, 92.33%, 78.35%, and 32.72% compared to the bundled SWCNT, DWCNT, 4-shell MWCNT, and 8-shell MWCNT, respectively; similarly, the overall reduction in out-phase delay is 85.89%, 73.38%, 45.92%, and 12.56%, respectively.

1. Introduction

During recent past, several researchers [1] have designed the stacked IC layers on top of each other in order to integrate more devices on a single chip with improved performance. This advocated technique, known as 3D die stacking, primarily results in higher transistor density, improved speed, lower power dissipation and area [2]. Traditionally, the connections were made through the multiple IP (intellectual property) cores on a single die (System-on-Chip), multiple dies in a single package (Multi-Chip Package), and multiple ICs on a printed circuit board (PCB) [3]. Later on, system-in-package (SiP) technology is introduced where dies containing ICs are stacked vertically on a substrate. Another stacking technique is package-on-package (PoP) that uses vertically stacked multiple packaged chips [4]. The latest development in this area is the 3D stacked IC using through silicon vias (TSVs) that employs a single package containing vertical stack of naked dies and allows the die to be vertically interconnected with another die. TSVs are primarily referred as a vertical electrical connection "VIA" (vertical interconnect access) that passes completely through a silicon wafer or a die. A TSV based 3D IC offers various advantages in integrating a heterogeneous system onto a single platform as shown in Figure 1.

Copper (Cu), tungsten (W), polysilicon, gold (Au) and polymers are the most commonly used conductive filler materials for TSVs [5]. Cu is preferred due to its economical feasibility and technical superiority, but it faces certain challenges that arise due to fabrication limitations in achieving proper physical vapor deposition (PVD), seed layer deposition for ECD (electrochemical deposition), and performance limitations such as electromigration and higher resistivity. Therefore, researchers have targeted to find some alternative solutions that can potentially replace the Cu TSVs. Carbon nanotubes (CNTs) have emerged as an interesting choice of filler material. Improved thermal stability and negligible electromigration are the added advantages of CNT based TSVs. Thus, compared to Cu TSVs, an impressive result can be obtained for CNT based TSVs [5].

CNTs, known as the allotropes of carbon [6], have an extremely high length-to-diameter ratio up to 132,000,000 : 1. CNTs are considered as hollow cylindrical structures that are made of concentrically rolled up graphene sheets at specific

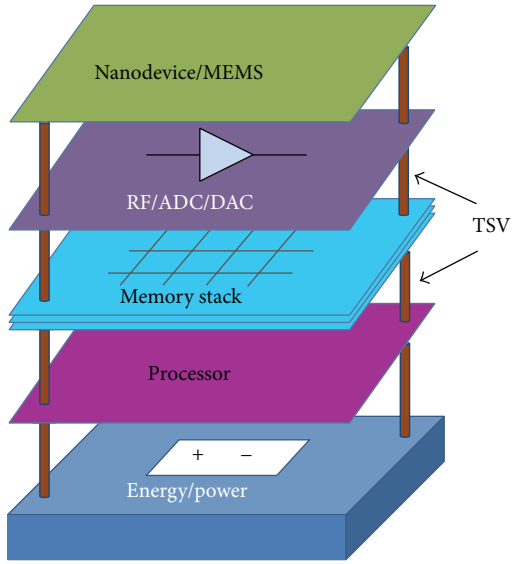

FIGURE 1: TSV based 3D technology.

and discrete angles. Depending on the rolled up direction (chirality) and the chiral angle, CNTs can exhibit unique electrical, thermal, mechanical, and chemical properties. The sp^2 bonding in graphene between carbon molecules is stronger than sp^3 bonds in diamond that makes CNTs the strongest and stiffest material in terms of tensile strength and elastic modulus, respectively [7]. The higher current carrying capability [8, 9], long ballistic transport length [8], higher thermal conductivity [10], and mechanical strength [11] are responsible for their exciting prospects in the areas of microelectronics/nanoelectronics [12], spintronics [13], optics [14], material science [15], mechanical [16], and biological fields [16, 17]. Moreover, CNTs can demonstrate a lot of research interest for their applications as energy storage devices, composite materials, field emitting devices, and chemical sensors [12–17]. Depending on the concentrically rolled up graphene sheets, CNTs are classified as single-walled CNTs (SWCNTs) and multi-walled CNTs (MWCNTs). SWCNTs consist of only one rolled up graphene sheet, whereas MWCNTs consist of two or more concentrically rolled up graphene sheets [18]. Double-walled CNT (DWCNT) is a special type of MWCNT wherein only two concentrically rolled up graphene sheets are present. Depending upon their different structures and chirality, CNTs can exhibit either metallic or semiconducting properties. Statistically, a natural mix of CNTs will have 1/3rd of metallic and 2/3rd of semiconducting chirality [8].

The research paper presents an equivalent electrical model that primarily integrates either SWCNT or MWCNT bundled TSVs on Si substrate. The equivalent model takes into account the conductive and capacitive behaviour of the Si substrate [5]. In this model, the capacitive effect of SiO_2 (insulating layer) is also considered and the interconnect line is represented by the electrical equivalent model of SWCNT, DWCNT, and MWCNT bundles. Using the capacitively coupled TSVs, crosstalk delay (signal integrity) is analyzed for in-phase and out-of-phase switching scenarios. The organization of this paper is as follows: Section 1 introduces the recent research scenario and briefs about the works carried out. Section 2 provides a detailed description of the physical configuration and an equivalent electrical model of a pair of CNT bundle based TSVs. Using the equivalent electrical model of different CNT bundled TSVs, Section 3 analyzes the signal integrity at different TSV heights. Finally, Section 4 draws a brief summary of the paper.

2. Physical Configuration and Equivalent *RLC* Model

The stacking of TSVs on Si substrate primarily uses a SWCNT/MWCNT bundle as prospective filler material. A thin layer of silicon dioxide (SiO_2) is the most commonly used dielectric material for TSVs. However, for high frequency applications, SiO_2 cannot be used due to its large fringing capacitance [19]. Hence, this layer needs to be replaced with a suitable polymer liner. The capacitance of TSVs with polymer liners reduces due to its lower dielectric constants and larger thickness than SiO_2 liners. It results in an improved electrical performance in terms of higher speed, reduced power dissipation, and crosstalk [20, 21].

The physical configuration of a pair of CNT bundle based TSV is shown in Figure 2. The number of CNTs (N_{CNT}) is approximated using the cross-sectional area of the via and the diameter of each CNT in a bundle. For a given via radius $r_{TSV} = 45$ nm, the cross-sectional area of the TSV is equal to 6361.73 nm^2. Therefore, the total numbers of SWCNTs, DWCNTs, and 4-, 8-, and 10-shell MWCNTs in a bundle are obtained as 8100, 2869, 876, 244, and 159, respectively, for a fixed SWCNT and DWCNT/MWCNT inner shell diameter (d_{CNT}) = 1 nm.

2.1. Equivalent Electrical Model of a Pair of CNT Bundle Based TSVs. Depending on the physical configuration of Figure 2, an equivalent electrical model of a pair of CNT bundle based TSV is shown in Figure 3 [5]. Between each TSV and the silicon substrate, SiO_2 is used as dielectric layer. The equivalent model takes into account per unit length (*p.u.l.*) scattering resistance (R'_{Bundle}), inductance (L'_{Bundle}), quantum ($C_Q^{'Bundle}$), and electrostatic capacitances ($C_E^{'Bundle}$). C_{TSV_OX} and C_{OX} represent the oxide capacitance around the via and between the TSVs, respectively. The capacitances C_{TSV_OX} and C_{OX} primarily depend on the thickness of SiO_2 layer (t_{ox}) and can be expressed as

$$C_{TSV\_OX} = \frac{4\varepsilon_0\varepsilon_r t_{si}\left(r_{TSV} - t_{ox}\right)}{t_{ox}}, \quad \text{where } t_{si} = H_{TSV},$$
$$C_{OX} = \left(\frac{2}{C_{TSV\_OX}} + \left(\frac{\varepsilon_0\varepsilon_r A}{d_{pitch}}\right)^{-1}\right)^{-1}, \quad (1)$$
$$\text{where } A = \pi r_{TSV} H_{TSV},$$

where H_{TSV}, d_{pitch}, ε_0, and ε_r represent the via height, distance between two TSVs, permittivity of vacuum, and SiO_2, respectively. The capacitance and conductance of Si substrate are represented as C_{SUB} and G_{SUB}, respectively. They

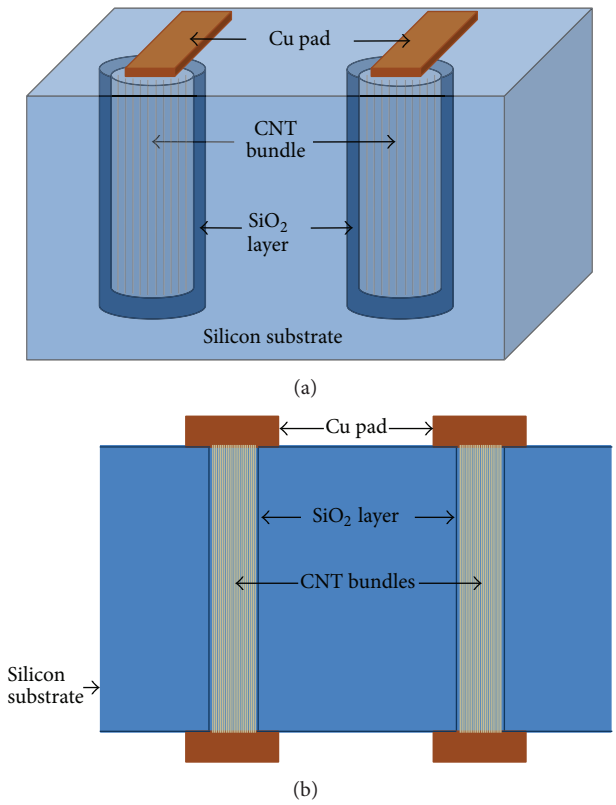

FIGURE 2: (a) Schematic and (b) physical configuration of a pair of CNT bundle based TSVs.

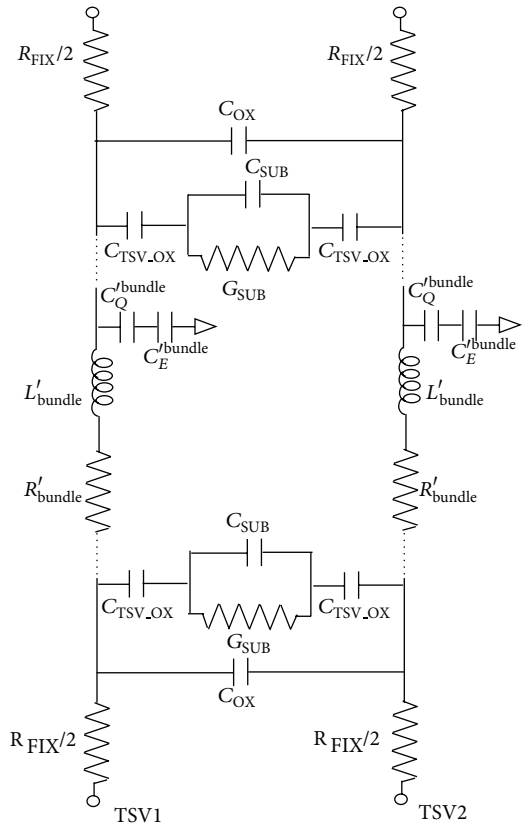

FIGURE 3: Equivalent electrical model of a pair of CNT bundle based TSVs.

primarily depend on the via area and d_{pitch} [5] and can be expressed as

$$C_{SUB} = \frac{\varepsilon_0 \varepsilon_r A}{d_{pitch}},$$

$$G_{SUB} = \frac{\pi\sigma}{\ln\left(\left(d_{pitch}/2r_{TSV}\right) + \left(\sqrt{\left(d_{pitch}/2r_{TSV}\right)^2 - 1}\right)\right)}, \quad (2)$$

where $\sigma = 0.1\,(\Omega.\text{cm})^{-1}$ represents the conductivity of the silicon substrate.

2.2. Equivalent RLC Model of CNT Bundle. The modeling of via parasitic is primarily dependent on the number of conducting channels associated with each CNT in a bundle. Naeemi and Meindl [22] modeled the conducting channels of MWCNTs as a function of shell diameter. Assuming one-third shells (or CNTs) as metallic, the average number of conducting channels for a particular shell (or diameter) can be expressed as [22]

$$N_i\left(D_i\right) \approx \begin{cases} k_1 T D_i + k_2, & D_i > \dfrac{d_T}{T} \\ \dfrac{2}{3}, & D_i \le \dfrac{d_T}{T}, \end{cases} \quad (3)$$

where D_i represents the diameter of the ith shell in MWCNT (or SWCNT) and constants k_1 and k_2 have a value of $3.87 \times 10^{-4}\,\text{nm}^{-1}\,\text{K}^{-1}$ and 0.2, respectively. The thermal energy of electrons and gap between two sub-bands determine the quantitative value of d_T that is equivalent to 1300 nm·K at room temperature ($T = 300$ K) [22]. For $D_i > 4.3$ nm, the average number of conducting channels is proportional to its shell diameter. Thus, the total number of conducting channels in a CNT is obtained using the summation of conducting channels (N_i) of each shell as

$$N_{channel} = \sum_{i=1}^{n} N_i. \quad (4)$$

The conduction mechanism in CNT is ballistic or dissipative due to the long mean free path (*mfp*) in the range of micrometers. The diameter dependent *mfp* can be expressed as

$$\lambda_{mfp,i} = \frac{1000 D_i}{\left(T/T_i\right) - 2}. \quad (5)$$

Thus, the total number of conducting channels in a bundle can be expressed as

$$N_{total} = N_{channel} \times N_{CNT}. \quad (6)$$

Table 1: Via parasitics associated with different CNT bundled TSVs.

Via parasitics	SWCNT bundle	DWCNT bundle	MWCNT bundle		
			Shell = 4	Shell = 8	Shell = 10
N_{total}	5400	3825	2336	1352	1148
R_{FIX} (kΩ)	3.2024	3.2013	3.2007	3.2004	3.2003
R'_{Bundle} (Ω/μm)	1.19	1.25	1.36	1.37	1.38
L'_{Bundle} (pH/μm)	2.99	4.23	6.93	11.97	14.09
$C_Q^{'Bundle}$ (fF/μm)	521.53	369.45	225.61	130.58	110.89
$C_E^{'Bundle}$ (fF/μm)	76.48	29.69	10.17	3.26	2.23
C'_{CM} (fF/μm)	7.71	5.07	3.17	1.93	1.64

Table 2: Percentage reduction of in-phase delay for 10-shell MWCNT bundled TSV w.r.t. SWCNT, DWCNT, and 4-shell and 8-shell MWCNT bundle based TSVs.

TSV heights (μm)	% reduction in delay for MWCNT bundle (shell = 10) in comparison to			
	SWB	DWB	MWB (shell = 4)	MWB (shell = 8)
50	96.62	91.82	77.08	30.26
100	96.71	92.02	77.53	31.02
150	96.79	92.20	77.85	31.52
200	97.32	93.27	80.92	38.07

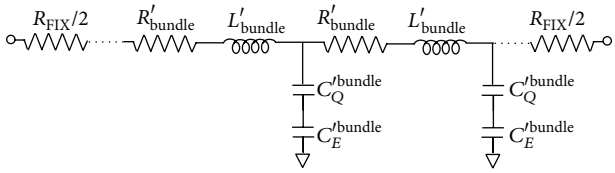

Figure 4: Equivalent *RLC* model of CNT bundle.

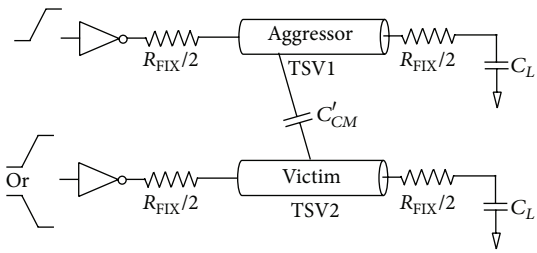

Figure 5: Capacitively coupled via lines.

The equivalent *RLC* model of CNT bundle is shown in Figure 4. Each CNT in a bundle primarily consists of three different types of resistances: (1) quantum or intrinsic resistance (R_q) that is due to the quantum confinement of electrons in a nanowire [23], (2) imperfect metal-nanotube contact resistance (R_c) that has a typical value of 3.2 kΩ depending on the fabrication process [24], and (3) scattering resistance (R') that occurs due to the higher nanotube length exceeding *mfps* of electrons. Therefore, the equivalent intrinsic and the scattering resistance of the ESC can be expressed as [22, 25]

$$R_{FIX} = \frac{R_q}{N_{total}} + R_c, \quad \text{where } R_q = \frac{h}{2e^2} \approx 12.9\,\text{k}\Omega,$$
$$R'_{Bundle} = \frac{\left(\sum_{i=1}^{n}\left(R_q/2N_i\lambda_{mfp,i}\right)^{-1}\right)^{-1}}{N_{CNT}}, \tag{7}$$

where h, n, and e represent Planck's constant, number of CNTs in a bundle, and charge of an electron, respectively.

The equivalent *RLC* model of CNT bundle primarily comprises two different types of capacitances: (1) quantum capacitance ($C_Q^{'Bundle}$) that represents the finite density of states at Fermi energy and (2) electrostatic capacitance ($C_E^{'Bundle}$) that is due to the potential difference between the CNT bundle and the ground plane. Thus, the $C_Q^{'Bundle}$ and $C_E^{'Bundle}$ can be expressed as

$$C_Q^{'Bundle} = C'_Q \times 2N_{total}, \quad \text{where } C'_Q = \frac{2e^2}{h\nu_F}, \tag{8}$$

$$C_E^{'Bundle} = \frac{2\pi\varepsilon_0\varepsilon_r}{\cosh^{-1}\left[\left(d_{CNT}^{Outer} + H_{TSV}\right)/d_{CNT}^{Outer}\right]}, \tag{9}$$

where ν_F and d_{CNT}^{Outer} represent the Fermi velocity ($\approx 8 \times 10^5$ m/s) and the diameter of the outer shell in MWCNT, respectively. The equivalent bundle inductance (L'_{Bundle}) consists of (1) kinetic inductance (L'_K) that originates from kinetic energy of electrons and (2) magnetic

Table 3: Percentage reduction of out-phase delay for 10-shell MWCNT bundled TSV w.r.t. SWCNT, DWCNT, and 4-shell and 8-shell MWCNT bundle based TSVs.

TSV heights (μm)	% reduction in delay for MWCNT bundle (shell = 10) in comparison to			
	SWB	DWB	MWB (shell = 4)	MWB (shell = 8)
50	78.14	60.86	35.98	10.19
100	85.27	70.12	44.12	10.55
150	88.61	75.69	49.89	13.49
200	90.37	78.84	53.67	15.99

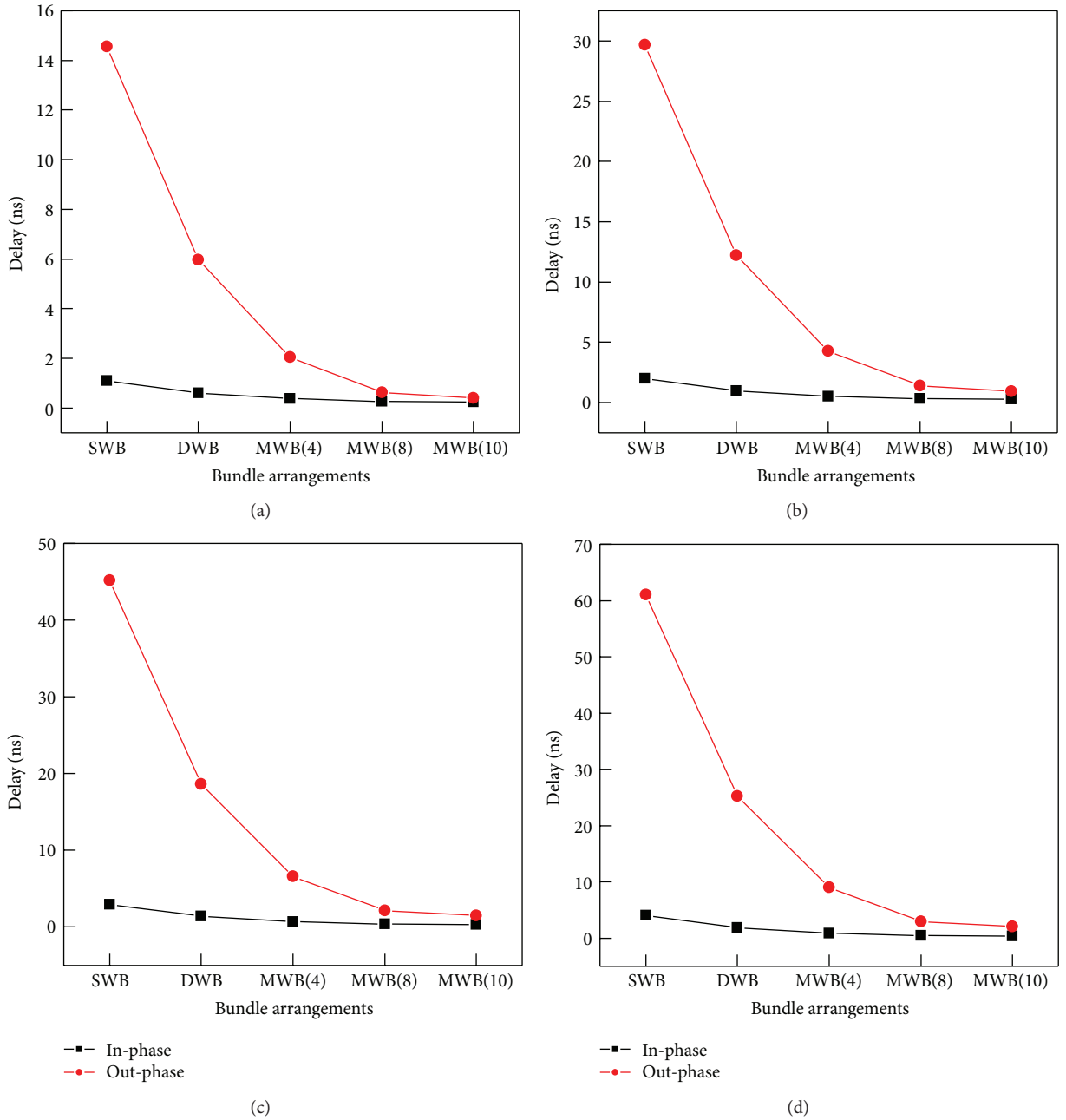

Figure 6: Crosstalk delays for different CNT bundles at (a) 50 μm, (b) 100 μm, (c) 150 μm, and (d) 200 μm TSV heights, where SWB, DWB, MWB(4), MWB(8), and MWB(10) represent the bundled SWCNT, DWCNT, and 4-shell, 8-shell, and 10-shell MWCNTs, respectively.

inductance (L'_M) that is due to the magnetic field induced by the current flowing through a nanotube [25]. Therefore, the L'_{Bundle}, L'_K and L'_M can be expressed as

$$L'_{\text{Bundle}} = \frac{L'_K}{2N_{\text{Total}}} + L'_M, \tag{10}$$

where

$$L'_K = \frac{h}{2e^2 v_F}, \qquad L'_M = \frac{\mu}{2\pi} \ln\left(\frac{y}{d_{\text{CNT}}}\right). \tag{11}$$

$y(= 1\,\mu m)$ is the distance between the CNT bundle and the ground plane. Tubes within the same and different bundled TSVs experience a coupling capacitance C_{CM} as shown in Figure 5. The C_{CM} has significant effect on crosstalk delay and primarily depends on the spacing between aggressor and victim ($S_{\text{a-v}}$) lines, number of peripheral SWCNTs/MWCNTs ($N_{\text{periphery}}$), and the outermost shell diameter (D_n). The C'_{CM} can be expressed as

$$C'_{CM} = \frac{\pi\varepsilon_0\varepsilon_r}{\cosh^{-1}\left(S_{\text{a-v}}/D_n\right)} \times N_{\text{periphery}}. \tag{12}$$

The quantitative values of the parasitics associated with different CNT bundled TSVs are placed in Table 1. These parasitic values are obtained using total numbers of conducting channels associated with each CNT in a bundle.

3. Signal Integrity Analysis

Crosstalk (signal integrity) in coupled lines is broadly classified in two categories: (1) functional and (2) dynamic crosstalk. Under functional crosstalk category, victim line experiences a voltage spike when the aggressor line switches. On the other hand, dynamic crosstalk is observed when aggressor and victim line switches simultaneously. A change in propagation delay is experienced under dynamic crosstalk when adjacent line (aggressor and victim) switches either in the same direction (in-phase) or in the opposite direction (out-of-phase) [26]. This section analyzes the in-phase and out-phase crosstalk delays using capacitively coupled TSV lines as shown in Figure 5. The TSVs in Figure 5 is primarily modeled by the equivalent *RLC* line of different SWCNT, DWCNT, and MWCNT bundles presented in Figure 3. A CMOS driver with supply voltage $V_{dd} = 1$ V is used for accurate estimation of crosstalk delay. The TSV lines are terminated by a load capacitance $C_L = 10$ aF.

Using the above mentioned setup and equivalent *RLC* model, Figure 6 presents the in-phase and out-phase delays for bundled SWCNT, DWCNT, and 4-shell, 8-shell, and 10-shell MWCNTs at different TSV heights ranging from 50 μm to 200 μm with a step size of 50 μm. Irrespective of heights, it is observed that both the in-phase and the out-phase delays are significantly reduced for MWCNT bundle (number of shells = 10) compared to the SWCNT, DWCNT, and 4-shell and 8-shell MWCNT bundled TSVs. The primary reason behind this reduction is the lower quantitative value of C'_{CM} (Table 1) that primarily depends on the number of CNTs in peripheral layers ($N_{\text{periphery}}$). For a fixed via radius, the number of 10-shell MWCNTs in periphery is lesser compared to the SWCNT, DWCNT, and 4-shell and 8-shell MWCNT bundled TSVs. Therefore, C'_{CM} is substantially reduced (shown in Table 1) that results in minimum crosstalk delay for the bundled TSV having MWCNTs of 10 shells.

Using different CNT bundles, the percentage reduction of in-phase and out-phase crosstalk delays for the 10-shell MWCNT bundle TSV is presented in Tables 2 and 3, respectively. Compared to bundled SWCNT, the overall reduction of in-phase and out-phase crosstalk delays of MWCNT bundle (shell = 10) is 96.85% and 85.59%, respectively.

4. Conclusion

This research paper presented an equivalent electrical model of a pair of CNT bundle based TSVs. The bundles having SWCNTs, DWCNTs, and MWCNTs with different number of shells are used as filler materials. Using capacitively coupled TSV lines, signal integrity is analyzed for different bundle configurations. Encouragingly, it is observed that the overall in-phase and out-phase crosstalk delays are substantially reduced for the bundled TSV having MWCNTs with higher diameters in comparison to the bundle having SWCNTs, DWCNTs, and MWCNTs of smaller diameters.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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