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Research Article

Investigation of the Low-Temperature Behavior of FD-SOI MOSFETs in the Saturation Regime Using Y and Z Functions

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The saturation regime of two types of fully depleted (FD) SOI MOSFET devices was studied. Ultrathin body (UTB) and gate recessed channel (GRC) devices were fabricated simultaneously on the same silicon wafer through a selective "gate recessed" process. They share the same W/L ratio but have a channel film thickness of 46 nm and 2.2 nm, respectively. Their standard characteristics ($I_{\rm DS}$ - $V_{\rm DS}$ and $I_{\rm DS}$ - $V_{\rm GS}$) of the devices were measured at room temperature before cooling down to 77 K. Surprisingly, their respective temperature dependence is found to be opposite. In this paper, we focus our comparative analysis on the devices' conduction using a Y-function applied to the saturation domain. The influence of the temperature in this domain is presented for the first time. We point out the limits of the Y-function analysis and show that a new function called Z can be used to extract the series resistance in the saturation regime.

1. Introduction

Planar fully depleted silicon-on-insulator (FD-SOI) technology relies on a silicon wafer having an ultrathin layer of crystalline silicon smartly built over a buried oxide (BOX) layer. Transistors built into this top silicon layer (whose thickness ranges in the decananometer thickness) are called ultrathin body (UTB) devices. Such devices have unique and extremely attractive characteristics for coming technology nodes. Since performance needs are increased together with power consumption control, UTB/FD-SOI is also a key technology for addressing high speed and leakage control. In the past several years, this technology has gained significant momentum in the mobile communications market space [1, 2]. FD-SOI devices were deeply analyzed across the literature, including the influence of the BOX/Si interface [3].

In a recent publication [4], we analyzed the transfer characteristics of the ultrathin body (UTB) and gate recessed channel (GRC) devices, sharing same W/L ratio (80 μ m/8 μ m) but having a channel film thickness of 46 nm and 2.2 nm, respectively. These characteristics were, respectively, measured in the linear domain for two temperatures: at 300 K and at 77 K. By decreasing the temperature, it was

found that the electrical behaviors of these devices were radically opposite: if, for UTB device, the conductivity was increased, the opposite effect was observed for GRC. Moving forward in the research, it was important to check if such kind of phenomenon (decreasing mobility by decreasing temperature) is also occurring in the saturation regime of the devices (higher currents). Using Y-function and Z-function analyses, both output and transfer characteristics of UTB and GRC devices were deeply investigated by varying the temperature from 300 K to 77 K.

The results confirmed that, for GRC device, the conduction exhibits a nonregular trend; that is, the extracted mobility is decreased by lowering the temperature. Using Y-function and complementary Z-function analyses, we could interpret this trend by the existence of very high series resistance values. The Y-function analysis in the saturation regime was recently published [5] at room temperature; however, no complementary analysis of both Y and Z functions was used to emphasize the nonstandard and opposite behavior of the mobility between UTB and GRC at low temperature. 2-dimensional TCAD process simulations of the UTB and GRC devices are, respectively, given for illustration in

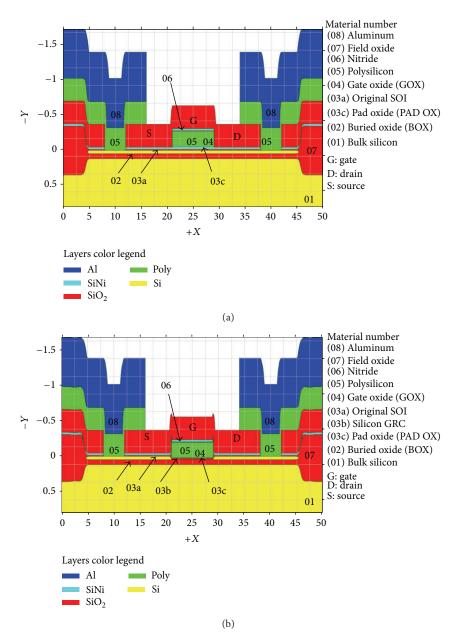


FIGURE 1: (a) 2-dimensional TCAD process simulation of the UTB device (scales are microns). (b) 2-dimensional TCAD process simulation of the GRC device (scales are microns).

Figures 1(a) and 1(b). An HRTEM image of a GRC device zoomed in its channel area is presented in Figure 2.

2. Electrical Characterizations and Analysis

2.1. Output Characteristics. The $I_{\rm DS}$ versus $V_{\rm DS}$ output characteristics in saturation mode (ranging from 0 to +3 V for UTB's and from 0 to +8 V for GRC's) were measured for a set of five gate voltage ($V_{\rm GS}$) values: 0 V, 1 V, 2 V, 3 V, and 4 V, respectively. In Figures 3(a) and 3(b), these characteristics are presented for the UTB device (46 nm channel thick) at 300 K (room temperature) and 77 K (liquid nitrogen), respectively. In Figures 3(c) and 3(d), the same characteristics are

presented for the GRC device (2.2 nm channel thick) having the same W/L ratio of 80 μ m/8 μ m for theses temperatures, respectively. By comparing Figures 3(a) to 3(c), the GRC's drain saturation current measured at 300 K (for $V_{\rm DS}=7$ V) is three orders of magnitude lower than those measured for UTBs at the same temperature (for $V_{\rm DS}=3$ V). But at 77 K, by comparing Figures 3(b) to 3(d), the saturation current ratio has almost reached five orders of magnitude. Such a huge current attenuation is not necessarily connected to a dumping of the electron mobility but can be related to the apparition of a huge series resistance during the channel thinning ("gate recessed" process) [6].

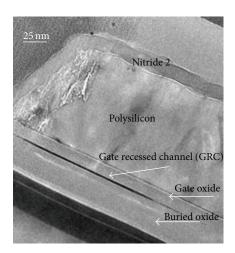


FIGURE 2: HRTEM image of a gate recessed channel (GRC) device, showing a view of the gate edge region. The silicon GRC film is 2.2 nm thick, while the gate oxide and the buried oxide films are, respectively, 26 nm and 70 nm thick.

2.2. Y-Function Analysis in the Saturation Domain. Ghibaudo et al. [7] introduced first the Y-method which has the interest to resolve the respective contributions of the intrinsic channel conduction from the series resistance. However, this extraction of series resistance usually relies on a set of devices with different channel lengths and is limited to the linear domain of device operation. In a previous study [8], we used this technique to extract the series resistance in the linear domain from the transfer characteristics. As a novelty, we proposed to apply this method to the same devices in the saturation domain.

Starting from the analytic expression of the saturation current [9],

$$I_{\mathrm{DS,sat}} \equiv \beta \frac{\left(V_{\mathrm{GS}} - V_{T} - \alpha V_{\mathrm{DS,sat}}\right)}{1 + \theta_{1} \left(V_{\mathrm{GS}} - V_{T}\right)} V_{\mathrm{DS,sat}} \tag{1}$$

With:
$$\beta = \frac{W}{L}C_{\text{ox}}\mu_0$$
. (2)

And μ_0 is the low field electron mobility. θ_1 is the "extrinsic" mobility degradation factor including the series resistance according to

$$\theta_1 = \theta_{1,0} + R_{\rm SD}\beta,\tag{3}$$

while $\theta_{1,0}$ is the "intrinsic" mobility degradation factor. The saturation voltage can be modeled by [9]

$$V_{\rm DS,sat} = \frac{1}{2\alpha} \left(V_{\rm GS} - V_T \right). \tag{4}$$

From Figure 3, we can point out the $V_{\rm DS,sat}$ value for each $V_{\rm GS}$ for a given device and temperature. V_T is extracted using the Y versus $V_{\rm GS}$ graph as described below. Using (4) and by measuring $V_{\rm DS,sat}$ from Figure 3, α is found to be about 0.75 and 0.2 for UTB and GRC, respectively, for both 300 K and 77 K. Since α is mainly connected to the capacitance ratio between the silicon channel and the front gate [9], it is independent of the temperature.

Assuming the same definition as used in the linear domain, the *Y* function in the saturation domain can be expressed by

$$Y_{\text{sat}} \equiv \frac{I_{\text{DS,sat}}}{\sqrt{g_{m,\text{sat}}}} \tag{5}$$

with the $g_{m,\text{sat}}$ being the transconductance in the saturation domain.

For the sake of model's simplicity, we assume that, at sufficiently high V_{GS} , θ_1 is no longer dependent on V_{GS} , so

$$\frac{\partial \theta_1}{\partial V_{\rm GS}} \ll \frac{\theta_1}{V_{\rm GS} - V_T}.\tag{6}$$

Then, by taking the derivative of (1) and after reduction of the expression (5), the *Y* function at saturation can be finally described by

$$Y_{\text{sat}} = \frac{\sqrt{A} (V_{\text{GS}} - V_T)^{3/2}}{\sqrt{\theta_1 (V_{\text{GS}} - V_T) + 2}} = \frac{\sqrt{A} (V_{\text{GS}} - V_T)}{\sqrt{\theta_1 + 2/(V_{\text{GS}} - V_T)}}$$
(7)

With:
$$A = \frac{\beta}{4\alpha}$$
. (8)

We would consider two limit cases.

First, if $R_{\rm SD}$ is negligible, then from (3), θ_1 should be also negligible relatively to $2/(V_{\rm GS}-V_T)$, so Y function at saturation can be approximated by

$$Y_{\rm sat} \approx \sqrt{\frac{A}{2}} \left(V_{\rm GS} - V_T \right)^{3/2}. \tag{9}$$

Then the $Y^{2/3}$ function is expected to be linear with $V_{\rm GS}$ in this limit case.

Secondly, if $R_{\rm SD}$ is dominating, then, from (3), θ_1 is also dominating relatively to $2/(V_{\rm GS}-V_T)$ and Y function at saturation can be approximated by

$$Y_{\rm sat} \approx \sqrt{\frac{A}{\theta_1}} \left(V_{\rm GS} - V_T \right).$$
 (10)

Consequently, the Y function is expected to be linear with $V_{\rm GS}$ in this limit case as observed for the classic Y function in the linear domain. This feature is useful to extract the V_T values. But, unlike classic Y function, the $Y_{\rm sat}$ expression is now dependent of $R_{\rm SD}$ through θ_1 .

The Y- $V_{\rm GS}$ graphs can be straight forward derived from the $I_{\rm DS}$ - $V_{\rm GS}$ characteristics measured at a given $V_{\rm DS,sat}$ (3 V) in the 0–4 V range as shown in Figures 4(a) and 4(b) for UTB at 300 K and 77 K, respectively. In Figures 4(c) and 4(d), $I_{\rm DS}$ - $V_{\rm GS}$ and Y- $V_{\rm GS}$ graphs are presented for GRC at 300 K and 77 K, respectively, for W/L = 80 μ m/8 μ m at a given $V_{\rm DS,sat}$ (7 V). In Figures 4(a) to 4(d), $Y^{2/3}$ $V_{\rm GS}$ is also plotted for comparison to the first limit case. We can see there that for UTB the $Y^{2/3}$ functions are almost more linear than the Y functions, as expected from the first limit case (9), but are significantly bended at lower $V_{\rm GS}$ values at 77 K. For GRC,

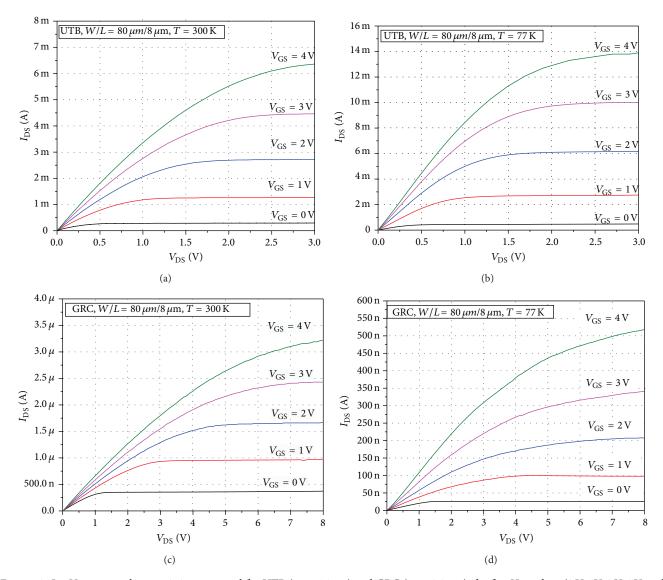


FIGURE 3: I_{DS} - V_{DS} output characteristics measured for UTB (t_{SI} = 46 nm) and GRC (t_{SI} = 2.2 nm), for five V_{GS} values (0 V, 1 V, 2 V, 3 V, and 4 V) and at two temperatures: (a) UTB at T = 300 K, (b) UTB at T = 77 K, (c) GRC at T = 300 K, and (d) GRC at T = 77 K.

the Y functions are linear with $V_{\rm GS}$ as expected by the second limit case at high $V_{\rm GS}$ values from (10).

According to (9), we can extract the threshold value V_T for UTB from the intercept of the $Y^{2/3}$ function with the $V_{\rm GS}$ axis. The extracted values of V_T , obtained at saturation condition for the different temperatures, are summarized in Table 1. The low field electron mobility μ_0 can be extracted directly from the slope parameter b of the $Y^{2/3}$ function through the β parameter using (2) and (9). Consequently,

$$\mu_0 = \beta \left(\frac{L}{WC_{\rm ox}}\right),\tag{11}$$

where:
$$\beta = 4\alpha A = \alpha (2b)^3$$
. (12)

For UTB, the $C_{\rm ox}$ value is $121\,{\rm nF/cm^2}$ since a 38 nm thick nitride layer is capping the pad oxide in the gate region. The extracted values of μ_0 obtained at saturation conditions for the different respective temperatures are summarized in Table 1. As mentioned above, α is taken as 0.75 for UTB.

2.3. Z-Function Analysis in the Saturation Domain for GRC. If by using (10) the Y function can be used to extract the V_T values for GRC, it cannot be used to extract the GRC low field electron mobility μ_0 from the slope since A and θ_1 parameters are coupled. So it is necessary to introduce a new function that decouples theses parameters, by using the so-called X function [10] defined as follows:

$$X_{\text{sat,GRC}} \equiv \frac{1}{\sqrt{g_{m.\text{sat}}}} = \sqrt{\frac{\theta_1}{A}} \left[\frac{1}{\theta_1 (V_{\text{GS}} - V_T)} + 1 \right].$$
 (13)

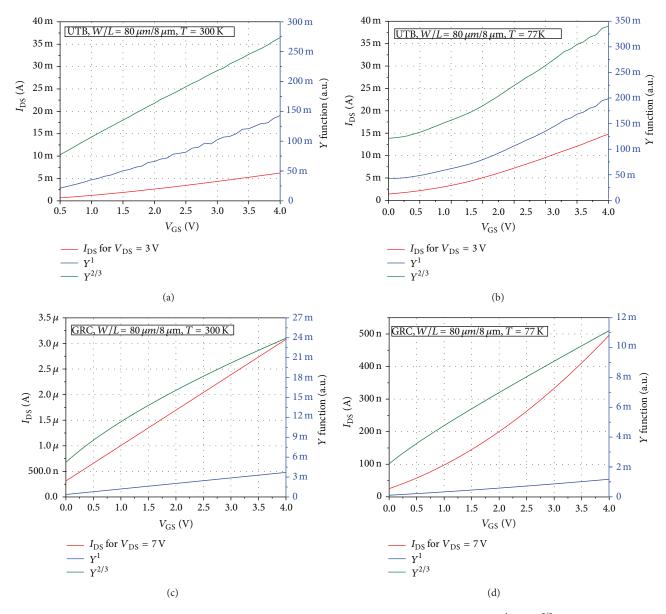


FIGURE 4: $I_{\rm DS}$ - $V_{\rm GS}$ characteristics measured in the saturation domain and corresponding Y-functions (Y^1 and $Y^{2/3}$) for UTB ($t_{\rm SI}=46$ nm) and GRC ($t_{\rm SI}=2.2$ nm) taken at $V_{\rm DS}=3$ V and $V_{\rm DS}=7$ V, respectively: (a) UTB, W/L=80 μ m/8 μ m, T=300 K. (b) UTB, W/L=80 μ m/8 μ m, T=77 K. (c) GRC, W/L=80 μ m/8 μ m, T=300 K. (d) GRC, W/L=80 μ m/8 μ m, T=77 K.

However, in our case the $X_{\rm sat}$ function cannot still discriminate between A and θ_1 . So we will use the Z function defined by the product of X and Y functions as follows:

$$Z_{\rm sat,GRC} \equiv X_{\rm sat,GRC} \cdot Y_{\rm sat,GRC} = \frac{I_{\rm DS,sat}}{g_{m,\rm sat}} = \frac{1}{\theta_1} + \left(V_{\rm GS} - V_T\right). \tag{14}$$

Now θ_1 can be extracted from the intercept of the Z function with Z axis as shown in Figure 5 for GRC's devices having a W/L of 80 μ m/8 μ m. As assumed in (10) a linear fit is taken for sufficient high $V_{\rm GS}$ values.

Note that if at 300 K, the slope of the Z versus $V_{\rm GS}$ plot is 1 for 80 μ m/8 μ m, it is found to be much lower than 1 (0.58)

at 77 K. This seems to indicate a temperature dependence of the limit case presented in (14). However, the slope of the Z versus $V_{\rm GS}$ is not critical issue for the parameter extraction method and is ignored.

Finally from the θ_1 extraction and using the slope of the *Y* function, the *A* and then μ_0 parameters for GRC can be extracted using (10) and (2)–(8), respectively, and taking $\alpha=0.2$. Results are presented in Table 2 for the different temperatures. For GRC the $C_{\rm ox}$ value was (138 nF/cm²) by considering the 26 nm thick gate oxide as seen in Figure 2.

From (3), we can see that the low values of the β parameter for GRC should be compensated by a very high value of $R_{\rm SD}$ in order to get the high θ_1 ($\gg 1\,{
m V}^{-1}$) values as presented in Table 2. Here, the intrinsic parameter $\theta_{1,0}$ is assumed

Table 1: Summarizing table of the threshold voltage V_T , the b slope extracted from the $Y^{2/3}$ versus $V_{\rm GS}$ function, the subsequent β parameter, and saturation mobility μ_0 for UTB device at 300 K and 77 K. $V_{\rm DS}$ = 3 V (saturation domain).

Temperature [K]	300	77	Shift or ratio 300 K/77 K
$V_T\left[\mathrm{V} ight]$	-0.89	-0.40	-0.51
$b = \text{slope } Y^{2/3} \text{ versus } V_{GS} \text{ [metric units]}$	0.0563	0.0774	0.73
β [mS/V] from (12)	1.064	2.775	0.38
$\mu_0 [\text{cm}^2/\text{Vs}] \text{from (11)}$	880	2300	0.38

Table 2: Summarizing table of the extracted parameters for GRC's having W/L ratio of 80 μ m/8 μ m at $V_{\rm DS}$ = 7 V (saturation) for both 300 K and 77 K. Threshold voltage V_T is extracted from the Y function while the θ_1 factor is extracted from the Z function. The β parameter and the subsequent saturation mobility μ_0 are extracted from the Y function slope. Extracted series resistance $R_{\rm SD}$ is appended accordingly.

Temperature [K]	300	77	Shift or ratio 300 K/77 K
V_T [V] from (10)	-0.55	-0.24	+0.31
$ \theta_1 $ [V ⁻¹] from (14)	7.87	2.65	3
$\beta [\mu S/V]$ from (12)	3.84	0.15	26
μ_0 [cm ² /Vs] for GRC from (11)	2.78	0.11	26
μ_0 [cm ² /Vs] for UTB (given as reference)	880	2300	0.38
$R_{\rm SD}$ [M Ω] from (15)	2.05	17.4	0.12

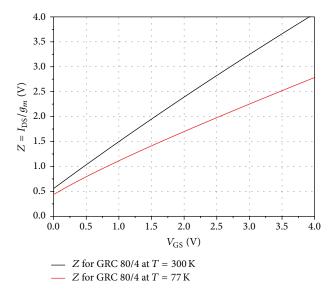


FIGURE 5: Z function versus $V_{\rm GS}$ for GRC device ($W/L=80~\mu{\rm m}/8~\mu{\rm m}$) at 300 K and 77 K measured in the saturation domain ($V_{\rm DS}=7~{\rm V}$). θ_1 is extracted from the reciprocal of the Z function intercept with vertical axis.

negligible since the gate oxide is relatively thick in such a way that the mobility should be weakly gate dependent. Then, the series resistance $R_{\rm SD}$ could be extracted directly from the following expression:

$$R_{\rm SD} = \frac{\theta_1}{\beta}.\tag{15}$$

3. Interpretation and Discussion

3.1. Behavior of the I_{DS} - V_{DS} Saturation at Low Temperature. Firstly, from Figure 3, we can see that both UTB and GRC

are depletion-type devices (normally open, i.e., negative V_T for p-type channel) at 300 K and 77 K. From Table 1, the UTB's threshold voltage V_T is increased by decreasing the temperature which is in accordance with the decreasing of the Fermi potential as observed in similar devices [11]. Secondly, the low field electron mobility μ_0 is increased by decreasing the temperature which is consistent with the classic increasing of mobility at low temperature (<150 K) due to the freezing of phonon scattering [12]. However, from Table 2, for the GRC device, μ_0 parameter is surprisingly decreased by decreasing the temperature. So, when lowering the temperature, the conduction was increased in UTB, while the opposite effect is observed for GRC. As seen in Table 2, this should be correlated to the increase of the series resistance as extracted from the Y- and Z-function analysis. This trend can be physically explained by the freeze-out of the silicon dopants outside the GRC channel as reported in [13]. Moreover, for the UTB device, the extracted μ_0 values are similar to those expected in similar silicon based devices [14], while, for GRC device, the corresponding μ_0 values are found to be very low and are inconsistent with such kind of fully depleted SOI MOSFETs [15]. Consequently, this corroborates the influence of a series resistance in the GRC's case.

3.2. Comparison to Extraction Method in the Linear Regime. The $I_{\rm DS}\text{-}V_{\rm GS}$ behavior at low temperature in the linear regime was studied in a previous publication [4]. Using the Y-function method based on a first order analysis has been shown to be effective to interpret the radically opposite electrical behavior which was observed at low temperature. In Table 3, for UTB device, the threshold voltage $V_T,~\beta$ parameter, and mobility μ_0 extracted from saturation and linear domain at 300 K and 77 K, respectively, are compared. The threshold voltage values extracted from the saturation are found more negative and less dispersed than those extracted from the linear domain, especially at 77 K. This seems to

-	the threshold voltage V_T , β parameter, and UTB device ($W/L = 80 \ \mu \text{m}/8 \ \mu \text{m}$).	mobility μ_0 extracted from saturation and linear method [4] at
Extraction domain	Saturation	Linear

Extraction domain	Saturation			Linear		
Temperature [K]	300 K	77	Shift or ratio 300 K/77 K	300	77	Shift or ratio 300 K/77 K
$V_T\left[\mathrm{V} ight]$	-0.89	-0.40	-0.51	-0.65	+0.26	-0.91
β [mS/V]	1.064	2.775	0.38	1.47	2.41	0.61
$\mu_0 [\text{cm}^2/\text{Vs}]$	880	2300	0.38	1210	2000	0.61

Table 4: Comparative table of threshold voltage V_T , β , and mobility μ_0 extracted from saturation and linear domain [4] at 300 K and 77 K, respectively, for GRC device ($W/L = 80 \ \mu \text{m/8} \ \mu \text{m}$).

Extraction domain	Saturation			Linear		
Temperature [K]	300	77	Shift or ratio 300 K/77 K	300	77	Shift or ratio 300 K/77 K
$V_T [V]$	-0.55	-0.24	-0.31	-2.35	-2.60	+0.25
β [μS/V]	3.84	0.15	26	0.31	0.007	44
$\mu_0 [\mathrm{cm}^2/\mathrm{Vs}]$	2.78	0.11	26	0.222	0.005	44
$R_{\mathrm{SD}}\left[\mathrm{M}\Omega\right]$	2.05	17.4	0.12	1.73	8.93	0.19

be more consistent with the model of the threshold voltage temperature dependence [16]. Moreover, the mobility values extracted from the saturation domain are found also to be in better agreement with the expected values for similar devices [17].

In Table 4, threshold voltage V_T , β parameter, mobility μ_0 , and $R_{\rm SD}$ extracted from saturation and linear domain at 300 K and 77 K, respectively, for GRC are compared.

Unlike threshold voltage values extracted from the linear domain, those from the saturation regime are found less negative and are decreasing by lowering the temperature. Again, it seems to be more consistent with the model of the threshold voltage temperature dependence [16]. If the extracted mobility values from the saturation domain are about 10 times higher than those extracted from the linear domain, they are still lower than the expected values for such kind of devices [15]. However, the series resistance $R_{\rm SD}$ extracted from the saturation domain is still comparable to those extracted from the linear domain. So the series resistance is less sensitive to the extraction domain than the mobility showing the better consistency of this interpretation.

3.3. Extraction of the Effective Mobility Using Conventional C-V Method. In order to corroborate our previous results about the electron channel mobility and the series resistance extraction method, we could independently extract the mobile channel charge density $Q_{\rm inv}$ and finally the effective electron mobility $\mu_{\rm eff}$ according to the respective definitions [18]:

$$Q_{\text{inv}} = \frac{1}{WL} \int_{-\infty}^{V_{\text{GDS}}} C_p dV_{\text{GDS}} \sim \frac{1}{WL} C_{\text{ox}} \left(V_{\text{GDS}} - V_T \right)$$

$$\sim 29 \,\text{nC/cm}^2$$
(16)

$$\mu_{\text{eff}} \equiv \frac{g_d L/W}{Q_{\text{inv}}} = 0.074 \,\text{cm}^2/\text{Vs},$$
 (17)

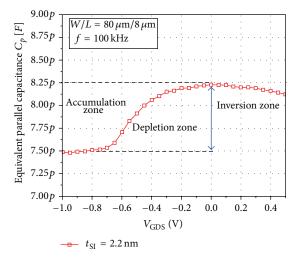


FIGURE 6: Parallel mode C_P - $V_{\rm GDS}$ characteristics for GRC with 2.2 nm channel film thickness. The device has the same gate $W \times L = 80 \times 8 \ \mu {\rm m}^2 = 6.4 \times 10^{-6} \ {\rm cm}^2$. The capacitance C_P was measured at 100 kHz. Drain and source are shorted.

where $C_{\rm ox}$ is oxide capacitance measured as the step of the C-V plot at $V_{\rm GDS}=0$ V (inversion zone) according to Figure 6, while the threshold voltage V_T is taken as -0.25 V and is matching the corresponding value in Table 4 at 77 K. The channel conductance g_d is 21 nS as measured from the slope of the $I_{\rm DS}$ - $V_{\rm DS}$ plot at $V_{\rm GS}=0$ V in Figure 3(d).

The effective electron mobility $(0.074\,\mathrm{cm^2/Vs})$ is found close to the corresponding value in Table 4 at 77 K $(0.11\,\mathrm{cm^2/Vs})$ which corroborates our extraction method based on Z-function analysis in the saturation domain. Consequently, this measurement well confirms that the extracted effective mobility is too low in particular at low temperature. So the series resistance seems to be a more valuable parameter to explain the low conductivity of such nanoscale devices.

4. Conclusion

By studying the electrical characteristics in the saturation regime at room and low temperature (77 K), we confirm the opposite behavior observed in the linear regime between ultrathin body (UTB) and gate recessed channel (GRC) devices having a channel film thickness t_{SI} of 46 nm and 2.2 nm, respectively, and a fixed W/L ratio. If the apparent conductivity is increased for UTB by lowering the temperature, the opposite effect is observed for GRC. This phenomenon, which is not in accordance with the classical interpretation of the phonon scattering model, is consistently explained by a massive series resistance which is increased at low temperature due to the freeze-out effect of the dopants. By comparison to the linear domain, the use of *Y* and *Z* functions in the saturation regime allows extracting more accurate values of the threshold voltage and mobility parameters for UTB and a consistent series resistance for GRC devices. From a general point of view, such an analysis should be useful to interpret high series resistance effect in new nanoscale devices.

Conflict of Interests

The authors have no conflict of interests associated with this paper.

References

- [1] T. Skotnick, F. Arnauld, and O. Faynot, "UTBB SOI: a wolf in sheep's clothing," in *Future Fab International*, vol. 42, pp. 72–79, 2012.
- [2] W. Schwarzenbach, N. Daval, V. Barec et al., "Atomic scale thickness control of SOI wafers for fully depleted applications," *ECS Transactions*, vol. 53, no. 5, pp. 39–46, 2013.
- [3] L. Zafari, J. Jomaah, and G. Ghibaudo, "Impact of BOX/ substrate interface on low frequency noise in FD-SOI devices," in Noise and Fluctuations in Circuits, Devices, and Materials, M. Macucci, L. K. J. Vandamme, C. Ciofi, and M. B. Weissman, Eds., vol. 6600 of Proceedings of SPIE, 2007.
- [4] A. Karsenty and A. Chelly, "Y-function analysis of the low temperature behavior of ultrathin FD SOI MOSFETs," *Active* and Passive Electronic Components, vol. 2014, Article ID 697369, 10 pages, 2014.
- [5] C. Diouf, A. Cros, S. Monfray et al., "Y function method applied to saturation regime: apparent saturation mobility and saturation velocity extraction," *Solid-State Electronics*, vol. 85, pp. 12–14, 2013.
- [6] A. Karsenty and A. Chelly, "Modeling of the channel thickness influence on electrical characteristics and series resistance in gate-recessed nanoscale SOI MOSFETs," *Active and Passive Electronic Components*, vol. 2013, Article ID 801634, 10 pages, 2013.
- [7] G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Electronics Letters*, vol. 24, no. 9, pp. 543–545, 1988.
- [8] A. Karsenty and A. Chelly, "Application, modeling and limitations of Y-Function based methods for massive series resistance in nanoscale SOI MOSFETs," *Solid-State Electronics*, vol. 92, pp. 12–19, 2014.

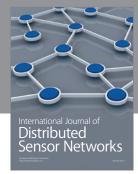
- [9] H.-K. Lim and J. G. Fossum, "Current-voltage characteristics of thin-film SOI MOSFET's in strong inversion," *IEEE Transac*tions on Electron Devices, vol. 31, no. 4, pp. 401–408, 1984.
- [10] A. Cros, S. Harrison, R. Cerutti, P. Coronel, G. Ghibaudo, and H. Brut, "New extraction method for gate bias dependent series resistance in nanometric double gate transistors," in *Proceedings* of the 2005 IEEE International Conference on Microelectronic Test Structures, vol. 18, pp. 69–74, April 2005.
- [11] T. Elewa, F. Balestra, S. Cristoloveanu et al., "Performance and physical mechanisms in SIMOX MOS transistors operated at very low temperature," *IEEE Transactions on Electron Devices*, vol. 37, no. 4, pp. 1007–1019, 1990.
- [12] S.-I. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: part I—effects of substrate impurity concentration," *IEEE Transactions on Electron Devices*, vol. 41, no. 12, pp. 2357–2362, 1994.
- [13] G. Ghibaudo and F. Balestra, "Characterization and modeling of silicon CMOS transistor operation at low temperature," *Journal de Physique IV*, vol. 6, no. 3, pp. C3-3–C3-11, 1996.
- [14] M. Schmidt, M. C. Lemme, H. D. B. Gottlob, F. Driussi, L. Selmi, and H. Kurz, "Mobility extraction in SOI MOSFETs with sub 1 nm body thickness," *Solid-State Electronics*, vol. 53, no. 12, pp. 1246–1251, 2009.
- [15] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. Takagi, "Experimental study on carrier transport mechanism in ultrathin-body SOI nand p-MOSFETs with SOI thickness less than 5 nm," in *Proceedings of the International Electron Devices Meeting (IEDM '02)*, pp. 47–50, 2002.
- [16] G. Groeseneken, J.-P. Colinge, H. E. Maes, J. C. Alderman, and S. Holt, "Temperature dependence of threshold voltage in thin-film SOI MOSFET's," *IEEE Electron Device Letters*, vol. 11, no. 8, pp. 329–331, 1990.
- [17] K. Uchida and S.-I. Takagi, "Carrier scattering induced by thickness fluctuation of silicon-on-insulator film in ultrathin-body metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters*, vol. 82, no. 17, pp. 2916–2918, 2003.
- [18] M. S. Liang, J. Y. Choi, P. K. Ko, and C. Hu, "Inversion-layer capacitance and mobility of very thin gate-Oxide MOSFET's," *IEEE Transactions on Electron Devices*, vol. 33, no. 3, pp. 409– 413, 1986.



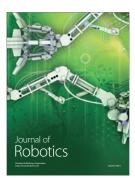














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