

Research Article

New Realizations of Single OTRA-Based Sinusoidal Oscillators

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Received 23 October 2013; Revised 3 January 2014; Accepted 6 January 2014; Published 10 March 2014

Academic Editor: Jiun-Wei Horng

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This study proposes three new sinusoidal oscillators based on an operational transresistance amplifier (OTRA). Each of the proposed oscillator circuits consists of one OTRA combined with a few passive components. The first circuit is an OTRA-based minimum RC oscillator. The second circuit is capable of providing independent control on the condition of oscillation without affecting the oscillation frequency. The third circuit exhibits independent control of oscillation frequency through a capacitor. This study first introduces the OTRA and the related formulations of the proposed oscillator circuits, and then discusses the nonideal effects, sensitivity analyses, and frequency stability of the presented circuits. The proposed oscillators exhibit low sensitivities and good frequency stability. Because the presented circuits feature low impedance output, they can be connected directly to the next stage without cascading additional voltage buffers. HSPICE simulations and experimental results confirm the feasibility of the new oscillator circuits.

1. Introduction

Sinusoidal oscillators constitute an important unit in numerous electronic devices, including electronic instruments, measurement systems, telecommunications, power conversion control circuits, and signal processing applications [1]. For the past several years, the typical configurations of sinusoidal oscillators in a wide array of circuit systems have combined operational amplifiers (op-amp) and additional passive components. A variety of sinusoidal oscillators using an op-amp as the active device are available [2, 3]. However, the finite gain bandwidth product of an op-amp decreases the oscillator circuit performance. To overcome this problem, researchers have investigated current-mode circuit techniques for signal processing in the past decades because they offer the advantages of greater accuracy, wider bandwidth, and higher slew rate than their voltage-mode counterparts [4]. Previous studies present several implementations of sinusoidal oscillators employing current conveyors (CCs) and current feedback amplifiers (CFOAs) [5–8], and the literature contains numerous sinusoidal oscillators constructed with different types of modern active devices [9–12]. Since the introduction of OTRA in 1992, it has become an important building block in analog circuit designs [13]. Subsequent

development led to two high-performance CMOS OTRA realizations [14, 15]. OTRA can also be implemented using commercially available ICs [16], and has sparked interest in the design of OTRA-based analog signal processing circuits. Several oscillator circuits based on OTRAs have been presented [17–21]. To our knowledge, the first reported oscillator circuits using OTRA as the active device appeared in [17]. That study first introduced three single OTRA-based oscillator circuits and then four additional topologies using two OTRAs. However, the main disadvantage of these circuits is that they require excessive active devices and passive components. To overcome this problem, an improved topology built with a single OTRA, three resistors, and two capacitors was subsequently reported to reduce the component count [18]. Recent research presents an OTRA-based oscillator with noninteractive control [19]. However, that design suffers from complex circuitry involving two OTRAs, three resistors, and three capacitors. A literature review presents other types of sinusoidal oscillators, such as quadrature oscillators and multiphase oscillators, that use OTRA as the active device [20, 21]. Previous study revealed that an available method for generating quadrature oscillators is based on the cascaded all-pass filters technology [20, 22, 23]. Although single OTRA-based sinusoidal oscillators

appear in previous reports, a number of effective topologies are missing in the literature. Therefore, the main purpose of this paper is to add three unpublished schemes to this list. One OTRA with a few passive components is required for the three topologies in this study. Because the OTRA-based application circuits got more and more attentions, we believe that these brand-new circuit configurations can be a good alternative to exploit OTRA for the design of sinusoidal oscillators. To illustrate the novelty of the proposed topologies, comparisons of various solutions are shown in Table 1. It should be noted that among the existing circuits, the proposed oscillators in this study feature the following benefits: (1) fewer or the same number of active devices and passive components is used; (2) independent control on the oscillation condition (oscillation frequency) without affecting the oscillation frequency (oscillation condition); (3) low active and passive sensitivities; (4) good frequency stability; (5) insensitive to the parasitic parameters; and (6) without an additional buffer for cascading applications. This paper is organized as follows. Section 2 first introduces the active OTRA device and then explains and analyzes the proposed circuits. Section 3 investigates the nonideal effects, sensitivity analysis, and frequency stability of the proposed circuits. Section 4 describes how examples were made for conducting simulation and experimental tests. Section 5 presents conclusions.

2. Circuit Descriptions

The OTRA design concept originated from the commercially available Norton amplifier [24, 25]. However, the Norton amplifier has not gained considerable attention because commercial products do not provide a virtual ground at the input terminals and they only allow the input currents to flow in one direction. These adverse conditions limit its applications. Therefore, an improved design was suggested and renamed as operational transresistance amplifier (OTRA) [13]. The OTRA is a trans-impedance type active building block with two current input terminals (I_+ and I_-) and a voltage output terminal (V_o), which means that the input currents control output voltage through a transresistance gain. Figure 1 shows a circuit diagram of the OTRA used in this study. Its terminal relationships can be defined by (1), where R_m represents the transresistance gain. In the ideal case, the transresistance gain R_m approaches infinity and the two input currents are forced to be equal. However, this would only happen when OTRA is used in closed feedback loop and the infinite feedback loop gain ensures this. Since the input terminals of OTRA are internally grounded, this active device is free from numerous parasitic effects [26]. Another advantage of using OTRA to design analog circuits is that it is possible to obtain very accurate transfer functions in cascading applications [20]:

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_o \end{bmatrix}. \quad (1)$$

Figure 2 depicts a feasible CMOS OTRA consisting of a differential current controlled current source (DCCCS)

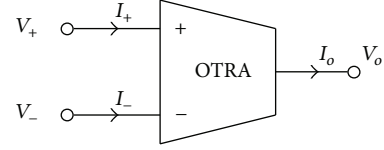


FIGURE 1: OTRA circuit diagram.

followed by a voltage buffer [15]. The DCCCS unit in this figure is based on transistors M_1 to M_{12} , and M_{13} to M_{20} form the voltage buffer. Furthermore, the OTRA can be easily implemented using commercially available ICs with a configuration consisting of two AD844ANs [16] (Figure 3). If terminal T_z of the second AD844AN is an open circuit, the precise behavior of an ideal OTRA can be determined. Because the AD844AN IC is widely used in a variety of analog circuits, the implementation depicted in Figure 3 provides a viable means with which to implement an OTRA even though such a device is not currently available.

Figure 4 shows the proposed new oscillators. Each circuit consists of a single OTRA and a few passive components. Since the minimum passive component sinusoidal oscillators have received much interest in the literature [27, 28], this study first introduces a $2R + 2C$ topology to fulfill the minimum RC component design (Figure 4(a)). Assuming an ideal OTRA characterized by (1), routine circuit analysis yields the characteristic equation expressed in (2). Equations (3) and (4) determine the oscillation condition and oscillation frequency, respectively. The oscillation condition and oscillation frequency cannot be independently controlled on this circuit because it is a minimum RC oscillator:

$$S^2 C_1 C_2 + S(G_1 C_2 + G_1 C_1 - G_2 C_1) + G_1 G_2 = 0, \quad (2)$$

$$\frac{G_2}{G_1} - 1 = \frac{C_2}{C_1}, \quad (3)$$

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}}. \quad (4)$$

To achieve independent control of the oscillation condition without affecting the oscillation frequency, the second topology employs one OTRA with three resistors and two capacitors (Figure 4(b)). Equations (5) to (7) derive the expressions of the characteristic equation, oscillation condition, and oscillation frequency for this circuit. Among them, G_1 , G_2 , and G_3 represent the corresponding admittances of the resistors R_1 , R_2 , and R_3 , respectively. Equations (6) and (7) show that the admittance G_3 can control the oscillation condition without affecting the oscillation frequency:

$$S^2 C_1 C_2 + S(G_1 C_1 + G_2 C_1 + G_3 C_1 - G_1 C_2) + G_1 G_2 = 0, \quad (5)$$

$$1 + \frac{G_2}{G_1} + \frac{G_3}{G_1} = \frac{C_2}{C_1}, \quad (6)$$

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}}. \quad (7)$$

TABLE 1: Comparisons among various sinusoidal oscillators.

Topology	Component numbers and passive component types	Classification of oscillator	Independent control of OC and OF	Signal output mode/buffer circuit requirement	Circuit implement technology
CCII-based [5]	CCII $\times 1$ resistor $\times 3$ (grounded) capacitor $\times 2$ (only one grounded)	SSO	Yes OC: by R OF: NA	VM/Yes	Commercial ICs
CFOA-based [8]	CFOA $\times 1$ resistor $\times 3$ (only one floating) capacitor $\times 3$ (grounded)	SSO	Yes OC: NA OF: by R	VM/No	Commercial ICs
CDBA-based (Topology a in Figure 2 of [9])	CDBA $\times 1$ resistor $\times 2$ (floating) capacitor $\times 2$ (only one grounded)	SSO	No OC: NA OF: NA	VM/No	Commercial ICs
FTFN-based [10]	FTFN $\times 2$ resistor $\times 4$ (only one grounded) capacitor $\times 2$ (grounded)	SSO	Yes OC: NA OF: by R	CM/No	Commercial ICs
DVCC-based [11]	DVCC $\times 1$ resistor $\times 2$ (grounded) capacitor $\times 2$ (grounded)	SSO	No OC: NA OF: NA	VM/Yes	CMOS realization
OTA-based (Topology a in Figure 2 of [12])	OTA $\times 1$ resistor $\times 4$ (only one grounded) capacitor $\times 2$ (grounded)	SSO	No OC: NA OF: NA	VM/Yes	Commercial ICs
OTRA-based (Topology b in Figure 3 of [17])	OTRA $\times 1$ resistor $\times 4$ (only one grounded) capacitor $\times 2$ (floating)	SSO	Yes OC: by R OF: NA	VM/No	CMOS realization
OTRA-based [18]	OTRA $\times 1$ resistor $\times 3$ (only one grounded) capacitor $\times 2$ (floating)	SSO	Yes OC: NA OF: by R	VM/No	CMOS realization
OTRA-based [19]	OTRA $\times 2$ resistor $\times 3$ (floating) capacitor $\times 3$ (floating)	SSO	Yes OC: by R OF: by R	VM/No	Commercial ICs
OTRA-based [20]	OTRA $\times 2$ resistor $\times 6$ (floating) capacitor $\times 2$ (floating)	QSO	No OC: NA OF: NA	VM/No	Commercial ICs
OTRA-based (Figure 2 of [21])	OTRA $\times n$ resistor $\times 2n$ (floating) capacitor $\times n$ (floating) (for n -phase output)	MSO	Yes OC: by R OF: NA	VM/No	Commercial ICs

TABLE 1: Continued.

Topology	Component numbers and passive component types	Classification of oscillator	Independent control of OC and OF	Signal output mode/buffer circuit requirement	Circuit implement technology
OTRA-based (proposed in Figure 4(a))	OTRA $\times 1$ resistor $\times 2$ (floating) capacitor $\times 2$ (floating)	SSO	No OC: NA OF: NA	VM/No	CMOS realization/Commercial ICs
OTRA-based (proposed in Figure 4(b))	OTRA $\times 1$ resistor $\times 3$ (only one grounded) capacitor $\times 2$ (floating)	SSO	Yes OC: by R OF: NA	VM/No	CMOS realization/Commercial ICs
OTRA-based (proposed in Figure 4(c))	OTRA $\times 1$ resistor $\times 2$ (floating) capacitor $\times 3$ (only one grounded)	SSO	Yes OC: NA OF: by C	VM/No	CMOS realization/Commercial ICs

OC: oscillation condition; OF: oscillation frequency; SSO: single-phase sinusoidal oscillator; QSO: quadrature sinusoidal oscillator; MSO: multiphase phase sinusoidal oscillator; NA: not available; VM: voltage-mode; CM: current-mode.

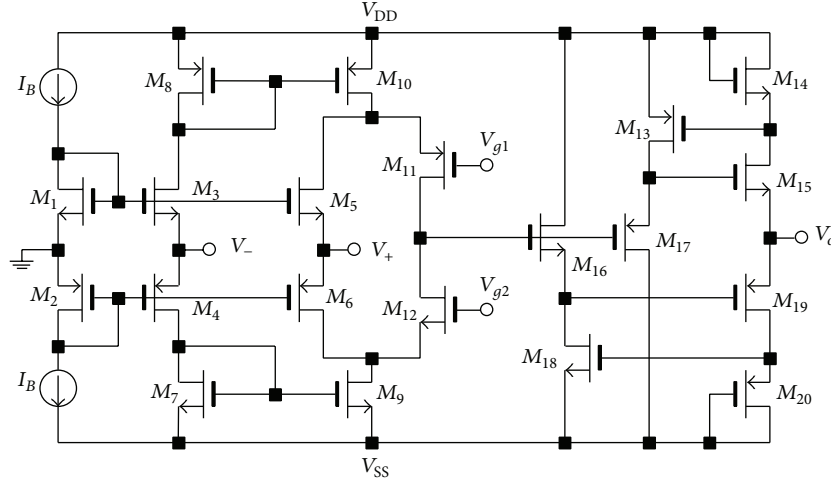


FIGURE 2: CMOS implementation of OTRA.

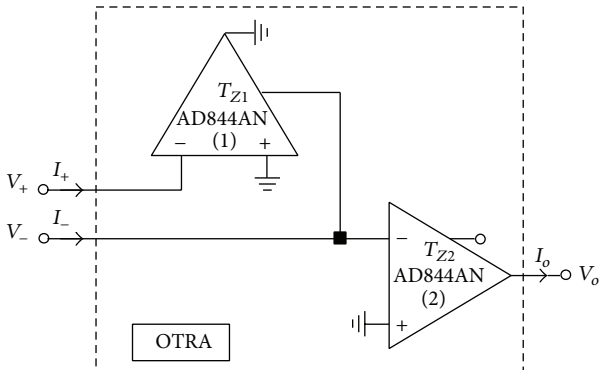


FIGURE 3: OTRA constructed using commercially IC AD844ANs.

It is also possible to achieve independent control of the oscillation frequency without affecting the oscillation condition. In this case, Figure 4(b) shows that changing the resistor R_3 to be a capacitor C_3 yields the third topology, shown in Figure 4(c). Routine circuit analysis shows that the characteristic equation, oscillation condition, and oscillation frequency of this circuit are expressed as

$$S^2 C_1 (C_2 + C_3) + S (G_1 C_1 + G_2 C_1 - G_1 C_2) + G_1 G_2 = 0, \quad (8)$$

$$1 + \frac{G_2}{G_1} = \frac{C_2}{C_1}, \quad (9)$$

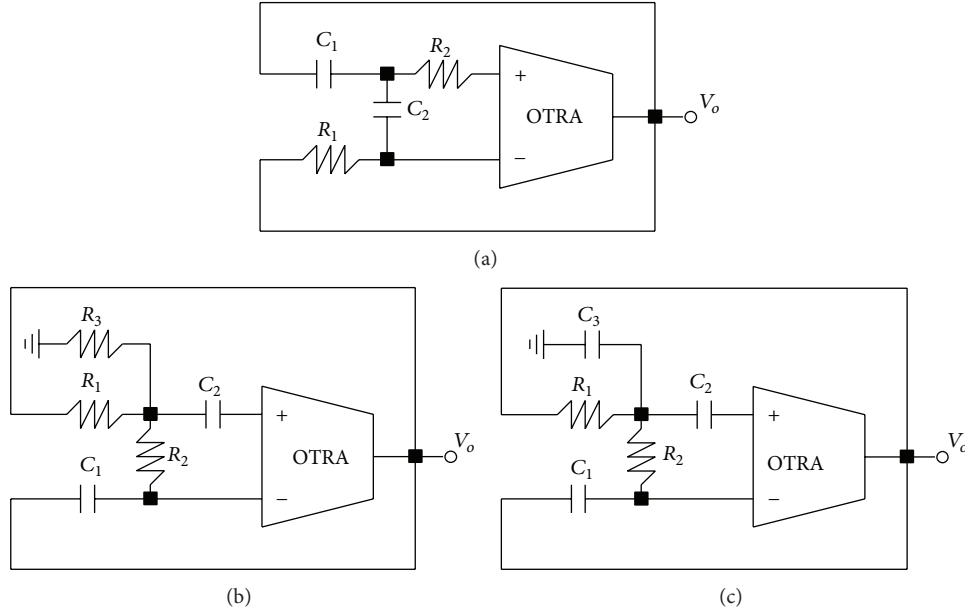


FIGURE 4: Circuit diagrams of the proposed single OTRA-based sinusoidal oscillators.

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 (C_2 + C_3)}}. \quad (10)$$

This oscillator can be considered a single capacitor-controlled oscillator (SCCO) because the oscillation frequency can be controlled independently by C_3 . The presented scheme in this study provides a more compact circuit topology than the previous design (single capacitor-controlled oscillator) reported in [17]. However, typical single capacitor-controlled oscillators cannot provide an excellent tuning capability for the oscillation frequency. To attain a high tuning capability of the oscillation frequency, a tunable capacitor simulated circuit can be applied to overcome this problem [29]. Compared with the topologies reported in [17] [Figures 3(b) and 3(c)], the proposed oscillators use relatively few passive components to realize the topologies for the independent control of the oscillation condition and oscillation frequency. Because OTRA-based application circuits have received more attention in recent years, the proposed oscillator circuits can serve as practical designs for apply in the OTRA circuit systems.

3. Nonideal Analysis of the Proposed Circuits

This section considers several nonideal characteristics to determine the influences of nonideal effects on the proposed circuits. According to the datasheet [30], show that an AD844AN IC can be modeled as a positive second-generation current conveyor (CCII+) cascading a voltage buffer with inherent parasitic resistances and finite tracking errors. Figure 5 reveals a more sophisticated circuit model of the OTRA (Figure 3), where R_x and R_z are the terminal parasitic resistances. In this design, R_x is on the order of several tens of ohms, whereas R_z is in the range of a few mega-ohms. β represents the current tracking error factor

from terminal T_z with respect to the inverting terminal. The AD844AN datasheet indicates that the standard values of these parameters are $\beta = 0.98$, $R_x = 50 \Omega$, and $R_z = 3 \text{ M}\Omega$. Figure 5 includes the resulting expressions of the related currents. The parasitic resistance at the noninverting terminal and voltage tracking error effect between the inverting and noninverting terminals of CCII+ both disappear in the circuit model because of the ground connection at the noninverting terminal for each CCII+.

After applying the nonideal OTRA equivalent circuit model to the proposed circuits shown in Figure 4, tedious derivations lead to the following modified characteristic equations, oscillation condition, and oscillation frequency. The characteristic equation of Figure 4(a) becomes

$$\begin{aligned} & s^2 \left(C_1 C_2 \left(\beta + \frac{G_z}{G_x} \right) \right) \\ & + s \left(\beta G_1 C_1 + \beta G_1 C_2 + \frac{G_1 G_z}{G_x} C_1 + \frac{G_1 G_z}{G_x} C_2 \right. \\ & \quad \left. + \frac{2 G_2 G_z}{G_2 + G_x} C_2 - \beta \frac{G_2 G_x}{G_2 + G_x} C_1 \right) \\ & + \left(\beta \frac{G_1 G_2 G_x}{G_2 + G_x} + \frac{G_1 G_2 G_z}{G_2 + G_x} \right) = 0, \end{aligned} \quad (11)$$

where G_x and G_z represent the corresponding admittances of the parasitic resistances R_x and R_z , respectively. The modified oscillation condition and oscillation frequency are

$$\frac{G_2 G_x}{(1+k) G_1 (G_2 + G_x)} = \frac{C_1 + C_2}{C_1 - 2k C_2} \quad (12)$$

$$\omega'_o = \sqrt{\frac{G_1 G_2 G_x}{C_1 C_2 (G_2 + G_x)}} = \sqrt{\frac{G_x}{G_2 + G_x}} \omega_o. \quad (13)$$

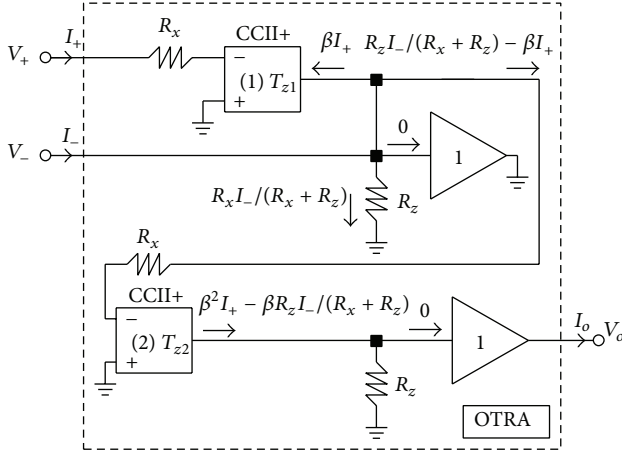


FIGURE 5: Equivalent circuit model of the OTRA (Figure 3) with nonideal and parasitic effects.

The parameter k is defined as

$$k = \frac{G_z}{\beta G_x}. \quad (14)$$

Equations (12) and (13) reveal that the nonideal current tracking error β and parasitic admittances G_x and G_z influence the oscillation condition and oscillation frequency. However, the influence of the parameter k can be ignored because the parasitic admittance G_x is much larger than G_z in magnitude. Note also that the parasitic admittance G_x slightly changes the oscillation frequency on this circuit. This slight deviation can be compensated for by selecting $G_x \gg G_z$ to minimize the influence on the circuit. Utilizing (13), the active and passive sensitivities of the circuit (Figure 4(a)) are

$$\begin{aligned} S_{G_1}^{\omega_o'} &= S_{G_2}^{\omega_o'} = -S_{C_1}^{\omega_o'} = -S_{C_2}^{\omega_o'} = \frac{1}{2}, \\ S_{G_x}^{\omega_o'} &= \frac{1}{2} \left(\frac{G_2}{G_2 + G_x} \right), \\ S_{\beta}^{\omega_o'} &= S_{G_z}^{\omega_o'} = 0. \end{aligned} \quad (15)$$

For the condition $G_x \gg G_z$, $S_{G_x}^{\omega_o'} = 0$. The circuit exhibits a good sensitivity performance because all active and passive sensitivities are less than unity in magnitude. For Figure 4(b) circuit, the modified characteristic equation is

$$\begin{aligned} &S^2 \left(\left(1 + \frac{G_z}{\beta G_x} \right) C_1 C_2 \right) \\ &+ S \left(G_1 C_1 + G_2 C_1 + G_3 C_1 - G_1 C_2 \right. \\ &\quad \left. + \frac{G_z}{\beta G_x} (2G_2 C_2 + G_1 C_1 + G_2 C_1 + G_3 C_1) \right) \\ &+ \left(G_1 G_2 + \frac{1}{\beta} \left(\frac{G_1 G_2 G_z}{G_x} + \frac{G_2 G_3 G_z}{G_x} \right) \right) = 0. \end{aligned} \quad (16)$$

The modified oscillation condition and oscillation frequency are

$$\frac{(1+k)(G_1 + G_2 + G_3)}{G_1 - 2kG_2} = \frac{C_2}{C_1} \quad (17)$$

$$\omega_o' = \sqrt{\frac{G_2(G_1 + (kG_3/(1+k)))}{C_1 C_2}} = \omega_o + \sqrt{\left(\frac{k}{1+k} \right) \frac{G_2 G_3}{C_1 C_2}}. \quad (18)$$

Equations (17) and (18) show that the parameter k slightly changes the oscillation condition and oscillation frequency, respectively. Again, this slight deviation can be overlooked because the parameter k represents a very small value on the proposed circuits. The active and passive sensitivities for this circuit are determined in (19). Equation (19) shows that the active and passive sensitivities are all low because the parameter k is nearly zero:

$$\begin{aligned} S_{G_2}^{\omega_o'} &= -S_{C_1}^{\omega_o'} = -S_{C_2}^{\omega_o'} = \frac{1}{2}, \\ S_{G_z}^{\omega_o'} &= -S_{\beta}^{\omega_o'} = \frac{1}{2} \left(\frac{kG_3}{(1+k)^2 G_1 + k(1+k)G_3} \right), \\ S_{G_x}^{\omega_o'} &= -\frac{1}{2} \left(\frac{kG_3/(1+k)}{(1+k)G_1 + kG_3} \right), \\ S_{G_1}^{\omega_o'} &= \frac{1}{2} \left(\frac{1+k}{k(1+G_3) + 1} \right), \\ S_{G_3}^{\omega_o'} &= \frac{1}{2} \left(\frac{kG_3}{(1+k)G_1 + kG_3} \right). \end{aligned} \quad (19)$$

The circuit depicted in Figure 4(c) has the following modified characteristic equation:

$$\begin{aligned} &S^2 \left(\left(1 + \frac{G_z}{\beta G_x} \right) (C_2 + C_3) C_1 \right) \\ &+ S \left(G_1 C_1 + G_2 C_1 - G_1 C_2 \right. \\ &\quad \left. + \frac{G_z}{\beta G_x} (G_2 C_3 + 2G_2 C_2 + G_1 C_1 + G_2 C_1) \right) \\ &+ \left(G_1 G_2 - \frac{1}{\beta} \frac{G_1 G_2 G_z}{G_x} \right) = 0. \end{aligned} \quad (20)$$

The modified oscillation condition and oscillation frequency are

$$(1+k) \left(1 + \frac{G_2}{G_1} \right) + \frac{kG_2 C_3}{G_1 C_1} = \frac{C_2}{C_1}, \quad (21)$$

$$\omega_o' = \sqrt{\frac{(1-k)G_1 G_2}{(1+k)C_1(C_2 + C_3)}} = \sqrt{\frac{1-k}{1+k}} \omega_o. \quad (22)$$

Equations (21) and (22) show that the parameter k affects the oscillation condition and oscillation frequency,

respectively. However, the influence of the nonideal effect can be nearly disregarded because the parameter k is a very small value that ideally approaches zero. The active and passive sensitivities of the circuit are

$$\begin{aligned} S_{G_1}^{\omega_o'} &= S_{G_2}^{\omega_o'} = -S_{C_1}^{\omega_o'} = \frac{1}{2}, \\ S_{G_x}^{\omega_o'} &= -S_{G_z}^{\omega_o'} = S_{\beta}^{\omega_o'} = \frac{G_z}{1 - k^2}, \\ S_{C_2}^{\omega_o'} &= -\frac{1}{2} \left(\frac{C_2}{C_2 + C_3} \right), \\ S_{C_3}^{\omega_o'} &= -\frac{1}{2} \left(\frac{C_3}{C_2 + C_3} \right). \end{aligned} \quad (23)$$

Equation (23) shows that when $C_3 > C_2$ is set, the values of $S_{C_2}^{\omega_o'}$ and $S_{C_3}^{\omega_o'}$ do not exceed 50%. In addition, $S_{G_x}^{\omega_o'}$, $S_{G_z}^{\omega_o'}$, and $S_{\beta}^{\omega_o'}$ approach zero because the admittance G_z is a very small value ($G_z = 0$, in ideal case). Thus, the active and passive sensitivities are all low. Thus, to eliminate the nonideality effects and reduce the influence of sensitivity on the proposed circuits, the following conditions should be met: $G_x \gg G_z$, $G_x \gg G_2$, and $C_3 > C_2$. In considering the integration aspects, the proposed oscillator circuits with the top plate and bottom plate parasitic capacitances of C_1 and C_2 may render to alter the order of the oscillator circuits and change its oscillation frequency. To reduce the influences of the top plate and bottom plate parasitic capacitances of C_1 and C_2 on the proposed oscillators, an advanced layout technology can be applied to overcome this obstacle [31]. Table 2 summarizes the key equations for the proposed oscillators.

The frequency stability is an important performance criterion for sinusoidal oscillators [1]. The frequency stability factor S_F is defined as

$$S_F = \left. \frac{d\Phi(\mu)}{d\mu} \right|_{\mu=1}, \quad (24)$$

where $\mu = \omega/\omega_0$ and $\Phi(\mu)$ represents the phase function of the open loop transfer function for the oscillator circuit. Using the definition expressed in (24), Table 2 gives the frequency stability factor for the proposed oscillators. This table shows that good frequency stability can be obtained by choosing a larger value of n for the proposed circuits.

4. Simulation and Experimental Results

To verify the feasibility of the proposed circuits, commercial AD844AN ICs were adopted to implement an OTRA (Figure 3) to execute the experimental tests. All experiments were performed at a supply voltage of ± 5 V. The proposed circuits were also simulated with circuit simulation program HSPICE using the CMOS OTRA implementation as shown in Figure 2. Feasible design procedures of the oscillation condition and the oscillation frequency for the proposed oscillators (Figure 4) were arranged as follows. For Figure 4(a) circuit, $C_1 = C_2$ was first assigned and an oscillation frequency was

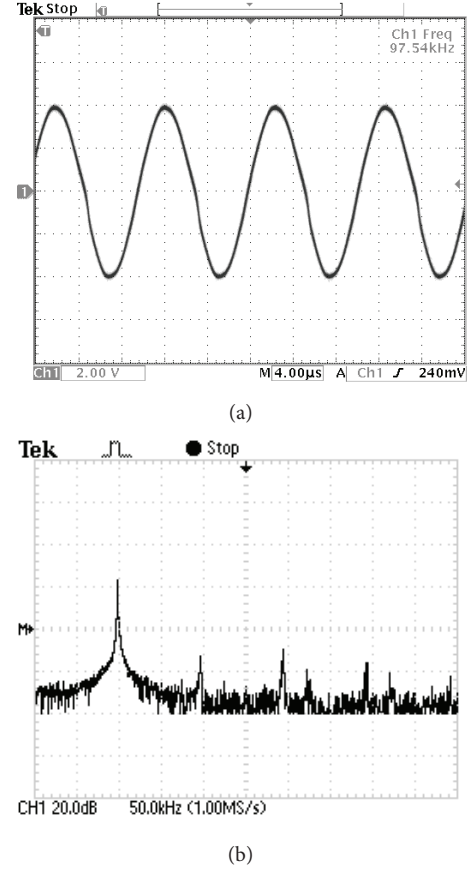


FIGURE 6: Experimental results for the circuit (Figure 4(a)): (a) output waveform and (b) corresponding frequency spectrum.

specified. Therefore, the values R_1 and R_2 can be determined using (4). For the Figure 4(b) circuit, $R_1 = R_2$ and $C_2 = nC_1$ were chosen. From (6) and (7), R_3 can be determined when an oscillation frequency was assigned. For the final oscillator (Figure 4(c)), $C_2 = 3C_1$ was first assigned and thus the ratio of R_1/R_2 was decided from (9). Subsequently, the value of C_3 can be determined from (10) when an oscillation frequency was specified. For example, the oscillator in Figure 4(a) was designed with $R_1 = 2.43$ k Ω , $R_2 = 1.1$ k Ω , and $C_1 = C_2 = 1$ nF. Together with the nonideal parameters $\beta = 0.98$, $R_x = 50$ Ω , and $R_z = 3$ M Ω , this resulted in 94.98 kHz theoretical oscillation frequency. The experimental results in Figure 6(a) show an oscillation frequency of 97.54 kHz, which is close to the theoretical prediction. The percentage error between theoretical and experimental result is 2.62%. Figure 6(b) displays the corresponding frequency spectrum. The percentage total harmonic distortion (THD) was measured as 2.52%. The experimental result shows the slight distortion on this circuit because Figure 4(a) circuit suggests a compact circuit topology with minimum RC design [9, 27, 28]. However, an additional auxiliary amplitude control circuit and technology can be used to yield a lower distortion of the generated output signal through external means [32]. The oscillator of Figure 4(b) was designed with $R_1 = R_2 = 10.83$ k Ω ,

TABLE 2: Key equations for the proposed oscillators.

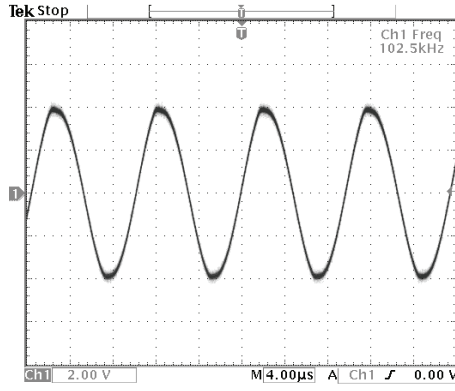
Configuration	Oscillation condition and frequency	Active and passive sensitivities	Frequency stability factor
Figure 4(a)	Ideal:		
	$\frac{G_2}{G_1} - 1 = \frac{C_2}{C_1}$		
	$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}}$	$S_{G_1}^{\omega_o} = S_{G_2}^{\omega_o} = -S_{C_1}^{\omega_o} = -S_{C_2}^{\omega_o} = \frac{1}{2}$	\sqrt{n}
	Nonideal:		
	$\frac{G_2 G_x}{(1+k)G_1(G_2+G_x)} = \frac{C_1+C_2}{C_1-2kC_2}$	$S_{G_x}^{\omega_o} = \frac{1}{2} \left(\frac{G_2}{G_2+G_x} \right)$	For conditions: $C_1 = C_2 = C$ $G_1 = G$ and $G_2 = nG$
	$\omega_o' = \sqrt{\frac{G_1 G_2 G_x}{C_1 C_2 (G_2+G_x)}}$	$S_{\beta}^{\omega_o} = S_{G_z}^{\omega_o} = 0$	
Figure 4(b)	Ideal:		
	$1 + \frac{G_2}{G_1} + \frac{G_3}{G_1} = \frac{C_2}{C_1}$	$S_{G_2}^{\omega_o} = -S_{C_1}^{\omega_o} = -S_{C_2}^{\omega_o} = \frac{1}{2}$	
	$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}}$	$S_{G_z}^{\omega_o} = -S_{\beta}^{\omega_o} = \frac{1}{2} \left(\frac{kG_3}{(1+k)^2 G_1 + k(1+k)G_3} \right)$	$\frac{2\sqrt{2}n}{2n+1}$
	Nonideal:		
	$\frac{(1+k)(G_1+G_2+G_3)}{G_1-2kG_2} = \frac{C_2}{C_1}$	$S_{G_x}^{\omega_o} = -\frac{1}{2} \left(\frac{kG_3/(1+k)}{(1+k)G_1+kG_3} \right)$	For conditions: $C_2 = C = 2C_1$ $G_1 = G_2 = G$ and $G_3 = \frac{G}{n}$
	$\omega_o' = \sqrt{\frac{G_2(G_1+(kG_3/(1+k)))}{C_1 C_2}}$	$S_{G_1}^{\omega_o} = \frac{1}{2} \left(\frac{1+k}{k(1+G_3)+1} \right)$	
		$S_{G_3}^{\omega_o} = \frac{1}{2} \left(\frac{kG_3}{(1+k)G_1+kG_3} \right)$	
Figure 4(c)	Ideal:		
	$1 + \frac{G_2}{G_1} = \frac{C_2}{C_1}$	$S_{G_1}^{\omega_o} = S_{G_2}^{\omega_o} = -S_{C_1}^{\omega_o} = \frac{1}{2}$	
	$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 (C_2+C_3)}}$	$S_{G_x}^{\omega_o} = -S_{G_z}^{\omega_o} = S_{\beta}^{\omega_o} = \frac{G_z}{1-k^2}$	$\sqrt{\frac{8(1+n)}{3}}$
	Nonideal:		
	$(1+k) \left(1 + \frac{G_2}{G_1} \right) + \frac{kG_2 C_3}{G_1 C_1} = \frac{C_2}{C_1}$	$S_{C_2}^{\omega_o} = -\frac{1}{2} \left(\frac{C_2}{C_2+C_3} \right)$	For conditions: $C_2 = C = 3C_1$ $C_3 = nC_2 = nC$ $G_1 = G = \frac{G_2}{2}$
	$\omega_o' = \sqrt{\frac{(1-k)G_1 G_2}{(1+k)C_1 (C_2+C_3)}}$	$S_{C_3}^{\omega_o} = -\frac{1}{2} \left(\frac{C_3}{C_2+C_3} \right)$	

$R_3 = 29.6 \text{ k}\Omega$, and $C_1 = 0.1 \text{ nF}$, $C_2 = 0.2 \text{ nF}$ together with the nonideal parameters $\beta = 0.98$, $R_x = 50 \Omega$, and $R_z = 3 \text{ M}\Omega$. Figure 7 shows the experimental results of the output waveform and the corresponding frequency spectrum. In this case, the theoretical value of the oscillation frequency is 104.16 kHz , whereas experimental results (Figure 7(a)) reveal an oscillation frequency of 102.5 kHz . The percentage error between theoretical and experimental result is 1.59% . The percentage THD was measured as 2.64% .

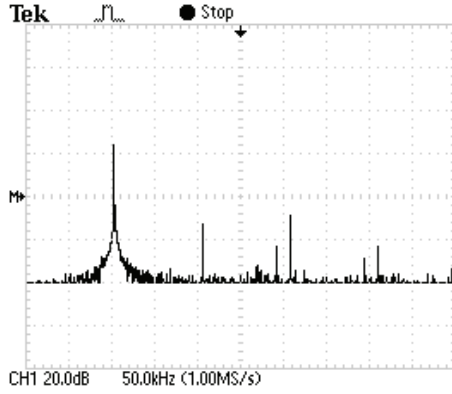
The oscillator in Figure 4(c) was designed with $R_1 = 2 \text{ k}\Omega$, $R_2 = 1 \text{ k}\Omega$, and $C_1 = 0.1 \text{ nF}$, $C_2 = 0.3 \text{ nF}$, $C_3 = 12.4 \text{ nF}$. The theoretical value of the oscillation frequency was determined as 99.85 kHz . The experimental results

in Figure 8(a) reveal an oscillation frequency of 101.3 kHz . The percentage error between theoretical and experimental result is 1.43% . Figure 8(b) indicates that the corresponding frequency spectrum and the percentage THD was measured as 2.98% .

Considering the achievements in CMOS technology, Figure 2 presents an alternative implementation of OTRA for simulation testing. For this purpose, all of the proposed circuits in Figure 4 were simulated using the HSPICE program based on the CMOS OTRA (Figure 2). All simulations were performed by TSMC $0.35 \mu\text{m}$ MOS transistor parameters with the same aspect ratios as those in [15]. The CMOS OTRA (Figure 2) was biased with a power supply of $\pm 2.5 \text{ V}$. The bias



(a)

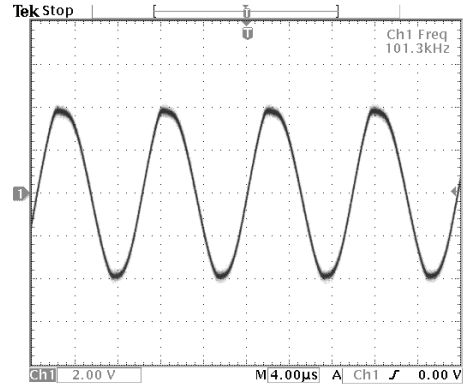


(b)

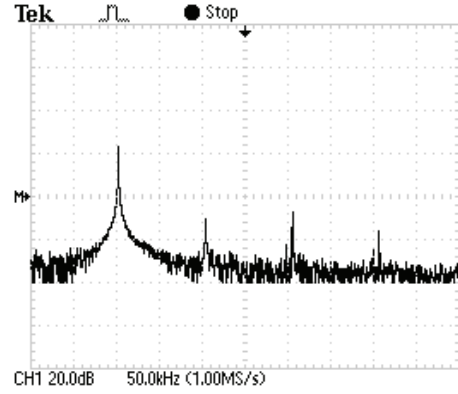
FIGURE 7: Experimental results for the circuit (Figure 4(b)): (a) output waveform and (b) corresponding frequency spectrum.

current and voltages $I_B = 30 \mu\text{A}$, $V_{g1} = -1 \text{ V}$, and $V_{g2} = 1 \text{ V}$ were set. Figure 9(a) shows the simulation results of the output waveform for Figure 4(a) with $R_1 = 21.3 \text{ k}\Omega$, $R_2 = 9.85 \text{ k}\Omega$, $C_1 = 0.1 \text{ nF}$ and $C_2 = 0.1 \text{ nF}$, where R_1 was designed to be larger than R_2 to achieve good frequency stability. Simulation results indicate that the oscillation frequency is 108.48 kHz (theoretical value is 109.87 kHz), yielding a percentage error of only 1.26% between the theoretical and simulation oscillation frequency results. These slight deviations in the oscillation frequency of the circuit from theoretical values were caused by the nonideality of the CMOS OTRA. Figure 9(b) shows that the simulation result of the frequency spectrum and the percentage THD was analyzed as 2.59% . The circuit in Figure 4(b) was simulated with the following values: $R_1 = 12 \text{ k}\Omega$, $R_2 = 12 \text{ k}\Omega$, $R_3 = 12 \text{ k}\Omega$, $C_1 = 0.05 \text{ nF}$, and $C_2 = 0.16 \text{ nF}$. Under these design values, the theoretical value of the oscillation frequency was calculated as 148.28 kHz . Figure 10 shows the simulation results of the output waveform and its output frequency spectrum. Figure 10(a) shows that the oscillation frequency of the output waveform is 150.01 kHz . Figure 10(b) shows that the percentage THD was analyzed as 2.71% , yielding a 1.15% percentage error between theoretical and simulation result of the oscillation frequency.

For the circuit in Figure 4(c), the passive components were chosen as $R_1 = 20 \text{ k}\Omega$, $R_2 = 9 \text{ k}\Omega$, $C_1 = 0.05 \text{ nF}$,



(a)



(b)

FIGURE 8: Experimental results for the circuit (Figure 4(c)): (a) output waveform and (b) corresponding frequency spectrum.

$C_2 = 0.15 \text{ nF}$, and $C_3 = 0.1 \text{ nF}$. This design yields a theoretical oscillator frequency of 106.1 kHz . Figure 11(a) shows the output waveform view obtained from HSPICE simulation for the chosen example. Simulation results show an oscillation frequency of 105.08 kHz , which is close to the theoretical prediction. The percentage error of the oscillation frequency between theoretical and simulation result is 0.96% . Figure 11(b) displays the corresponding output frequency spectrum, with the percentage THD analyzed as 0.56% . Once again, these results verify that the HSPICE simulations are in good agreement with the theoretical analysis. Simulation results show that the CMOS OTRA-based solutions provide the better output waveforms with low signal distortion. With regard to the highest applicable operating frequency of the proposed circuit (Figure 4(c)), an experimental test with values $R_1 = 15 \text{ k}\Omega$, $R_2 = 7.5 \text{ k}\Omega$, $C_1 = 0.03 \text{ nF}$, $C_2 = 0.1 \text{ nF}$, and $C_3 = 0.01 \text{ nF}$ was executed to explore this characteristic. Figure 12 shows the simulation result for the output waveform of the circuit (Figure 4(c)) with an oscillation frequency of 260.35 kHz , which is close to the theoretical value of 261.21 kHz . The highest applicable operating frequency of the proposed oscillator was only demonstrated at approximated several hundreds of kHz based on the CMOS OTRA circuit (Figure 2). In this case, the percentage error between theoretical and experimental result is 0.79% . To demonstrate the properties used to control oscillation

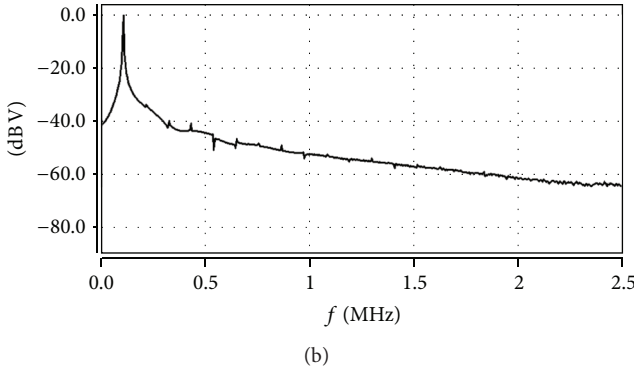
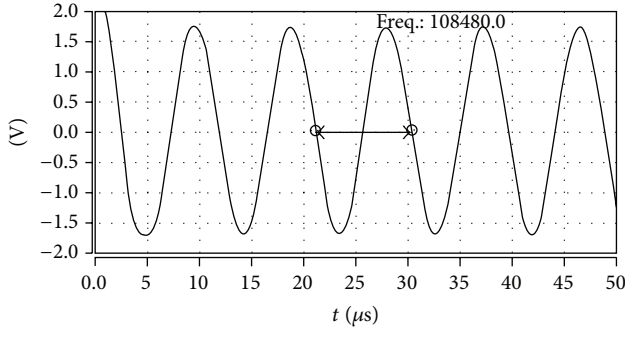


FIGURE 9: Simulation results for the circuit (Figure 4(a)) using CMOS OTRA (Figure 2): (a) output waveform and (b) corresponding frequency spectrum.

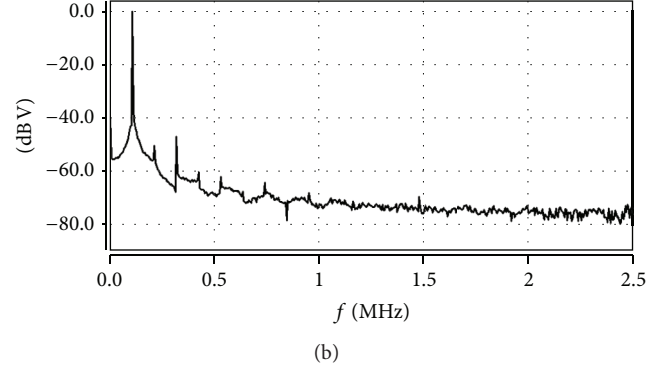
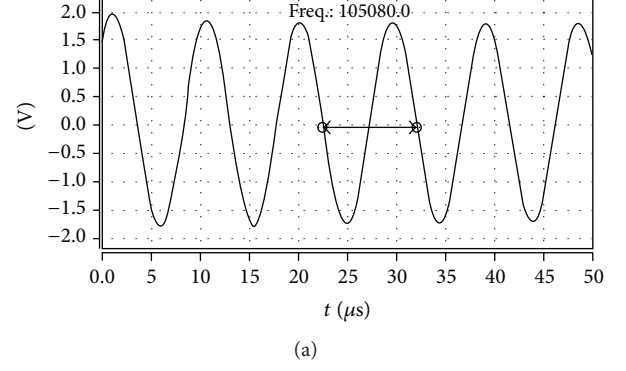


FIGURE 11: Simulation results for the circuit (Figure 4(c)) using CMOS OTRA (Figure 2): (a) output waveform and (b) corresponding frequency spectrum.

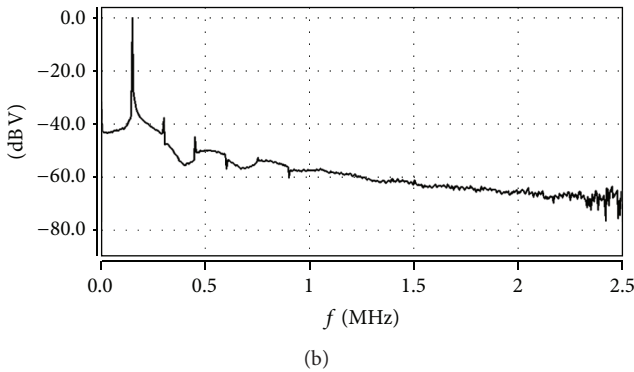
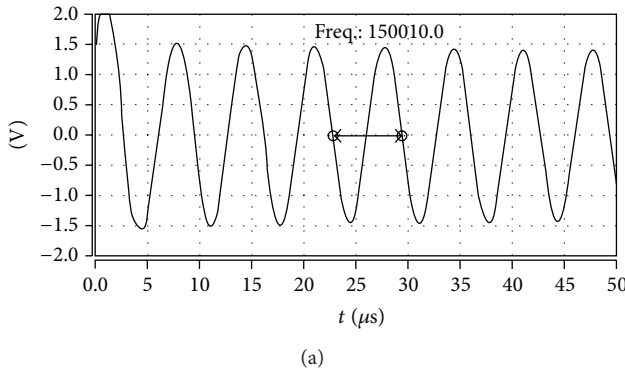


FIGURE 10: Simulation results for the circuit (Figure 4(b)) using CMOS OTRA (Figure 2): (a) output waveform and (b) corresponding frequency spectrum.

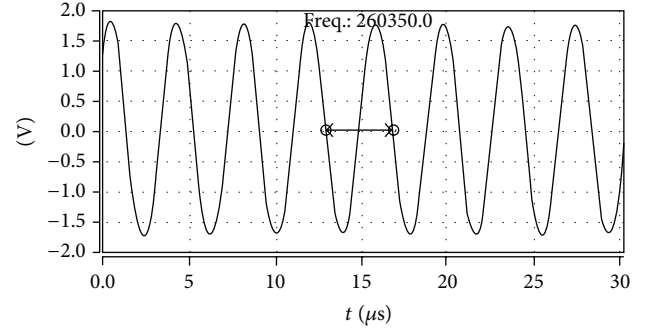


FIGURE 12: Simulation result of the highest applicable oscillation of the circuit (Figure 4(c)).

frequency by using resistors, Figure 4(b) circuit is employed to investigate such phenomenon. By adopting $C_1 = 0.05$ nF and $C_2 = 0.16$ nF, $R_1=R_2=R_3 = R$ was assigned and varied from 10 kΩ to 20 kΩ in 1 kΩ steps. Figure 13 shows the theoretical and simulation results for the variation of the oscillation frequency. The experimental results correspond with the theoretical prediction. Experimental tests suggest that the proposed oscillators can be implemented using commercially available AD844AN ICs or CMOS technology.

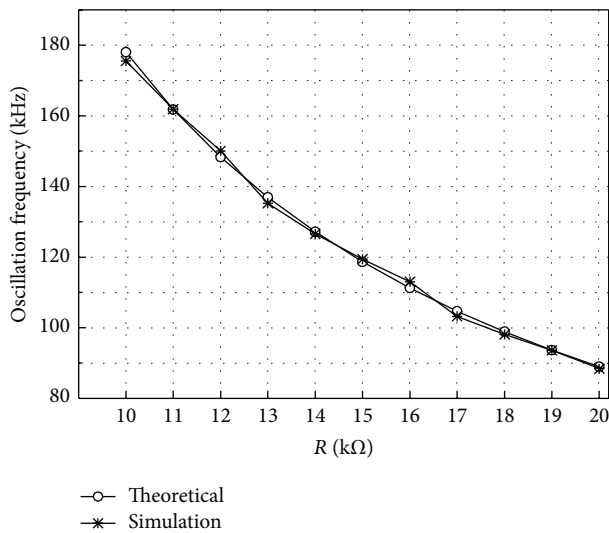


FIGURE 13: Variation of the oscillation frequency against R for the circuit (Figure 4(b)).

5. Conclusions

This study reports three new sinusoidal oscillators that have not been seen in the open literature. Each circuit consists of a single OTRA with a few external passive components. The first circuit features the least RC components design. The second and third circuits provide independent control of the oscillation condition and oscillation frequency, respectively. The proposed circuits also exhibit low active and passive sensitivities to oscillation frequency, and most parasitic parameters in the proposed circuits disappear due to the OTRA's internal ground input terminals. The HSPICE simulations and experiment measurements in this study verify the effectiveness of the proposed circuits. The proposed topologies provide brand-new sinusoidal oscillators for OTRA devices. Because of their simplicity, these new schemes can be expected to find wide applications in modern analog circuit systems.

Conflict of Interests

The author declares that there is no conflict of interests regarding the publication of this paper.

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