Hindawi
Active and Passive Electronic Components
Volume 2017, Article ID 1650161, 6 pages
https://doi.org/10.1155/2017/1650161

Research Article

A Self-Biased Active Voltage Doubler for Energy Harvesting Systems

Umais Tayyab and Hussain A. Alzaher

Electrical Engineering Department, KFUPM, Dhahran 31261, Saudi Arabia

Correspondence should be addressed to Hussain A. Alzaher; alzaherh@kfupm.edu.sa

Received 21 July 2017; Revised 30 September 2017; Accepted 9 November 2017; Published 3 December 2017

Academic Editor: Yuh-Shyan Hwang

An active voltage doubler utilizing a single supply op-amp for energy harvesting system is presented. The proposed doubler is used for rectification process to achieve both acceptably high power conversion efficiency (PCE) and large rectified DC voltage. The incorporated op-amp is self-biased, meaning no external supply is needed but rather it uses part of the harvested energy for its biasing. The proposed active doubler achieves maximum power conversion efficiency (PCE) of 61.7% for a 200 Hz sinusoidal input of 0.8 V for a 20 KΩ load resistor. This efficiency is 2 times more when compared with the passive voltage doubler. The rectified DC voltage is almost 2 times more than conventional passive doubler. The relation between PCE and the load resistor is also presented. The proposed active voltage doubler is designed and simulated in LF 0.15 μm CMOS process technology using Cadence virtuoso tool.

1. Introduction

Various surrounding energy harvesting has been verified to be a feasible method of augmenting wireless system lifetimes while decreasing dependency on batteries. Relying on the surrounding stimulus, radio frequency, solar, and mechanical vibrations can be utilized as energy sources for energy harvesting [1]. Exclusion of batteries is greatly beneficial for certain applications such as embedded medical devices and wireless sensor nodes, where substitution of a battery is expensive or unrealistic [2, 3]. Energy scavenging suggests a feasible answer for these applications. Vibration energy based harvesters are very well suited for systems in some technical surroundings like buildings, cars, aircraft, and engines. There, valuable mechanical vibrations can be found in the frequency band from mHz up to some kHz [4] and transformed into electrical energy using piezoelectric (PE) generator. Piezoelectric (PE) energy scavenging systems provide fairly a high-energy density going from 10 to several hundreds μW/cm^3 [5–7]. A rectifier, which acts as interfacing circuit, is required to efficiently convert the output AC signal of PE device into a DC signal that can be utilized for operating other circuits or to store in energy for later use. The interfacing circuit is very significant as it determines amount of the extracted energy from PE devices.

Various rectifiers are proposed for PE energy harvesting system [1–10]. The full bridge passive rectifier is utilized for low frequency PE energy harvesting systems but results in poor efficiency. A huge voltage drop cannot be accepted; thus CMOS diodes or Schottky diodes must be avoided. This voltage drop can be reduced by superimposing a bias voltage onto the gate of the MOS transistor that efficiently eliminates the voltage drop associated with threshold voltage V_{th} [8]. Nevertheless, an extra supply voltage circuit is assumed to be available which is not often there. CMOS active rectifier ideas are an innovative method for low voltage drop and higher PCE. These active rectifier techniques deliver output voltages almost equal to the input voltage combined with less power consumption. The comparator based diode can be used as an active element to overcome voltage drop issue for rectifier designs [9, 10]. The rectifier switches are driven from comparator by sensing the forward voltage drop across the MOS switches. The offset of the comparator causes oscillations (the comparator output leakage in the capacitor) which degrades the PCE of the rectifier design. The solution for this problem is to replace the comparator based diode with

an op-amp based diode. These rectifiers provide DC rectified voltage often less than amplitude of the AC input voltage. Output voltage of larger amplitudes is usually required for specific low power applications, for example, digital baseband circuits in RFIDs wherein a supply voltage of a 3–5 × V_{th} is needed [11]. Voltage doubler rectifier structure can be used as it provides DC output proportional to the twofold of the approaching input signal amplitude but results in the degradation of PCE [10]. This paper focuses on the design of self-biased active voltage doubler feed by a low frequency PE transducer, as it is easily available and provides high output efficiency. A 1 μF of load capacitance is utilized to store the scavenged energy and used to bias the active element of the voltage doubler. Therefore, passive diodes may be replaced by active diodes to achieve large output voltage and enhanced the PCE.

The paper is arranged as follows. Review of PCE calculations is given in Section 2. The operation of a conventional voltage doubler circuit is discussed in Section 3. The design of the proposed self-biased active voltage doubler is presented in Section 4. The adopted op-amp design is presented in Section 5. Simulation results obtained using CMOS 0.15 μm technology in Cadence are provided in Section 6.

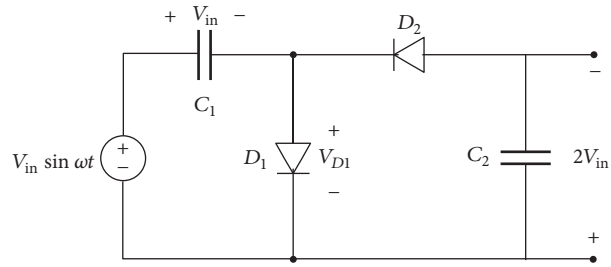

Figure 1: Traditional voltage doubler.

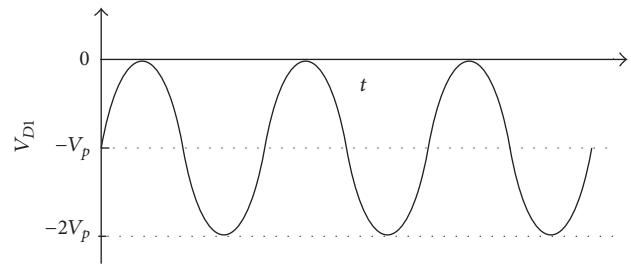

Figure 2: Voltage waveform across D_1.

2. Power Conversion Efficiency

Power originating from vibration energy source may be unregulated, alternating, and/or small. Therefore, in such situations it becomes dominant to enhance the PCE of the rectifier. As the output of the precision rectifier can be the input of the next stage or to power another active element, larger PCE is desired so that next stage gives more DC output voltage with feasible efficiency for its proper operation. If the PCE of the first stage is bad, then second stage is useless to be utilized for further operation.

Maximization of the PCE of the whole system mainly relies on the performance of rectifier circuit. In fact, enhancement in the PCE of the rectifier is considered as a distinctive and powerful way to upgrade the efficiency of the entire system. This is because the performance of front-end is often limited by regional regulation. For example, the maximum power transmission allowed in the Japan and US is 4 W [11].

The power conversion efficiency (PCE) of rectifier circuit is described as ratio of the output power to the input power. The input power equals the loss in the rectifier plus the output power. Thus, PCE can be expressed as

$$\text{PCE} = \frac{P_{\text{OUT}}}{P_{\text{IN}}} = \frac{P_{\text{OUT}}}{\left(P_{\text{OUT}} + P_{\text{LOSS}}\right)}. \quad (1)$$

For further elaborating on the definition, P_{LOSS} is defined as

$$P_{\text{LOSS}} = N \cdot P_{\text{DIODE}}. \quad (2)$$

P_{DIODE} is the loss in the diode and N is the total number of diode stages [10, 11]. When current flows through the diode, the resistive loss generates the diode loss and is expressed as

$$P_{\text{DIODE}} = P_{\text{FWD}} + P_{\text{REV}}. \quad (3)$$

P_{FWD} is the diode forward drop and P_{REV} is the diode reverse drop. These two are found by the diode voltage turn-on and the diode leakage reverse current. Therefore, less forward voltage drop and less reverse leakage current are needed to realize large PCE of the entire harvesting system.

3. Traditional Voltage Doubler

The conventional passive voltage doubler [12] circuit is shown in Figure 1.

The circuit is a combination of two cascaded parts: one is the clamp circuit formed by C_1 and D_1, and second is the peak rectifier circuit formed by C_2 and D_2. Diode D_1 conducts during positive half cycle storing input voltage in C_1. Assuming ideal diodes, the clamped output voltage V_{D1} is shown in Figure 2 when sinusoidal input is applied.

Diode D_2 conducts in negative half cycle which results in the negative peak of $-2V_{\text{in}}$ while positive peak is clamped to 0 V. The output of the peak detector at C_2 gives DC voltage of $-2V_{\text{in}}$. The circuit is known as voltage doubler since output voltage is double than the input voltage.

The conventional diodes are replaced by diode-connected MOS transistors as shown in Figure 3. The diode-connected NMOS transistors are attached in series and an intermediate node is linked to the input terminal via coupling capacitor C_C [11].

The effective turn-on voltage of the diode-connected MOS transistor is practically equivalent to V_{th} of the MOS transistor, which is smaller than a pn-junction diode, however for the most part larger than a Schottky diode. Thus, a rectifier using this straightforward diode-connected MOS setup achieves neither large voltage nor large PCE.

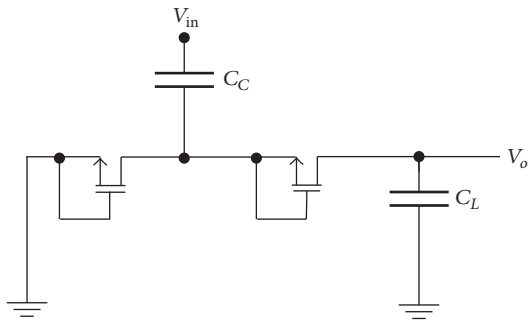

Figure 3: Simple diode-connected voltage doubler.

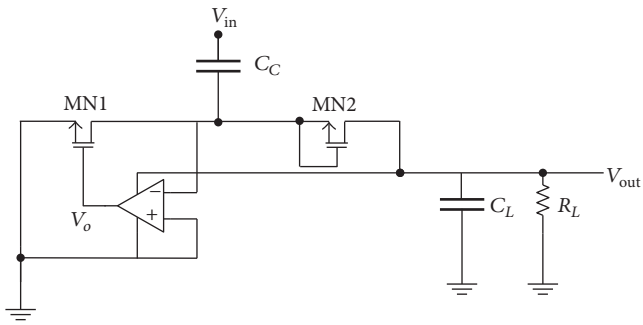

Figure 4: Proposed self-biased active voltage doubler.

4. Proposed Self-Biased Active Voltage Doubler

Different energy sources have different types of transducer. RF transducer is basically an antenna whose power is very small. It is fed to impedance matching circuit and PCB Balun to get appropriate AC voltage [13]. This voltage signal is then applied to the input of a rectifier. The matching network circuit is ignored in this study since it is beyond the scope of this paper. PE transducer consists of voltage source with cantilever capacitance used for low operating frequency.

Figure 4 shows the proposed self-biased active voltage doubler circuit. NMOS transistor MN1 is used as diode and circuit has configuration of inverting super diode with only one op-amp that is used for rectification purpose to achieve large PCE. The other NMOS transistor MN2 is connected to the load capacitance C_L and load resistor R_L forming active voltage doubler.

There is no addition DC power supply needed to bias the op-amp; instead the biasing is obtained from part of harvested energy. Therefore, the op-amp must be biased from a single positive supply. The output DC voltage V_{out} is connected to V_{DD} of the op-amp meaning the proposed doubler circuit is self-biasing the incorporated active element.

The active element will not work during the start of the process as input voltage is not large enough to supply biasing to the op-amp. The energy stored in the capacitor is small and op-amp requires feasible DC voltage to operate. So, during the startup the voltage doubler's operation is governed by body source of diode MN1. The proposed active doubler circuit can be considered as two parallel rectifier stages: passive one which only works during startup and high efficiency active one which dominates when op-amp starts working.

The working of the proposed active doubler circuit is explained as follows. In each input cycle one of the NMOS diodes is ON and other is OFF. During the startup, when the input cycle is positive, MN2 is ON storing the energy at C_L while MN1 is OFF. In the negative half cycle, MN1 conducts due to body source operation while MN2 is OFF. The energy is stored in the storage capacitance C_L during this operation and is fed back to bias the op-amp. The op-amp requires certain DC voltage to function properly. The op-amp dominates in the rectifier design when it gets enough voltage for operation. The output of the op-amp is attached to the gate of NMOS switch MN1. When the AC input is positive, the output of op-amp becomes zero as configuration is inverting and diode MN1 is cut off. The output of op-amp does not go to negative saturation level; instead it is zero as op-amp is using single supply and reduces the reverse leakage loss. The AC input voltage goes from diode MN2 to output storage capacitance C_L with some loss due to ON resistance of the diode. When the AC input is negative, the output of op-amp is increased making MN1 ON and voltage drop at MN1 is reduced while diode MN2 is cut off. The output starts to decrease slowly and becomes more when the next input positive cycle comes.

Simple diode-connected NMOS transistor MN2 is not configured as super diode. The principle of the doubler circuit is that only one of the diodes should be conducting during specific half cycle. When MN2 is setup as active diode like MN1, the two diodes MN1 and MN2 would be either ON or OFF simultaneously during specific cycle. During positive half cycle, both transistors are OFF and both are ON during negative cycle. The reason is that both the active diodes have same type of configuration and have same type of transistors. The problem occurs even if MN1 is used as passive diode and MN2 as active diode and the reason is the same that both active diodes are simultaneously ON.

5. Self-Biased OP-AMP

Some of the harvested energy is used to operate the op-amp, so its energy consumption should be as small as possible. The main hurdle in op-amp based active rectifiers is that the op-amp itself requires DC power supply. There are two drawbacks if DC power supply is used for op-amp. First, additional element and additional price have to be paid every time the circuit is utilized for certain application. Second, the addition of an external DC supply means that the system is not truly harvesting energy.

Above-mentioned drawbacks can be eliminated if the DC supply of the op-amp based rectifier comes from the harvested energy. When the DC supply of the op-amp is coming from the harvested energy, there is no need of an additional supply. It saves the price. The stored energy in the capacitor is positive voltage DC and this energy is fed back to bias the op-amp. Hence, op-amp must be single ended supply as only positive DC rectified voltage is coming from the output of the active doubler. Now, the only problem left is the power consumption of the op-amp. If the op-amp power

consumption is less than the remaining parts then the PCE of the active rectifier can be improved; otherwise there is no use for op-amp in the rectifier design.

Although the dual supply op-amp is advantageous to implement, there are many applications where single supply op-amp is required. For example, in marine and automotive equipment, battery power provides single supply. One of the main advantages of single supply op-amp is low power consumption and hence it is useful for low power applications such as biomedical implants and wireless sensor nodes. But single supply op-amp needs appropriate signal biasing; otherwise the op-amp becomes unstable or does not provide the desired output. A single supply differential pair MOS configuration [15] is adopted as shown in Figure 5.

The op-amp designed is ground compatible because of the input voltage fed from storage capacitance. The op-amp has been designed to work with the minimum possible value of the voltage supply. In this way the active voltage doubler takes over the passive one as soon as a very low energy has been stored into capacitance C_L. NMOS input differentials (M3 and M4) are used which are matched and inputs are fed into sources of these transistors. The active loads are PMOS transistors (M1 and M2). The sources of these PMOS transistors are connected together which are connected to DC power supply coming from the storage capacitance. All the transistors are in pinch-off condition and the op-amp has been carefully optimized for better performance.

For frequency response analysis in simulation, the op-amp is powered with 0.6 V DC supply and transistor widths and lengths are all set to 1 μm except for PMOS active load, and length is set to 0.3 μm. The gain and phase response of the op-amp are simulated and shown in Figure 6.

The gain of the op-amp is 41 dB and the unity gain frequency is 110 MHz. The current consumption of the op-amp is 200 nA at 0.6 V supply and it increases with the supply voltage. The DC supply used here is shown for simulation purpose. In the proposed design, the op-amp is self-biased as explained earlier.

6. Simulation Results

The simulation results are presented in this paper and compared with passive voltage doubler circuit. PE transducer is employed as an input as it is easily available and provides high output efficiency. PE transducers are one of the primary devices that can harvest energy from a button press action and produces high inputs at low frequency [14]. The transducer for simulation purpose is implemented by an AC voltage source since the transducer output is an alternating electrical signal. The simulation results demonstrated in this section are carried out using Cadence Virtuoso Simulator with LF 0.15 μm CMOS process technology. The op-amp transistor widths and lengths are all set to 1 μm except for PMOS length, and it is set at 0.3 μm. The active voltage doubler circuit is operating at 200 Hz with 0.8 V input supply. The storage capacitor C_L is set to 1 μF and R_L = 20 KΩ. The NMOS transistor ratios are set to 18 μ/0.15 μ. The threshold voltages NMOS and PMOS are 0.5 V and −0.56 V in the adopted LF 0.15 μm CMOS process technology.

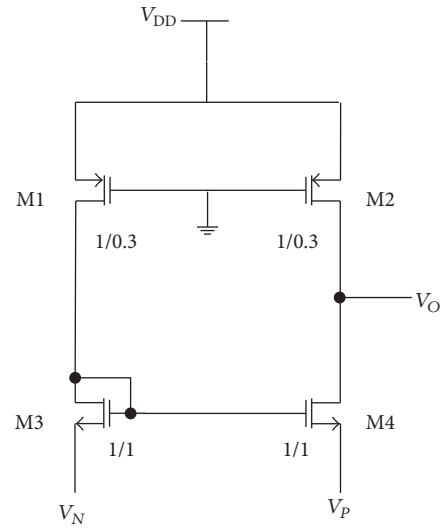

Figure 5: Single supply op-amp.

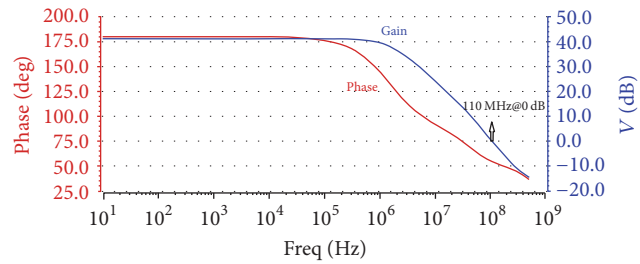

Figure 6: Simulated frequency response of differential amplifier.

6.1. Transient Response. Figure 7 shows the internal voltage waveforms of self-biased active voltage doubler at steady state. The output voltage of 0.98 V from V_{in} = 0.8 V. The self-biased active voltage doubler achieves power conversion efficiency (PCE) of 61.7% at R_L = 20 KΩ. This efficiency is 2 times more when compared with the passive voltage doubler. The conventional voltage doubler circuit gives PCE of 30% at R_L = 20 KΩ with rectified output voltage of 0.48 V. The PCE of the active doubler design depends upon loading condition as will be explained later in the paper.

6.2. Operating Voltage. The output voltage graph with respect to input voltage is simulated and shown in Figure 8. Below 0.5 V input voltage, the output voltages are negligible, that is, less than 0.1 V, and also have less PCE. The output voltage starts to increase after 0.5 V resulting in higher PCE since the active rectifier starts to operate. At 0.6 V input voltage, the output voltage is 0.66 V with PCE of 57% and it increases twice by every 0.1 V input voltage since the active rectifier starts working. At 0.8 V the output voltage is 0.98 V and is increasing smoothly for higher inputs. The output voltage is compared with conventional voltage doubler circuit and gives output voltage of 0.2 V with PCE of 17% at 0.6 V input voltage. In fact, output voltages of active voltage doubler circuit are more than the traditional passive voltage doubler for all input range.

Table 1: Comparison with several available active rectifiers.

Reference	[3]	[7]	[14]	This Work
Year	2012	2015	2013	2017
Technology	0.18 μm	0.18 μm	0.35 μm	0.15 μm
Topology	Op-amp based active rectifier	Self-Powered Rectifier	Series SSHI	Self-Biased Doubler
Input voltage	2.8 V	3 V	3.7 V	0.8 V
Operating frequency	200 Hz	200 Hz	200 Hz	200 Hz
Output voltage	2.78 V	2.9 V	3.63 V	0.98 V
Area	0.24 mm^2	0.016 mm^2	0.016 mm^2	0.001 mm^2
PCE	90%	91.2%	90%	61.7%
Inductor	No	No	Yes	No
Load	R_L = 95 kΩ C_L = 1 μF	R_L = 100 kΩ	R_L = 160 kΩ	R_L = 20 KΩ C_L = 1 μF

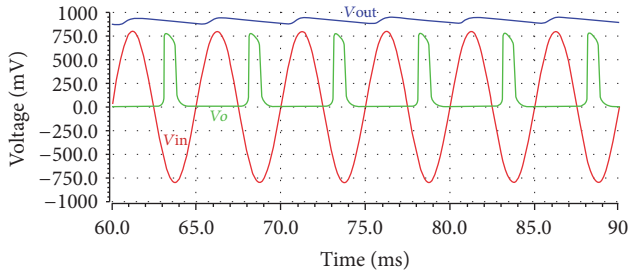

Figure 7: Simulated voltage waveforms when V_{in} = 0.8 V.

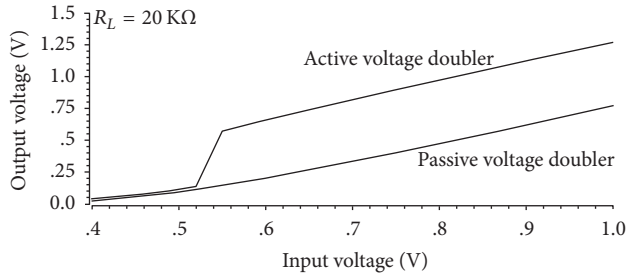

Figure 8: Simulated output voltage with respect to input voltage.

6.3. PCE Dependence on Load. The PCE of the active voltage doubler depends upon the output loading condition (different output loads) and its simulation is demonstrated in Figure 9. The input amplitude is 0.8 V. The proposed active doubler achieves maximum PCE of 61.7% at R_L = 20 kΩ and it extracts power of 39.36 μW. This means input power is around 64 μW (−11.94 dBm). The PCE decreases with the load resistor due to the phenomenon of maximum power transfer. When the rectifier input impedance equals the output impedance, maximum power is transferred to the load which leads to the high efficiency of the rectifier at that particular point. When there is variation in input and output impedance then PCE varies. The PCE of the conventional active doubler employing diode-connected MOS transistors (Figure 3) is 30% at 20 kΩ and it extracts 10.4 μW of power. Clearly, the proposed self-biased active doubler is always better than the conventional passive voltage doubler for all loads.

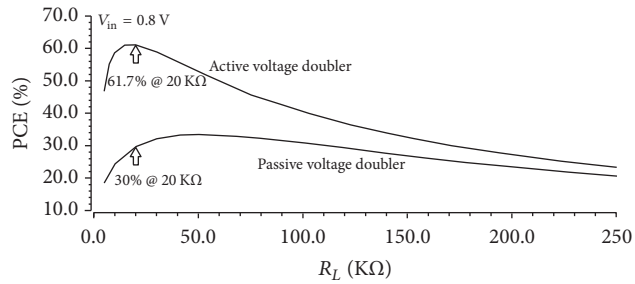

Figure 9: PCE as a function of load resistor (R_L).

The proposed design is compared with its counterparts of [3, 7, 14] as can be seen in Table 1. Other solutions give high efficiency around 90% but these designs are built for higher input voltages around 3 V and provide lower DC outputs than the input signal amplitudes. The proposed self-biased doubler gives 61.7% power efficiency but at small input voltage of 0.8 V and with enhanced rectified output voltage of 0.98 V. So, the proposed self-biased doubler can be used for low power applications that require low inputs.

7. Conclusion

The proposed self-biased active voltage doubler is suited for low power energy harvesting system applications. The active doubler starts to operate 0.5 V input and achieves larger PCE at high inputs. The proposed rectifier achieves power conversion efficiency (PCE) of 61.7% under the condition of 200 Hz operating frequency, 0.8 V input signal for 20 kΩ load resistor. The PCE is 2 times more when compared with the passive voltage doubler. The self-biased active voltage doubler circuit would be used in biomedical devices and wireless sensor nodes for direct powering or to charge a rechargeable battery. This work can be extended to multistage rectifier circuit design that provides larger DC output voltages to power remote devices while maintaining acceptable PCE.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

The authors would like to acknowledge the support of KAUST-KFUPM Initiative (KKI) program, Project no. OSR-2016-KKI-2880.

References

[1] M. Ouda, W. Khalil, and K. Salama, "Self-biased differential rectifier with enhanced dynamic range for wireless powering," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. PP, no. 99, 2016.

[2] H. Xu and M. Ortmanns, "A temperature and process compensated ultralow-voltage rectifier in standard threshold cmos for energy-harvesting applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 12, pp. 812–816, 2011.

[3] Y. Sun, N. H. Hieu, C.-J. Jeong, and S.-G. Lee, "An integrated high-performance active rectifier for piezoelectric vibration energy harvesting systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 623–627, 2012.

[4] C. Williams and R. Yates, "Analysis Of A Micro-electric Generator For Microsystems," in *Proceedings of the International Solid-State Sensors and Actuators Conference - TRANSDUCERS '95*, pp. 369–372, Stockholm, Sweden.

[5] X. D. Do, Y. H. Ko, H. H. Nguyen, H. B. Le, and S. G. Lee, "An efficient parallel SSHI rectifier for piezoelectric energy scavenging systems," in *Proceedings of the IEEE Int. Conf. Adv. Commun*, pp. 1394–1397, 2011.

[6] Y. K. Ramadass and A. P. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 1, pp. 189–204, 2010.

[7] X.-D. Do, H.-H. Nguyen, S.-K. Han, D. S. Ha, and S.-G. Lee, "A self-powered high-efficiency rectifier with automatic resetting of transducer capacitance in piezoelectric energy harvesting systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 3, pp. 444–453, 2015.

[8] S. Guo and H. Lee, "An efficiency-enhanced CMOS rectifier with unbalanced-biased comparators for transcutaneous-powered high-current implants," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 6, pp. 1796–1804, 2009.

[9] Y. Sun, I. Y. Lee, C. J. Jeong, S. K. Han, and S. G. Lee, "An comparator based active rectifier for vibration energy harvesting systems," in *Proceedings of the IEEE Int. Conf. Adv. Commun. Technol*, pp. 1404–1408, 2011.

[10] T. T. Le, J. Han, A. Von Jouanne, K. Mayaram, and T. S. Fiez, "Piezoelectric micro-power generation interface circuits," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 6, pp. 1411–1419, 2006.

[11] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, pp. 3011–3018, 2009.

[12] Adel S. S. and Kenneth C. S., *Microelectronic Circuits*, Oxford University Press, 6th edition, 2009.

[13] S. Scorcioni, L. Larcher, and A. Bertacchini, "A reconfigurable differential CMOS RF energy scavenger with 60% peak efficiency and -21 dBm sensitivity," *IEEE Microwave and Wireless Components Letters*, vol. 23, no. 3, pp. 155–157, 2013.

[14] X.-D. Do, H.-H. Nguyen, S.-K. Han, and S.-G. Lee, "A rectifier for piezoelectric energy harvesting system with series Synchronized Switch Harvesting Inductor," in *Proceedings of the 2013 9th IEEE Asian Solid-State Circuits Conference, A-SSCC 2013*, pp. 269–272, Singapore, November 2013.

[15] E. Dallago, D. Miatton, G. Venchi et al., "Active self supplied AC-DC converter for piezoelectric energy scavenging systems with supply independent bias," in *Proceedings of the 2008 IEEE International Symposium on Circuits and Systems, ISCAS 2008*, pp. 1448–1451, USA, May 2008.