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Research Article

Low-Power CMOS Integrated Hall Switch Sensor

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This paper presents an integrated Hall switch sensor based on SMIC 0.18 μm CMOS technology. The system includes a front-end Hall element and a back-end signal processing circuit. By optimizing the structure of the Hall element and using the orthogonal coupling and spinning current technology, the offset voltage can be suppressed effectively. The simulation results showed that the Hall switch can eliminate offset voltage greater than 1 mV at 3.3 V supply voltage. Two modes of the Hall switch circuit, the awake mode and the sleep mode, were realized by using clock logic signals without compromising the performance of the Hall switch, thereby reducing power consumption. The test results showed that the operate point and the release point of the switch were within the range of 3–7 mT at 3.3 V supply voltage. Meanwhile, the current consumption is 7.89 μA.

1. Introduction

In recent decades, Hall sensors have become compatible with today's semiconductor integrated circuit manufacturing technology. Integrated Hall switch sensors produced using CMOS technology feature stable performance, small size, long lifespan, and low price, which has led to their acceptance in many fields. However, Hall elements produced using CMOS technology have low sensitivity and weak Hall voltage signals. Normally, under a 1 mT weak magnetic field and 1 V bias voltage, the Hall elements only produce a Hall voltage of approximately a few tens of microvolts [1, 2]. It is therefore necessary to use the amplified circuit to amplify the Hall voltage signal for processing. Nonideal factors such as mismatched manufacturing technology, changes in working temperature, and stress caused by chip packaging can cause the Hall element and processing circuit to produce offset voltage much greater than the Hall voltage, which annihilates the effective Hall voltage signal, so measures should be taken to suppress this offset voltage [3]. Meanwhile, the internal resistance of the Hall element in working conditions is only about 1 kΩ, and the consuming current reaches the milliampere level. To develop a low-power sensor chip, measures must be taken to reduce the energy consumption of the chip.

In this study, we improved the sensitivity and reduced the offset of the Hall element by optimizing its structure. In addition, the dual-Hall element orthogonal coupling and spinning current technology was used to effectively lower the offset voltage. Circuit offset was suppressed using autozeroed technology. Clock-controlled micropower technology was used to reduce the power consumption of the low-speed Hall switch chip without compromising its performance. In Section 1, the application background of the Hall switch sensor is introduced. In Section 2, we present the CMOS part of this paper, and the application background of the Hall switch sensor is introduced. The second section presents the CMOS Hall element offset voltage and describes the technology used to suppress the Hall element offset voltage. The sensor's operating state is analyzed in Section 3. In Section 4, we discuss the analysis of the chip's test results. Section 5 contains our conclusions.

2. Design of Hall Element and Hall Offset Voltage Suppression

2.1. CMOS Hall Element. The sectional view and top view of the Hall element are shown in Figure 1. Based on a planar cross-shaped Hall element [4], a square Hall element with a 90° rotational symmetry structure was designed. Phosphorus was injected into a P-type substrate to generate an N-well that acted as the active region of the Hall element. The four corners of the square N-well were heavily doped to form N+,

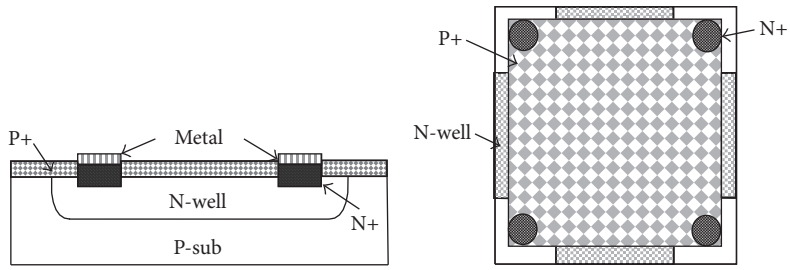

Figure 1: Cross-sectional view and top view of the Hall element.

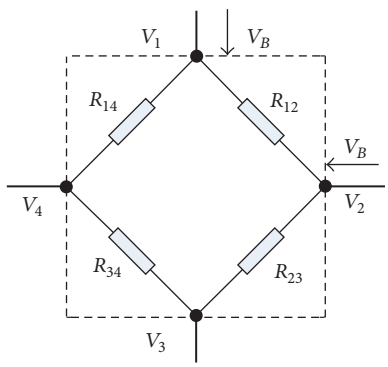

Figure 2: Hall element Wheatstone bridge model.

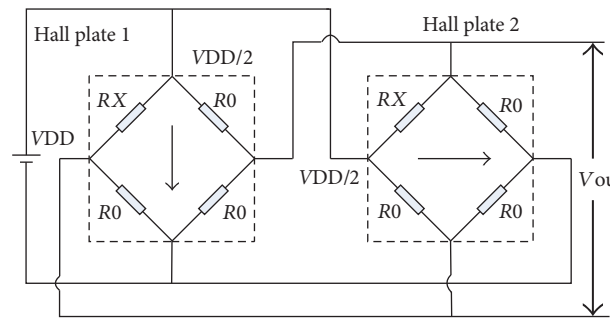

Figure 3: Orthogonal coupled Hall element.

which was connected to the metal wire as a contact electrode of the Hall element; on the surface of the Hall element, boron was used to form a P+ layer so as to reduce the effective thickness of the Hall element and increase its sensitivity, and the P+ layer was connected to the ground potential. Finally, the surface of the Hall element was covered with a layer of metal which was connected to the ground potential, and the element was surrounded by a circle of metal to reduce the interference on the Hall element caused by noise from other modules in the sensor.

2.2. Method of Suppressing the Offset Voltage of the Hall Element. In the absence of a magnetic field, due to defects in production technology, mechanical stress, and ambient temperature, when there is a source of excitation at the control end of the Hall element, there is a nonzero difference in potential at its output end (i.e., the offset voltage V_{offset} of the Hall element) [5–7]. Its Wheatstone bridge model is shown in Figure 2. When the bias current is I_{13} and I_{24}, the output voltage of the Hall element is as follows:

$$V_{13} = V_B \cdot \left(\frac{R_{14}}{R_{12} + R_{14}} - \frac{R_{34}}{R_{23} + R_{34}} \right),$$
$$V_{24} = V_B \cdot \left(\frac{R_{23}}{R_{12} + R_{23}} - \frac{R_{34}}{R_{14} + R_{34}} \right). \quad (1)$$

If resistance $R_{12} = R_{23} = R_{14} = R_{43} = R_0$, the output voltage of the Hall element is zero in the absence of a magnetic field. However, due to the mismatch between resistors, an offset voltage is generated at the output end, which is generally at the millivolt level. Assuming $R_0 = 1\,\text{k}\Omega$, 1% mismatch of R_{34}, and $R_{34} = 1.01\,\text{k}\Omega$, the offset voltage at the output end will be 8.2 mV with a 3.3 V bias voltage. When the Hall voltage sensitivity reaches 40 mV/V·T, the 8.2 mV offset voltage brings an error of 62 mT to the magnetic field, which is much greater than the magnetic signal. This can affect the performance of the Hall sensor and result in malfunction. Measures must be taken to suppress the offset voltage of the Hall element to improve the performance of the Hall sensor [8].

2.3. Orthogonal Coupling. Orthogonal coupling technology is applied to the Hall sensors as static compensation. As shown in Figure 3, two Hall elements are connected in parallel, and the two Hall elements have a 90° difference in the direction of bias voltage, so the offset voltages at the output of the two Hall elements are the same but have opposite polarity. In this case, by adding the offset voltage at the output voltage V_{OUT} of the orthogonal coupled Hall elements, the offset is suppressed:

$$V_{\text{offset 1}} = -V_{\text{offset 2}} = V_{\text{DD}} \cdot \left(\frac{R_0}{R_0 + R_0} - \frac{R_0}{R_0 + R_X} \right). \quad (2)$$

However, there is no guarantee that the other three resistors in the Wheatstone bridge model are exactly the same, which significantly reduces the effect of orthogonal coupling compensation. In order to improve the effect, large numbers of Hall elements are usually used for orthogonal coupling, such as four Hall elements, but this will increase the chip area and cost.

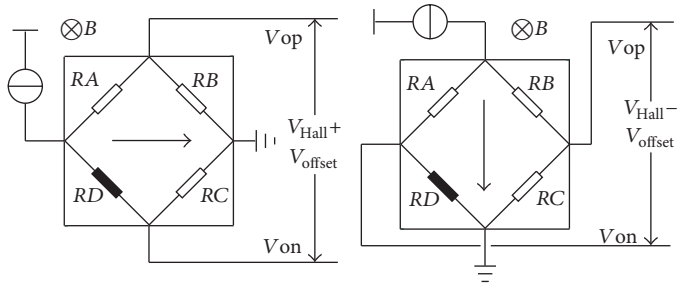

Figure 4: Spinning current technology.

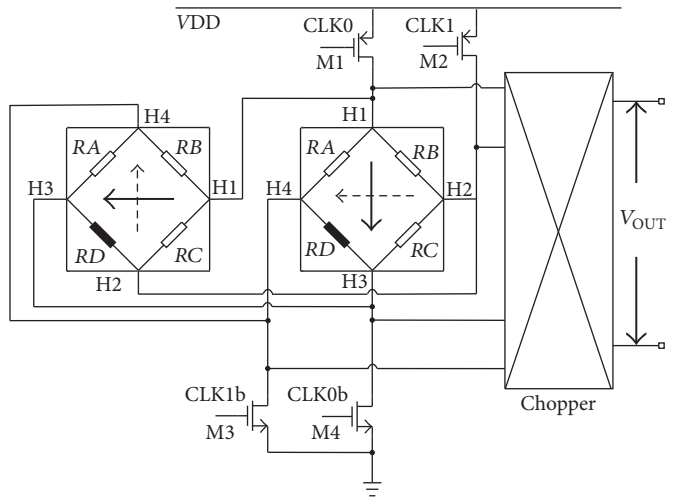

Figure 5: Orthogonal coupled spinning current circuit.

2.4. Spinning Current Technology. Orthogonal coupling technology can suppress the static offset more efficiently compared to the spinning current technology. However, the suppression of the Hall element offset by orthogonal coupling technology needs to be established on the premise that the Hall element has an orthogonally symmetrical structure, and this method is incapable of suppressing the offset caused by higher-order effects. Therefore, spinning current technology has been applied to Hall sensors to eliminate dynamic offset [9]. As shown in Figure 4, this changes the polarity of Hall voltage V_{Hall} and offset voltage V_{offset} by altering the positions of the control end and the output end of the Hall element. Through a periodic cycle, the offset voltage is modulated to spin frequency f_{spin} while the Hall voltage remains at the original frequency, and then the output voltage of the Hall element is the sum of DC Hall voltage and AC offset voltage. The offset voltage can be suppressed by subsequent circuit.

When the bias current flows from left to right, the output voltage of the Hall element is as follows:

$$V_{\Phi 1} = V_{\text{Hall}} + V_{\text{offset}}. \tag{3}$$

When the bias current rotates 90° and flows from top to bottom, the output voltage is as follows:

$$V_{\Phi 2} = V_{\text{Hall}} - V_{\text{offset}}. \tag{4}$$

The offset voltage can be suppressed by adding the output voltage in these two phases.

Combined with the orthogonal coupling technology and the spinning current technology, we can suppress the offset of the Hall element effectively and obtain a smaller residual offset [10]. A circuit structure with dual-Hall element coupling and four-phase spinning current was designed. As shown in Figure 5, CLK0 and CLK1 are a pair of nonoverlapping complementary clocks with a frequency of 50 kHz. The phases of CLK0b and CLK1b are opposite those of CLK0 and CLK1, respectively. Clock signals CLK0, CLK0b, CLK1, and CLK1b control the MOS switches M1–M4. When the clock signal CLK0 or CLK1 is low, orthogonal coupling is formed by these two Hall elements to eliminate static offset.

When CLK0 is low, M1 and M4 are switched on. H1 and H3 are the control ends, and H2 and H4 are the output ends. The output voltage is as follows:

$$V_{\text{OUT}} = V_{\text{Hall}} + V_{\text{offset}}. \tag{5}$$

When CLK1 is low, M2 and M3 are switched on. H2 and H4 are the control ends, and H1 and H3 are the output ends. The output voltage is as follows:

$$V_{\text{OUT}} = -V_{\text{Hall}} + V_{\text{offset}}. \tag{6}$$

The Hall voltage generated by the magnetic field was set to 100 μV. According to Figure 6, the maximum offset voltage

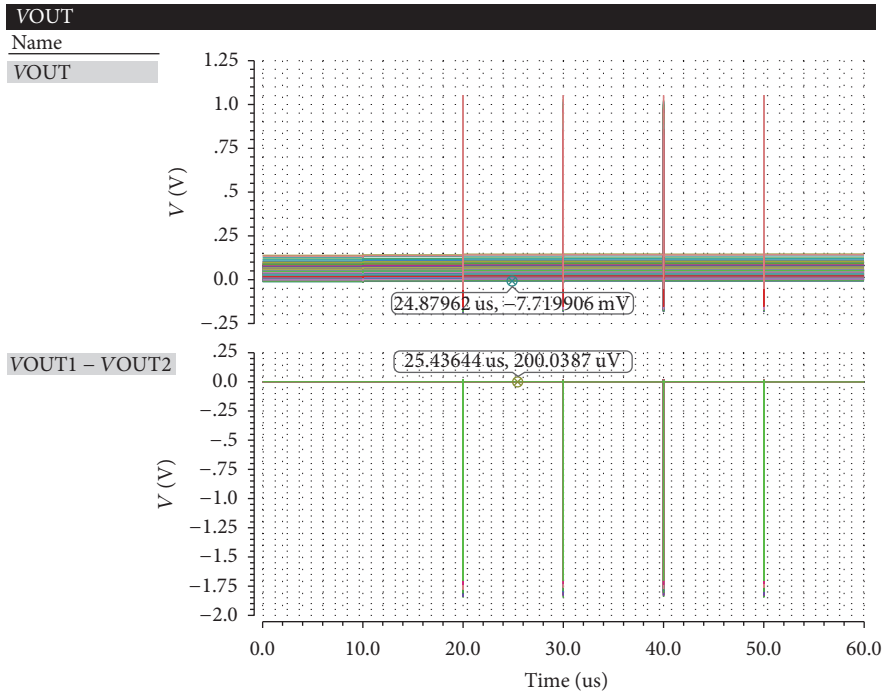

Figure 6: Simulation results of offset voltage suppression.

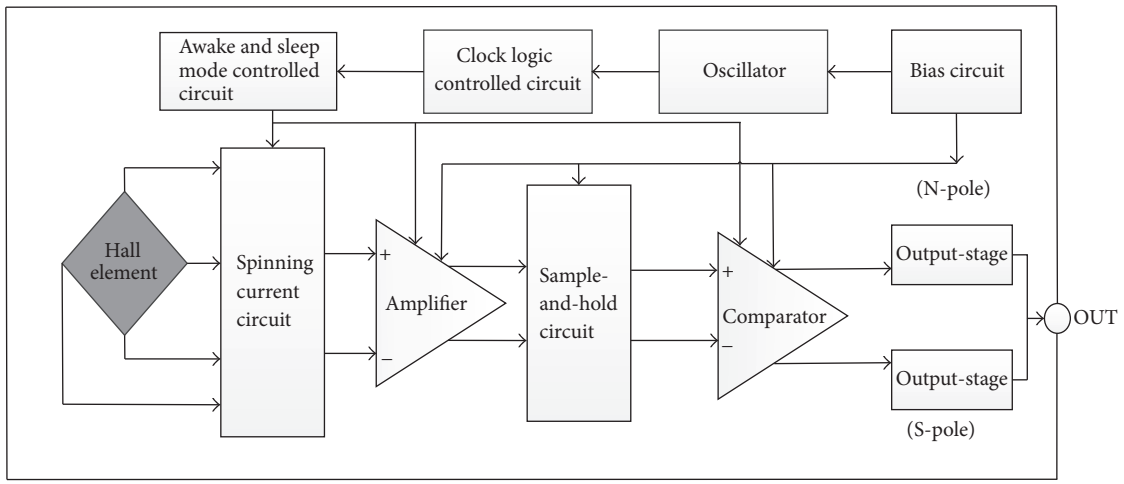

Figure 7: Circuit structure of the Hall switch sensor.

of the Hall element is greater than 7 mV. The output voltage could be obtained by using orthogonal coupled and spinning current technology and adding the output voltage in these two phases to each other, to obtain a sum of 200 μV, denoted here as $2{\cdot}V_{\text{Hall}}$.

Results show that the circuit combined with orthogonal coupled and spinning current technology can suppress the static and dynamic offset of the Hall element effectively.

3. Design of Hall Signal Processing Circuit

The circuit structure of the Hall switch sensor is shown in Figure 7. The sensor was divided into two parts: the front-end Hall element and the back-end Hall voltage signal processing circuit. The signal processing circuit was composed of a bias circuit, a spinning current circuit, a clock logic-controlled circuit, an oscillator, an amplifier, a sample-and-hold circuit, a comparator, and an output-stage circuit. The magnetic field signal was converted to a voltage signal by the Hall element; the voltage signal was then compared and outputted after amplification and sampling [11, 12].

3.1. Signal Amplification Module. As shown in Figure 8, the amplifying circuit module was composed of the input-stage amplifying circuit IA1 and the second-stage amplifying circuit IA2. As the Hall elements only produce a Hall voltage of

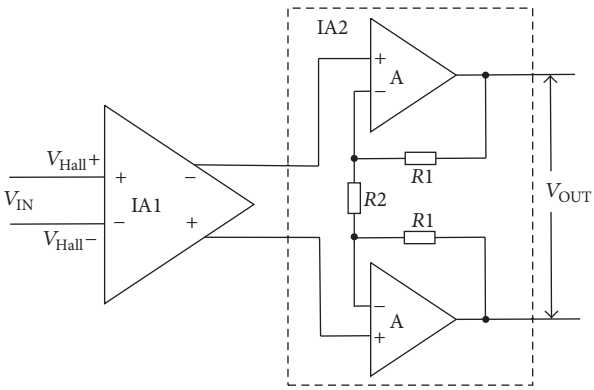

Figure 8: Amplifying circuit module of the Hall switch sensor.

approximately a few tens of microvolts, the offset voltage and noise can annihilate the effective Hall voltage signal. The most important issue to consider is the noise and offset of IA1. IA1 was used as a load in the form of diode connection and worked in an open-loop amplification mode, with an open-loop gain of 18 dB and a 3 dB bandwidth of 5.89 MHz. IA1 has a good signal-to-noise ratio, low input offset voltage, and good linearity of gain. Under different supply voltage, temperature, and process parameters, the range of the variation of gain was less than 8%. IA2 was realized using a fully differential instrumentation amplifier and featured strong anti-interference ability and stable output gain. The IA2 circuit consisted of two basic CMOS operational amplifiers that formed a double-ended input and double-ended output amplifier. By adjusting the resistance of $R1$ and $R2$, a stable gain was obtained, as required. The gain in this paper was 26.5 dB, and the 3 dB bandwidth was 128 KHz. The IA1 gain was set as $G1$, and the IA2 gain was set as $G2$. According to Figure 8, the total gain of the amplification module is as follows:

$$G = \left|\frac{V_{OUT}}{V_{IN}}\right| = G1 \cdot G2 = G1 \cdot \left(2\frac{R1}{R2} + 1\right). \tag{7}$$

3.2. Awake Control Module. Clock-controlled micropower technology was used to develop a low-power Hall switch sensor [13]. The clock logic circuit inside the sensor allowed it to sample in the external magnetic field every 45–60 ms. There were two working modes in a cycle: awake mode and sleep mode. In awake mode, the Hall voltage generated by an induced magnetic field was sampled, and it worked on a clock pulse of 1/1000 of a duty cycle. It was in sleep mode at all other times. During sleep mode, the chip's power consumption was almost negligible, as shown in Figure 9. The average current consumption decreased from 4–6 mA to 7.89 μA at 3.3 V supply voltage without affecting the normal operation of the Hall switch sensor.

3.3. Signal Sampling-Hold-Compare Module. The designed Hall switch sensor is a full-polarity magnetic field switch. In other words, it should work normally in both the N-pole magnetic field and the S-pole magnetic field. As shown in

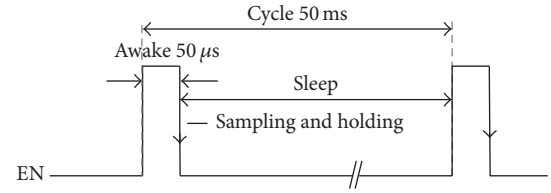

Figure 9: Low-power clock control module.

Figure 10, in a particular magnetic field ($B > 0$ or $B < 0$), the output of a comparator is always kept low to keep the subsequent NMOS switch tube in a disconnected state so that the overall output will not be affected. The other comparator reflects the results of the comparison of Hall voltage and reference voltage. When the Hall voltage is greater than the reference voltage, the comparator output is high. The NMOS switch tube is turned on, and the potential of the overall output is pulled to ground. When the Hall voltage is lower than the reference voltage, the comparator output is low. The NMOS switch tube is disconnected, and the potential of the overall output is VDD [14, 15].

It is assumed that magnetic field $B > 0$ to analyze the working state of the sampling-hold-compare circuit. During stage Φ1, the output voltage of Hall element was set as $V_{i1} = V_{offset} + V_{Hall}$, and the input voltage of INP and INN was V_{+1} and V_{-1}, respectively. The common mode voltage of the amplifier was V_C. At this point, the comparator was in autozeroed state. The amplified voltage V_{i1} was sampled by capacitor C_S, and the reference voltage V_{ref} was sampled by capacitor C_H. During stage Φ2, the output voltage was set to $V_{i2} = -V_{offset} + V_{Hall}$, and the input voltage of INP and INN was V_{-2} and V_{+2}, respectively. The amplified voltage V_{i2} was sampled by capacitor C_S, and the reference voltage V_{ref} was sampled by capacitor C_H. The polarity of the sampled voltage in stage Φ2 was the opposite to that in stage Φ1. The comparator functioned normally in stage Φ2. At the end of stage Φ2, V_P and V_N are as follows:

$$\begin{aligned} V_P &= \frac{1}{C_S + C_H}\left[\left(-V_{-1} \cdot C_S + V_{+2} \cdot C_S - V_{ref} \cdot C_H\right)\right] \\ &\quad + V_C, \\ V_N &= \frac{1}{C_S + C_H}\left[\left(-V_{+1} \cdot C_S + V_{-2} \cdot C_S + V_{ref} \cdot C_H\right)\right] \\ &\quad + V_C. \end{aligned} \tag{8}$$

$G \cdot V_{i1} = G \cdot (V_{offset} + V_{Hall}) = V_{+1} - V_{-1}$ and $G \cdot V_{i2} = G \cdot (-V_{offset} + V_{Hall}) = V_{+2} - V_{-2}$, so the input of the comparator at the end of stage Φ2 is as follows:

$$\begin{aligned} V_{COMP} &= V_P - V_N \\ &= \frac{1}{C_S + C_H}\left(2G \cdot V_{Hall} \cdot C_s - 2V_{ref} \cdot C_H\right). \end{aligned} \tag{9}$$

When $V_{COMP} > 0$, the output of the comparator is high, and when $V_{COMP} < 0$, the output is low.

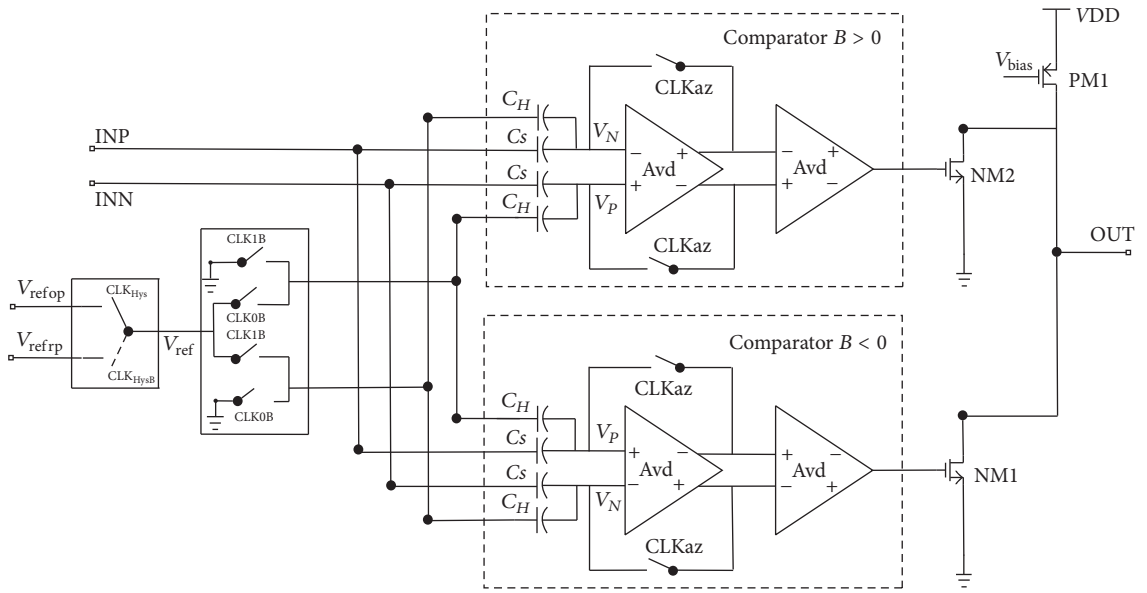

Figure 10: Sampling-hold-compare circuit module.

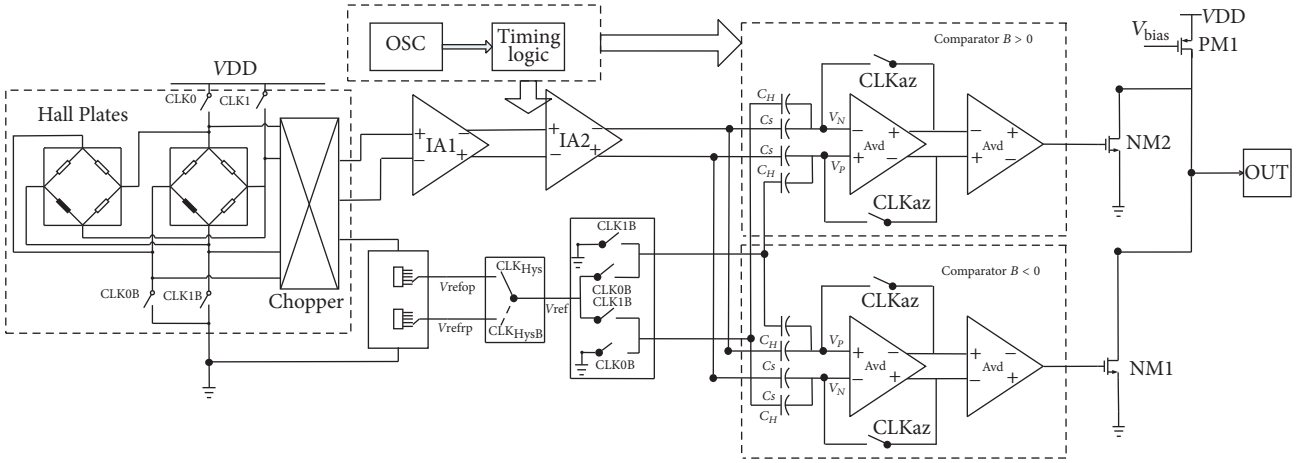

Figure 11: Circuit structure of the Hall switch sensor.

3.4. Working Process of the Entire Circuit. As shown in Figure 11, the changes in the magnetic field led to variations in Hall voltage, and the amplified Hall voltage was compared to the set reference voltage V_{ref} and then outputted the switch signal. The operate point B_{OP} and the release point B_{RP} could be changed by altering the voltage V_{ref}. The overall output of the sensor chip was determined by the output of the comparison circuit and the counter circuit. If the comparator circuit generates two consecutive high outputs, the Hall switch output will be low; if the circuit produces two consecutive low outputs, the switch output will be high.

The overall time series of the circuit is shown in Figure 12. The chip was set to awake mode and sleep mode to reduce the power consumption without compromising the chip's ability to test magnetic fields. Meanwhile, the chip's working state and oscillator's oscillation frequency were controlled by signal EN. When EN was high, the magnetic field was detected by the chip, with a clock oscillation frequency of 100 kHz. When EN was low, the chip entered the sleep mode, and the circuit stopped detecting magnetic fields. The clock oscillation frequency became 8 kHz. The awake mode consisted of a reset phase, Φ0, and two consecutive measurement phases, Φ1 and Φ2. The Φ0 circuit was reset to start. Then, the Hall element circuit was disconnected, and the signal processing circuit did not detect any output. In phases Φ1 and Φ2, complementary nonoverlapping clocks CLK0 and CLK1, which served as switching signals, controlled the Hall element to realize spinning current.

4. Chip Testing and Analysis

SMIC 0.18 μm CMOS technology was used for the design. An image of the chip and the packaging diagram are shown in

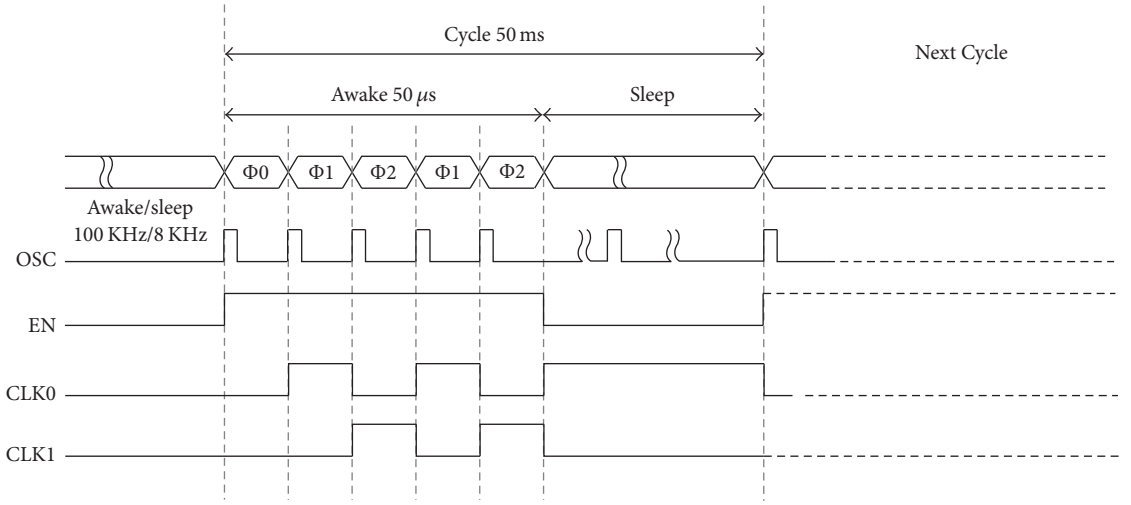

Figure 12: Circuit logic time series of the Hall switch sensor.

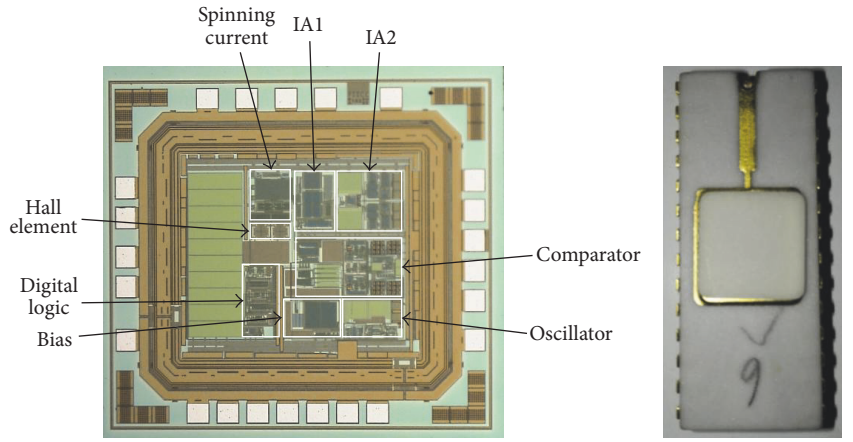

Figure 13: Photograph of the chip and packaging.

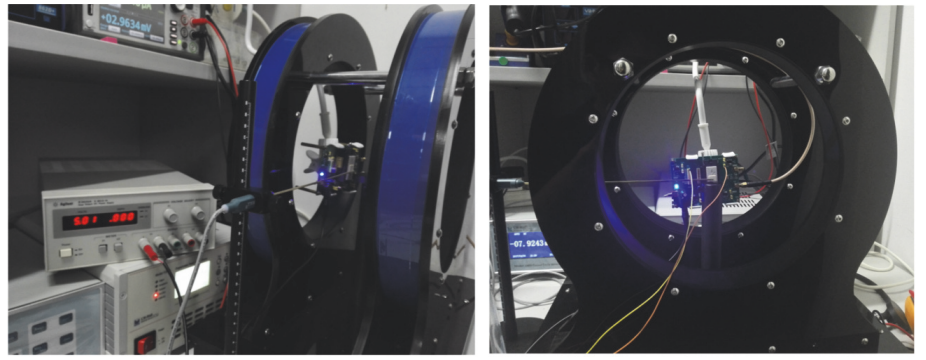

Figure 14: Physical setup of the testing system.

Figure 13. The design area of the chip was 720 μm × 550 μm. A dual in-line 28-pin ceramic package (CDIP28L) was used.

4.1. Test of Operate Point and Release Point. Figure 14 shows the physical diagram of the testing system. The use of a high-precision current source on the one-dimensional Helmholtz coil generated a high-precision magnetic field so as to test the operate point and release point of the Hall switch sensor. The coil was set to generate a triangular-wave magnetic field with full-cycle changes. The peak was ±10 mT. Table 1 shows the test results for 10 chip samples. According to the test data, the magnetic field operate point B_{OP} of the designed integrated

Table 1: Operate points and release points of the Hall switch sensor.

Chip number	N-pole B_{OP}	N-pole B_{RP}	S-pole B_{OP}	S-pole B_{RP}	Units
1	6.007	3.740	5.988	3.690	mT
2	6.300	3.966	6.350	3.920	mT
3	6.187	3.900	6.160	3.766	mT
4	6.155	3.845	6.201	3.921	mT
5	6.215	3.865	6.236	3.903	mT
6	6.176	3.916	6.056	3.746	mT
7	6.105	3.815	6.175	3.885	mT
8	6.237	3.917	6.195	3.915	mT
9	6.189	3.891	6.153	3.853	mT
10	6.064	3.750	6.127	3.777	mT
Average	6.1635	3.8605	6.1641	3.8376	mT
Standard deviation	0.0856	0.0738	0.098	0.0853	

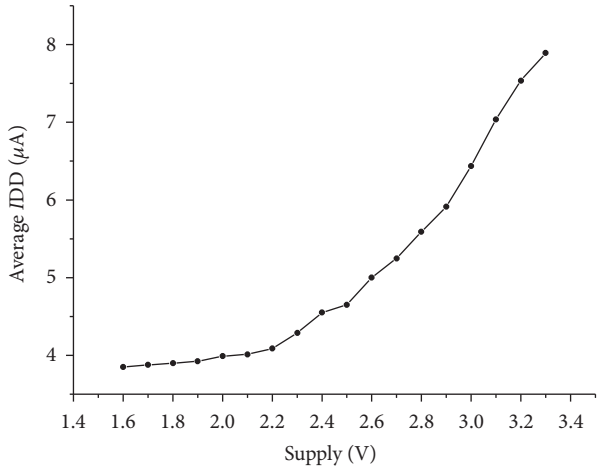

Figure 15: Testing results of power consumption at room temperature.

Hall switch sensor was approximately ±6.16 mT. The release point B_{RP} was approximately ±3.84 mT, and the hysteresis interval B_{HYS} was approximately 2.32 mT.

4.2. Power Consumption Test. A digital logic module was used on the designed Hall switch sensor chip to enable the two modes, namely, awake mode and sleep mode, which reduced the power consumption. The switch AWAKE was used to manually control the chip's working state in order to test its power consumption. Figure 15 shows the power consumption at room temperatures with different supply voltages.

4.3. Testing Results. The testing results in Table 2 show that by introducing sleep mode for the chip using a digital logic clock technology the power consumption of the Hall switch sensor was successfully reduced from the milliwatt level to the microwatt level; the operate point and the release point of the switch were within the range of 3–7 mT, which is applicable to switches and distance detection that usually require a magnetic field intensity of 3–50 mT.

Table 2: Test of the Hall sensor.

Parameters	Conditions	Results	Units
B_{OP}	VDD = 3.3 V, T = 25°C	±6.16	mT
B_{RP}	VDD = 3.3 V, T = 25°C	±3.84	mT
B_{HYS}	VDD = 3.3 V, T = 25°C	2.32	mT
S_V	VDD = 3.3 V, T = 25°C	20.335	mV/VT
$I_{DDaverage}$	VDD = 3.3 V, T = 25°C	7.89	μA

5. Conclusions

SMIC 0.18 μm technology was used to design an omnipolar low-power Hall switch sensor. The use of a digital logic clock enabled the sleep mode for the chip, thereby reducing its power consumption. The working frequency of the designed sensor was greater than 20 Hz, rendering it suitable for low-speed switches. Moreover, the offset voltage of Hall element and signal processing circuit was effectively suppressed by using the offset voltage suppression technology, resulting in an improvement in the performance of the Hall switch sensor.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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