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Research Article

Comprehensive Optimization of Dual Threshold Independent-Gate FinFET and SRAM Cells

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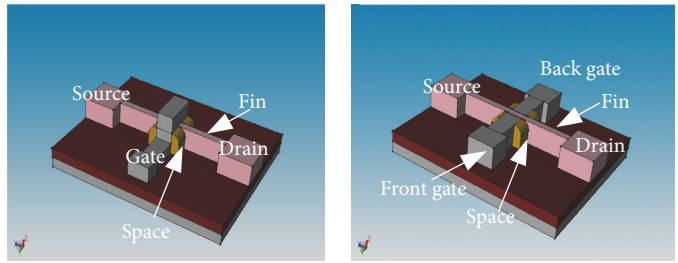
Independent-Gate (IG) FinFET is a promising device in circuit applications due to its two separated gates, which can be used independently. In this paper, we proposed a comprehensive method to optimize the Dual Threshold (DT) IG FinFET devices by carrying out modulations for the gate electrode work function, oxide thickness, and silicon body thickness. Titanium nitride (TiN_x) is used as the tunable work function gate electrode for good performances. The thicknesses of the gate oxide and silicon body are swept by TCAD simulations to obtain the appropriate values. The verification simulation of the optimized transistors shows that the DT IG FinFETs can realize merging parallel and series transistors, respectively, and the current characteristics of the transistors are improved significantly. By extracting the BSIM-IMG model parameters, we can simulate the circuits composed of the proposed DT IG FinFET by using HSPICE with BSIM-IMG model. As practical examples, we optimized two novel 7T SRAM cells using DT IG FinFETs. HSPICE simulation results indicate that the new SRAM cells obtain higher write margin and read static noise margin with lower leakage power consumption than the other implementations.

1. Introduction

Currently, FinFET has become mainstream IC technology due to its significant leakage reduction and performance improvement compared with the traditional planar CMOS. As a dual gate device, FinFET is more flexible than single gate devices, such as traditional CMOS and ultra-thin body (UTB) MOSFET. The two gates of the FinFET can work together or work separately, and it can provide greater flexibility and better performance in circuit designs. Shorted-Gate (SG) FinFET with two gates tied together can replace the single device in conventional circuits to achieve better performance and smaller size. But the Independent-Gate (IG) FinFET with two separated gates, formed by removing the material above the gate region of the fin, can provide different configuration methods and is suitable for different requirement in circuit designs.

Previous researches have seen that a regular IG FinFET is a low threshold device and it can be used as two merging parallel transistors to reduce the size and improve the performance in circuit designs. Some of the literature also proposed optimizations of the high threshold IG FinFET that can be used in circuits as merging series transistors to reduce the stack height and improve the operating speed [1–6]. The authors in [1, 2] optimized the values of the design parameters of gate work function, oxide thickness, silicon thickness, and gate underlap for both low threshold and high threshold devices. The parameters of the transistors were determined by using the University of Florida double gate (UFDG) SPICE model and verified by TCAD tool. In [3, 4], the authors only adjusted the value of gate work function to adjust the threshold voltage. In [5, 6], the high threshold IG FinFETs were used as basic logic cells to design circuits and the optimization procedure was not mentioned. There is more optimization space for the DT IG FinFETs, especially for the devices of the emerging technology node.

This paper proposed a comprehensive method to optimize the parameters for the Dual Threshold (DT) IG FinFET to obtain the better performance. We can know from the solution to the Poisson's Equation that the threshold voltage of a dual gate MOSFET is dominated by the gate work function (GWF) and the silicon body thickness. And we also know from the Vth roll-off theory that the oxide thickness can seriously impact the threshold voltage of a small size device.



(a) SG FinFET (b) IG FinFET

Figure 1: 3D structure of FinFET: (a) SG FinFET and (b) IG FinFET.

Therefore we optimize the DT IG FinFET by tuning the gate work function, oxide thickness, and silicon thickness by TCAD simulations. The optimized low threshold and high threshold IG FinFETs can serve as two merging parallel SG transistors and two merging series SG transistors, respectively. So the DT IG FinFETs can provide compact circuit implementations [2, 7]. And the on-state current (I_{on}) and leakage current (I_{off}) of the optimized DT IG FinFETs are also improved to reduce the delay and leakage of the compact circuits.

By using TCAD simulation results, we extracted the parameters for the BSIM-IMG model [8] and generated the model cards for simulation in HSPICE, which could be used for our circuit simulations. As practical examples, this paper realizes two novel 7T SRAM cells based on DT IG FinFETs, which have been simulated by HSPICE with the generated BSIM-IMG model cards. The simulation results show that the performances of the proposed SRAM cells are improved with the comparison of the other SRAM schemes.

The structure of the paper is organized as follows. In Section 2, after reviewing the traditional FinFET devices, we optimize the DT IG FinFET devices comprehensively by using appropriate gate electrode and modulating the oxide thickness and silicon body thickness to achieve good performance. The BSIM-IMG model fitting is also included in Section 2. In Section 3, we propose two novel 7T SRAM cells based on the DT IG FinFET devices and utilize more design space of DT IG FinFETs to improve read static noise margin (RSNM) and word line write margin (WLWM) and reduce leakage dissipation. And finally, conclusions are outlined in Section 4.

2. Optimization of DT IG FinFETs

In this section, we overview the FinFET firstly and then optimize the Dual Threshold FinFETs based on the modulation of the gate work function, the silicon body thickness, and the oxide thickness according to the theories. Finally, the Sentaurus Device simulations are used to determine the optimization parameters and test the current characteristics.

2.1. Overview of FinFET. FinFET is a double gate 3D transistor and has more benefits than ones of traditional planar CMOS. Especially in small geometric condition, the FinFET can effectively suppress the short channel effect (SCE) and drain induced barrier lowering (DIBL) effect, which are the two main reasons for limiting the size of planar CMOS transistor to scaling down to deep nanometer size. FinFET can be scaled down to sub 20nm channel length without heavy channel doping. Even in some modern technique, the channel and silicon body are undoped to minimize the impurity scattering. A lightly doped or undoped channel has higher carrier mobilities due to the lower transverse electric field and the negligible impurity scattering. In addition, it makes the FinFET have lower depletion charge and capacitance and thus a subthreshold slope of approaching to 60mV/dec [9].

There are two main configurations of FinFET devices as shown in Figure 1. The SG FinFET with two gates tied together, as shown in Figure 1(a), is used equivalently as the traditional planar single gate MOS transistor with better performance. If the front gate is logic high, the back gate is biased to high voltage to provide higher driving current and lower delay. When the front gate is logic low, the back gate is also biased to low voltage, which raised the threshold voltage and reduced the leakage current. In this way, the SG FinFET works like a single gate transistor and can directly transform the previous digital circuits by taking the place of the traditional CMOS devices to improve the performance and reduce the circuit area.

IG FinFET with two separated gates, which are formed by removing the material above the gate region of the SG device, is shown in Figure 1(b). The two gates are separated but strongly coupled to each other due to the thin Fin. In digital design, there are different performances when the back gate of the IG FinFET is connected in different way. It is the low power configuration when the back gate is in disabled mode (i.e., back gate is connected to VDD in PMOS or connected to GND in NMOS). In this mode, the threshold voltage is increased compared with the corresponding single gate device to reduce the leakage current. Meanwhile, its input capacitance is smaller and the dynamic power consumption is also lower. But the higher threshold voltage will increase the delay of the low power circuits, and so it can be used in the nonstrict path of the logic circuits. Because the threshold voltage of IG FinFET is highly sensitive to the voltage of the back gate, when the back gate of the transistor is used as the threshold voltage modulation terminal [10], threshold voltage can be adjusted in a certain range flexibly to balance the delay and power consumption. But the disadvantage is that it makes the circuit design and fabrication process more

complicated, and it limits the improvement of the circuit integration.

There is another mode with more flexibility to achieve the low power and improve the circuit integration simultaneously when the back gate is used as an independent signal input terminal. The advantage of this mode is that the one transistor can be used like two merging parallel traditional single gate transistors or two merging parallel SG FinFETs. It can attain the OR-like logic function of the two inputs, and thus it can largely reduce the amount of the transistors in a digital circuit and reduce the circuit area. It can increase the fan-in factor of a logic gate to improve its performance. Therefore, it can improve the flexibility of the digital circuit design except the extra considerations in the synthesis flow [4].

As the merging parallel transistors, IG FinFET can also work as merging series transistors when the threshold voltage is modulated to high enough, so that high threshold IG FinFET can realize the AND-like logic function of the inputs from the two gate electrodes [2]. But this realization needs special device engineering to modulate the threshold since the general double gate compact models, such as BSIM-IMG model, do not provide the high threshold FinFET model. In this work, we optimize and enhance the high threshold IG FinFET by modulating the work function of the gate electrode, the oxide thickness, and the body silicon thickness, which is addressed in the next section. For better cooperation with the high threshold device, the low threshold device is optimized at the same time in this paper.

Here, taking N-type FinFET as an example, we denote I_{dl0} as the drain current when back gate (BG) is tied to low and front gate is tied to high and I_{dl1} as the drain current when the two gates both connected to high. I_{on} and I_{off} are the on-state current and leakage current, respectively. When I_{on} is bigger, the operating speed is higher and the performance is better, and when I_{off} is smaller, the standby power is lower. When we optimize an IG FinFET device, we should consider the trade-off between the performance and the power dissipation, i.e., I_{on} and I_{off}. Additionally, in order to obtain the high threshold (high-V_{th}) device and realize the series AND-like logic function, I_{dl0} should be low enough to ensure the transistor is in off-state and I_{dl1} should be high enough to transform the transistor to on-state. And on the contrary, for a low threshold (low-V_{th}) device, I_{dl0} should be high enough to turn on the transistor to realize the OR-like logic function. When a high-V_{th} transistor and a low-V_{th} transistor work as a pair of dual threshold transistors, I_{dl0} of the low-V_{th} transistor should be higher than a cutoff current, about 10^{-7}·W/L (A), and I_{dl0} of the low threshold transistor should be lower than that cutoff current. Only by satisfying this condition, the dual threshold transistors circuit can work correctly. Note that the threshold voltage V_{th} can be accurately measured by extrapolating the I_D-V_G curve to the horizontal axis. But alternatively, it can be easy to get the value as the gate voltage at a small drain voltage of 0.05(V) and a small drain current of 10^{-7}·W/L (A) [11], where W/L is the aspect ratio of a transistor. Here in this paper the threshold voltage is measured just like this way.

In the next section, we will optimize the DT IG FinFET in detail. For convenience, we take the N-type FinFETs as examples to address the optimization procedure and only give out the results for the P-type FinFETs.

2.2. The Optimization of DT IG FinFETs. For a long channel double gate IG FinFET with lightly doped or undoped channel, the channel electrostatics under threshold condition is governed by the 2D Poisson equation with only the inversion charge term included [12]:

$$\nabla^2 \varphi(x, y) = \frac{q}{\varepsilon_{Si}} e^{q\varphi(x,y)/kT}, \tag{1}$$

where φ is the channel surface potential, q is the magnitude of the electronic charge, ε_{Si} is the permittivity of silicon, k is the Boltzmann constant, and T is the absolute temperature. Solving this 2D Poisson equation with some boundary conditions of the N-type FinFET, we can finally get the long channel threshold voltage (V_{th}) [13, 14]:

$$V_{th} = \Phi_{MS,i} + \frac{kT}{q} \ln\left(\frac{2C_{ox}kT}{q^2 n_i t_{Si}}\right), \tag{2}$$

where $\Phi_{MS,i}$ is the work function difference between the gate electrode and the silicon film, C_{ox} is the oxide capacitance, n_i is the intrinsic carrier concentration, and t_{Si} is the silicon body thickness (TSI).

This V_{th} equation (2) is derived for the long channel IG FinFET, but for a short channel transistor, we need to consider more effects, such as SCE, DIBL, and Quantum Effect (QE). So the V_{th} equation will become [15]

$$\begin{aligned} V_{th} = \Phi_{MS,i} + \frac{kT}{q} \cdot \ln\left(\frac{2C_{ox}kT}{q^2 n_i t_{Si}}\right) - 0.64 \cdot EI \cdot V_{bi} \\ - 0.80 \cdot EI \cdot V_{DS} + \frac{\pi^2 \hbar^2}{2qm^* t_{Si}^2}, \end{aligned} \tag{3}$$

where $\hbar$ is Plank constant, m^* is the effect mass of mobility, and EI is called Electrostatic Integrity factor given by

$$EI = \frac{\varepsilon_{Si} t_{ox} t_{dep}}{\varepsilon_{ox} L^2} \left[1 + \frac{x_j^2}{L^2}\right], \tag{4}$$

where ε_{ox} is the permittivity of oxide layer, L is the effective channel length, x_j is the source and drain junction depth, and t_{dep} is the penetration depth of the gate field in the channel region and t_{ox} is the equivalent oxide thickness (EOT).

The second term of right hand side (RHS) of (3) represents the potential in the channel, from which we can find that V_{th} is impacted by the silicon body thickness with inverse proportion. The third and the fourth items of RHS represent the voltage roll-off caused by SCE and DIBL, respectively, from which, it is known that V_{th} is impacted by the oxide layer thickness with inverse proportion.

From (3) and (4), we know that the threshold voltage V_{th} of a short channel transistor increases with the increase of the gate work function (GWF) or effective channel length (L) and decreases with the increase of the silicon body thickness (TSI) or equivalent oxide thickness (EOT). So we can optimize the threshold voltage by modulating the parameters of gate work

function, silicon body thickness, and gate oxide thickness, respectively.

The modulation of the gate work function can be achieved by carefully selecting appropriate gate electrode material to achieve the desired value. After careful investigation, in this work we chose the TiN_x as the gate electrode material for the optimized IG FinFET. It should be noted that the values of gate work function are different in NFET and PFET for the better performance of the two types of devices. The proper thicknesses of silicon body and gate oxide are obtained through TCAD device sweep simulations.

2.3. The Sentaurus Device Simulations Results. In this work, considering the practical manufacturing, TCAD three-dimensional (3D) simulations are carried out. All N-type and P-type transistors with independent gates are simulated by Synopsys Sentaurus Device tool. In these simulations, the drift-diffusion mobility and modified local-density approximation (MLDA) models are used. The mobility models include the mobility degradation due to scattering and high lateral and perpendicular electric fields. MLDA model is a numerically robust and fast model for quantum effect and it is suitable for three-dimensional device simulations because of its numeric efficiency [16]. According to the prediction of the International Technology Roadmap for Semiconductors (ITRS) [17], 14nm is an emerging technology node, and thus we choose the transistors with 14nm channel as the optimization target. First the 3D structure of the IG FinFET is established by using Synopsys Sentaurus Structure Editor. The 3D structure is shown in Figure 1(b) and the symmetrical cross section view is shown in Figure 2. The transistor we built is a High-K Metal Gate (HKMG) 3D FinFET, which is often used in modern high performance applications. The high-K dielectric is HfO_2 with a relative permittivity of 25, which is much higher than 3.9 of SiO_2, and thus the height of the gate stack can be increased to suppress the gate leakage. A SiO_2 thin film is inserted between HfO_2 and channel silicon for better bonding. The doping concentration of body region is N_{body}=1.0e12cm^{-3}, which is a relatively light value to improve the subthreshold slope. The doping concentration of source and drain region is a heavy value of N_{SD}=1.0e20cm^{-3} used to improve the impedance characteristic. The WF metal is a kind of alloy material (TiN_x, see below) used to modulate the work function of the gate electrode to obtain the desired performances. The Fin height of the device is a typical value of 40nm.

From aforementioned, because V_{th} is influenced by the silicon body thickness, gate oxide thickness, and the channel length, some TCAD device simulations are firstly carried out by sweeping the geometry values of TSI, EOT, and L, respectively, to study the relationship between V_{th} and these geometry sizes. Although the transistors we want to optimize are fixed channel length of 14nm, we also need to study the effects of SCE, DIBL, and QE. In addition, in order to obtain better performance of the transistor and to realize the series AND-like logic, we need to obtain the appropriate I_{d10}, $I_{d11,}$ and I_{off} of a device, so as to study the relation between the currents and the geometry parameters. The TCAD simulations have been carried out and the results are

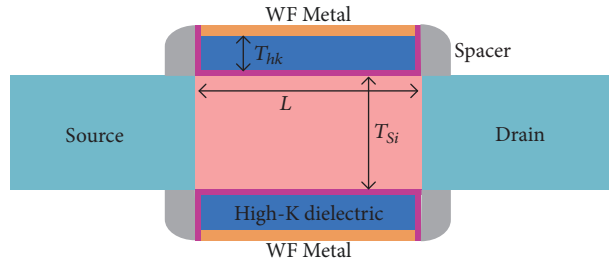


Figure 2: The cross section of the symmetric Independent-Gate High-K Metal gate FinFET with interfacial oxide between channel and high-k dielectric in TCAD simulation (N_{SD}=1.0e20cm^{-3}, N_{body}=1.0e12cm^{-3}, L=14nm, $HFin$=40nm).

shown in Figure 3. From the results, we can find out that V_{th} is decreased with the increase of EOT or TSI, or with the decrease of L. And I_{d01}, I_{d11}, and I_{off} are just the opposite, which are increased with the increase of EOT or TSI, or with the decrease of L. Note that the channel length L is only used to study physical effects such as SCE, DIBL, and QE, rather than as an optimization criterion in this paper.

Since the work function dominates the threshold voltage of the IG FinFET, the material of the gate electrode must be carefully selected to meet the V_{th} requirement. Several reports have shown that some values of the gate work function can be obtained by utilizing the available materials and processes. The titanium nitride (TiN_x) gate electrode with tunable work function can be achieved by varying the nitrogen gas flow rate in the reactive sputter deposition process of the metal gate [18–20]. Therefore we investigated the variation of V_{th} when the gate work function ranges from 4.0eV to 5.2eV for N-type FinFET by carrying out TCAD simulations. In order to get the relationship between V_{th}, I_{d10}, I_{d11}, and gate work function, TCAD simulations are also performed by sweeping the GWF values. The I_D-V_G characteristics of different gate work functions are then tested. The results of the measurements are shown in Figure 4, where the small diagram is a close-up picture of the upper range of GWF.

As shown in Figure 4, it can be found that, by increasing the gate work function of IG FinFET, the corresponding threshold voltage increases to a desired value as depicted. The relationship between gate work function and threshold voltage is linear, which agrees well with (2) and (3). From the current curves as shown in Figure 4, we can also find that the leakage current I_{off} and drain currents I_{d10} and I_{d11} all decrease with the increase of the gate work function, and the relationships are almost linear at small GWF and nearly exponential at big GWF.

The relationships in Figures 3 and 4 show that the influence of gate work function on threshold and current is larger than that of the geometric size TSI or EOT. Therefore, when the target device is optimized, the gate work function is first selected according to the voltage threshold and performance requirements, and then the geometric values of TSI and EOT are fine adjusted to meet the precision requirements.

When considering the trade-off among I_{d10}, I_{d11}, I_{d11}/I_{off}, and V_{th}, after a series of Sentaurus Device simulations had been carried out, the optimization parameters of N-type DT

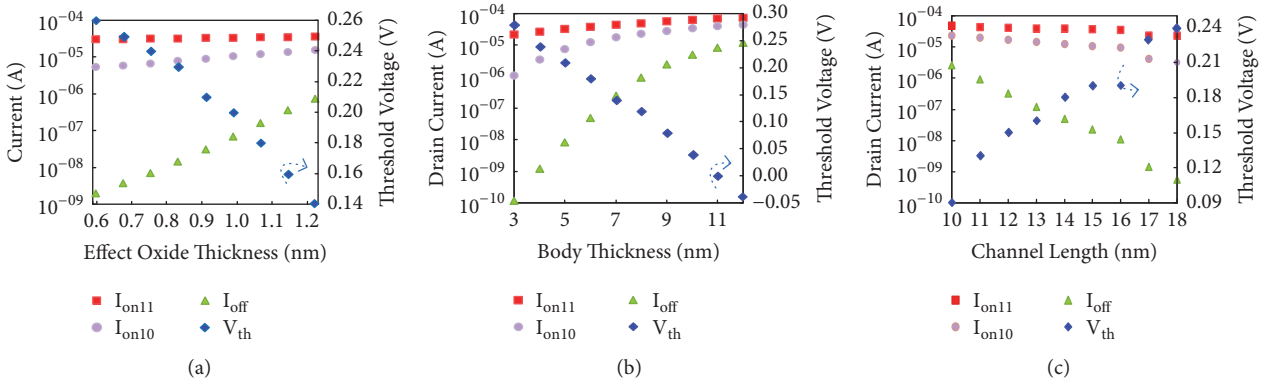


Figure 3: The trend of the drain current versus (a) EOT, (b) TSI, and (c) L.

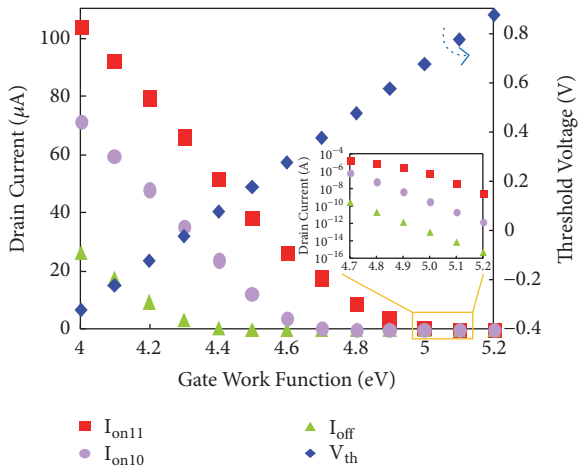


Figure 4: The trend of the drain current versus gate work function.

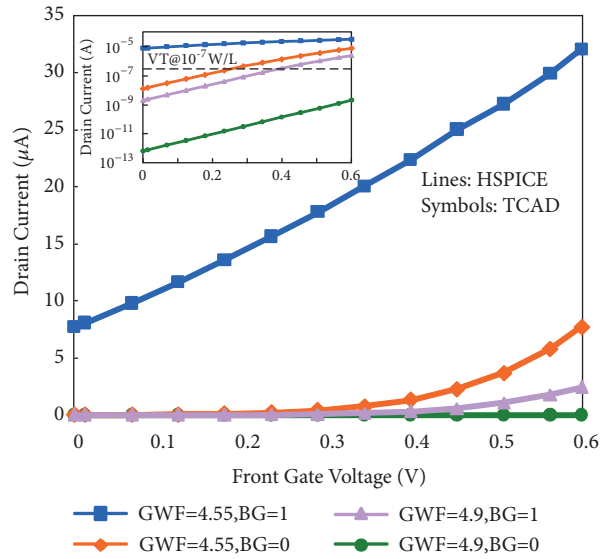


Figure 5: The current characteristic results of N-type DT IG FinFET from Sentaurus Device and HSPICE.

IG FinFET are selected as listed in Table 1. At the same time, in Table 1, some of the optimization results in literature [2–4] are listed as a comparison.

In Table 1, H represents the high-V_{th} transistor, while L is low-V_{th} transistor, and N/A indicates that data cannot be obtained from the literature. From these results, we can find that our results meet the needs of the novel transistor characteristics. The I_{dl0} is smaller than some comparison values but larger than others, and I_{dl1} is the same case. The ratio I_{on}/I_{off} of high-V_{th} transistor is the average among the comparison values, while the ratio I_{on}/I_{off} of low-V_{th} transistor is the biggest, from which, it can be seen that the proposed high-V_{th} transistor is in average performance and the proposed low-V_{th} transistor can work in high speed. Most importantly, the proposed transistors have the smallest occupation than others in area without the performance loss.

The current characteristics of the proposed N-type and P-type DT IG FinFETs have been measured by the Sentraurus Device tool. The tests are carried out by sweeping the voltage of the front gate from 0 (-0.6V) to 0.6V (0V) for N-type FinFET (P-type FinFET), when the back gate is activated by being tied to VDD (ground) or disabled by being tied to ground (VDD), respectively. The simulation results are plotted as symbols in Figures 5 and 6, and the subgraphs in the main diagrams are the same plots of logarithmic coordinates, and the dashed lines in figures are cutoff current lines. When the drain current rises to up the cutoff current line, the transistor will turn on, otherwise, the transistor will turn off when the drain current drops down to below the cutoff line. As can be seen from these curves, the high-V_{th} N-type IG FinFET with GWF=4.9eV is in on-state when front gate and back gate are both tied to high voltage; otherwise, they will be in off-state when one or none of the gate is tied to high voltage. The operation is just like the AND-like logic of the two gate signals and one high-V_{th} IG FinFET is working just like two merging series SG FinFET. On the other hand, the low-V_{th} N-type FinFET with GWF=4.55eV will be in on-state when any one of the two gates is tied to high voltage, and it will be turned off only when two gates are both tied to ground. The working mode is just like the OR-like logic of two gate signals.

As shown in Figure 6, for the P-type DT IG FinFETs, the operations are just complementary to the N-type FinFETs.

Table 1: Comparison with previous works.

	Ref. [2]	Ref. [3]	Ref. [4]	This work
L	32nm	25nm	22nm	14nm
Hfin	40nm	1um	1um	40nm
N_{body}	undoped	1e16	10e15	1e12
N_{sd}	2e20	N/A	10e20	1e20
TSI	H∗:6nm L∗:12nm	H:9nm L:N/A	H:80nm L:80nm	H:6nm L:6nm
EOT	L:1nm H:2nm	H:1nm L:N/A	H:2nm L:2nm	H:0.75nm L:0.8nm
GWF	H:4.8 L:4.5	H:4.85 L:N/A	H:5.2 L:4.5	H:4.9 L:4.55
Gate	Poly	MGHK	MGHK	MGHK
Vdd	0.9V	0.6V	1V	0.6V
I_{dl0}	H:1.0e-9A, L:2.0e-5A	H: 4.0e-7A L:N/A	H:2.0e-8A L:1.0e-3A	H:2.0e-9A L: 7.7e-6A
I_{dl1}	H:1.0e-5A L:4.0e-5A	H: 1.0e-4A L:*N/A*	H:1.0e-4A L:2.0e-3A	H:2.4e-6A L:3.2e-5A
I_{off}	H:5.0e-12A L:2.0e-11A	H: 2.0e-13A L:*N/A*	H:2.0e-15A L:2.0e-9	H:6.6e-13A L: 1.6e-8A
I_{on}/I_{off}	H: 2.0e+6 L2.0e+6	H:5.0e+6 L: *N/A*	H: 5.0e+10 L: 1.0e+6	H: 3.6e+6 L: 2.0e+3
Opt. Tools	FUDG/TCAD	MEDICI	MEDICI	Sentaurus Device

∗H: high-Vth transitor; L: low-Vth transistor.

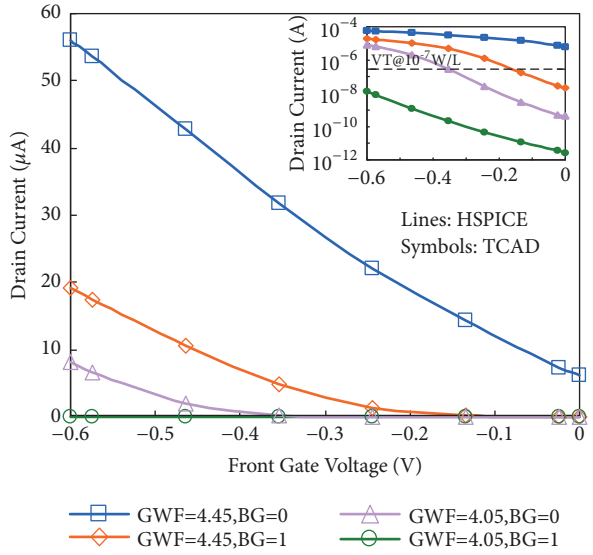


Figure 6: The current characteristic results of P-type DT IG FinFET from Sentaurus Device and HSPICE.

The high-V_{th} IG P-type FinFET works like two merging series SG FinFET of OR-like logic, and the low Vth IG FinFET works like two parallel SG FinFETs of AND-like logic.

After obtaining the optimized devices, the parameters in the BSIM-IMG model should be modified to match the parameters of the optimized devices [21]. BSIM-IMG model is a standard model adopted by Compact Model Coalition (CMC) [22] and the results of the simulations with BSIM-IMG model can be as a reference of IC manufacturing.

2.4. BSIM-IMG Model Fitting and HSPICE Simulation. FinFET compact model is the bridge between FinFET technology and FinFET-based circuits design. For the circuit simulation using the proposed DT devices, we choose BSIM-IMG model, a CMC standard compact model, from UC Berkley as our FinFET compact model in the applications. BSIM researchers have announced that the BSIM-IMG model is very effective for new devices when the parameters of model are properly adjusted [23]. For example, excellent BSIM model results for germanium FinFETs and InGaAs FinFETs are shown in [24, 25]. According to the instructions in BSIM-IMG technical manual, there are more than one hundred parameters that need to be extracted from the proposed devices based on several behaviors, such as long channel gate capacitance, long channel drain current, and short channel drain current to fit the curves from the TCAD simulation results.

The proposed devices are short channel devices of 14nm channel length. As a short channel device, some short channel fitting parameters are essential to be extracted. The V_{th} roll-off caused by short channel effect must be considered. This is modeled in BSIM-IMG model and given by [8]

$$\Delta V_{th,SCE} = -\frac{0.5 \cdot DVT0 \cdot (V_{bi} - \varphi_{st})}{\cosh\left(DVT1 \cdot L_{eff}/\lambda\right) - 1}, \quad (5)$$

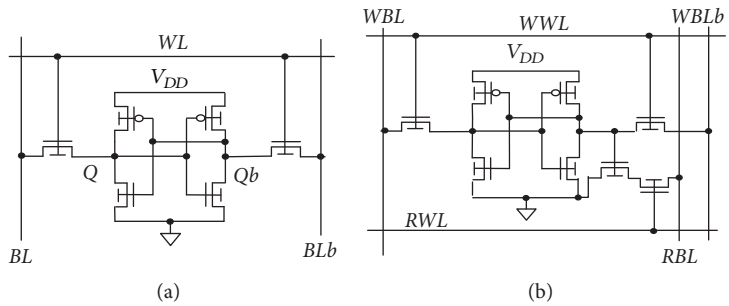


Figure 7: Reproduced from H. Yang et al. (2017) (under the Creative Commons Attribution License/public domain).

where λ is scale length factor, V_{bi} is built-in potential, φ_{st} is surface potential, L_{eff} is effective channel length, and *DVT0*, *DVT1* are parameters from device extraction.

As another effect, V_{th} roll-off caused by DIBL is modeled in BSIM-IMG model and represented by [8]

$$\Delta V_{th,DIBL} = -\frac{0.5 \cdot \left(ETA0 + ETAB \cdot V_{bgx}\right)}{\cosh\left(DSUB \cdot L_{eff}/\lambda\right) - 1} \cdot V_{dsx}, \quad (6)$$

where V_{gbx} approximates to back gate voltages V_{bg} and V_{dsx} approximate to drain terminal voltage V_{ds} when working in saturation region, and *ETA0*, *ETAB,* and *DSUB* are fit parameters from device extraction.

Above mentioned are two examples of the physics effects that affect the accuracy of the model. The parameters such as *DVT0, DVT1, ETA0, ETAB,* and *DSUB* all need to be carefully tuned to well fit the BSIM-IMG model for the proposed DT devices. The other model parameters that are related to physics effects, such as subthreshold slope degradation, carrier velocity saturation, and quantum mechanical effects, all need to be carefully adjusted. Therefore there are a set of parameters that need to be extracted from the experimental data of the devices to fit the BSIM-IMG model.

After parameters extractions, a series of HSPICE simulations are carried out for the verification, and the results are shown as the lines in Figures 5 and 6. The simulation results show that the BSIM-IMG model fits the devices very well and it can be used in the circuit designs and optimization based on the proposed DT IG FinFETs.

In the next section, we use the proposed devices to optimize the SRAM cells with the BSIM-IMG model.

3. Design and Performance of SRAM Cells

After reviewing the traditional SRAM cells, we present two new SRAM cells based on the optimized Independent-Gate FinFET devices. We discuss the performance of the new SRAM cells from some simulation results to end this section.

3.1. Traditional SRAM Cells. The traditional 6T SRAM cell based on SG FinFET devices (SG6T) is shown in Figure 7(a) [26], where the fin number of the two pull-down transistors must be increased to insure proper read operation. In order to improve RSNM and WLWM, an 8T SRAM cell based on SG FinFET devices (SG8T) with read-write separation structure is often used, as shown in Figure 7(b) [26, 27].

The back gate of IG FinFETs can be used to adjust the threshold of the devices to increase its driving ability or reduce its leakage current. The SRAM cells (IG6Ta-IG6Td) based on regular low-V_{th} IG FinFETs had also been investigated, as shown in Figure 8 [26], where the back gate of IG FinFETs is connected to ground or power source or the storage node to adjust their driving ability, and thus improve RSNM and WLWM, and reduce their leakage dissipation [28, 29].

3.2. Novel 7T SRAM Cells based on Proposed DT IG FinFET. The optimized DT IG FinFETs can serve as two merging parallel or series transistors, respectively. We utilize more design space of DT IG FinFETs to improve RSNM and WLWM and reduce their leakages. This work proposes two novel 7T SRAM cells (DGIG7Ta, DGIG7Tb) based on the optimized DT IG FinFETs abovementioned, as shown in Figure 9 [26]. The read and write operations are separated by adding a high threshold IG FinFET to improve the read and write stability. Only when Q is low and RWL is high, the high threshold IG FinFET is turned on, and the value of the storage cells is read to RBL. When Q is "1", the high threshold IG FinFET is turned off, and thus RBL will maintain its high level due to precharging.

In Figure 9(a), the write operation is the same as Figure 8(a), where the pull-down transistors use low threshold IG FinFETs. In Figure 9(b), the transmission gate consisting of a pair of low threshold P-type and N-type FinFETs is used as the access switch to promote driving ability and thus improve WLWN. The P-type and N-type high-V_{th} IG FinFETs constitute a clocked inverter controlled by WWL. At write period (WWL is high), the clocked inverter is turned off to promote write operation and to improve WLWN. At storage phase (WWL is low), the clocked inverter is enabled to hold its storage value.

3.3. SRAM Cell Performance Comparisons. The RSNM, WLWM, and leakage of the proposed SRAM cells (DTIG7Ta-DTIG7Tb) have been compared with the corresponding ones such as traditional 6T SRAM cell (SG6T), 8T SRAM cell with read-write separation (SG8T), and SRAM cells using regular IG FinFETs (IG6Ta-IG6Td), as shown in Figure 10. All circuits are simulated by HSPICE using BSIM-IMG

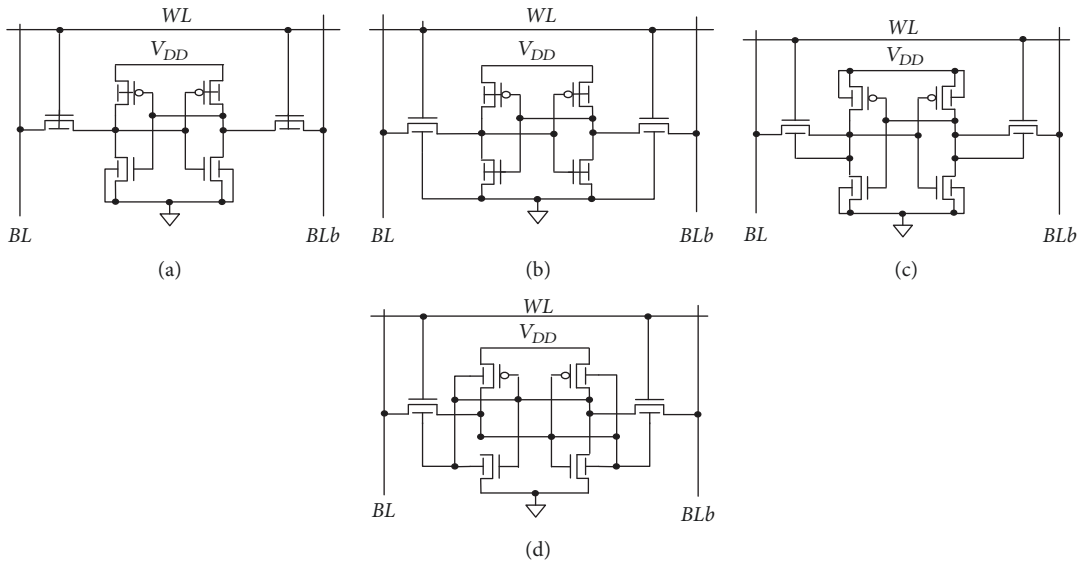


Figure 8: Reproduced from H. Yang et al. (2017) (under the Creative Commons Attribution License/public domain).

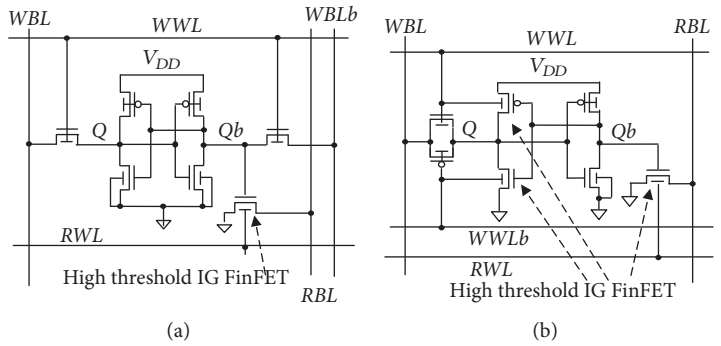


Figure 9: Reproduced from H. Yang et al. (2017) (under the Creative Commons Attribution License/public domain).

model. In order to assure the fairness of the comparison, the same read and write timing is given to all the SRAM cells. It is clear that, among all compared SRAM cells, the proposed two SRAM cells achieve best performance in terms of RSNM and WLWM and have lowest leakage dissipations.

4. Conclusions

This paper has proposed a novel high-V_{th} IG FinFET along with an optimized low-V_{th} one by modulating the gate work function, silicon body thickness, and gate oxide thickness, which can work as merging series transistors and merging parallel transistors. Sentiraurus Device simulation results show that the proposed DT IG FinFETs have excellent current characteristics (I_{d10}, I_{d11}, I_{off} and I_{on}/I_{off} *ratio*) and reduced occupied area of the device. After that, we extracted the parameters of the proposed devices for fitting the BSIM-IMG model to further circuit simulations. We also have proposed two novel 7T SRAM cells based on the optimized DT IG FinFETs. We utilize more design space of DT IG FinFETs to improve read static noise margin and write margin and reduce leakage power consumption. The HSPICE simulations based on the BSIM-IMG model show that the novel SRAM cells obtain higher write margin and read SNM with lower leakage power consumption than the other implementations.

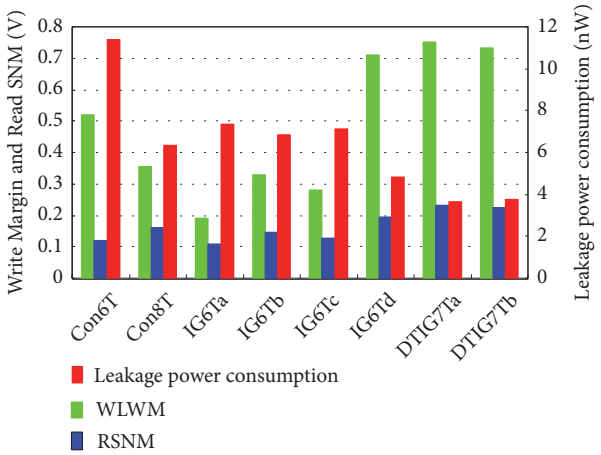


Figure 10: Performance comparison of SRAM cells.

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

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References

[1] M. Rostami and K. Mohanram, "Novel dual-Vth independent-gate FinFET circuits," in *Proceedings of the 2010 15th Asia and South Pacific Design Automation Conference, ASP-DAC 2010*, pp. 867–872, Taipei, Taiwan, January 2010.

[2] M. Rostami and K. Mohanram, "Dual-Vth independent-gate FinFETs for low power logic circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 3, pp. 337–349, 2011.

[3] M.-H. Chiang, K. Kim, C.-T. Chuang, and C. Tretz, "High-density reduced-stack logic circuit techniques using independent-gate controlled double-gate devices," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 2370–2377, 2006.

[4] M. C. Wang, "Independent-gate FinFET circuit design methodology," *IAENG International Journal of Computer Science (IJCS)*, vol. 37, no. 1, 2010.

[5] V. N. Possani, A. I. Reis, R. P. Ribas, F. S. Marques, and L. S. Da Rosa, "Exploring independent gates in FinFET-based transistor network generation," in *Proceedings of the 27th Symposium on Integrated Circuits and Systems Design, SBCCI 2014*, Aracaju, Brazil, September 2014.

[6] V. N. Possani, A. I. Reis, R. P. Ribas, F. S. Marques, and L. S. D. R. Junior, "New challenges on independent gate FinFET transistor network generation," 2014.

[7] X. Zhang, J. Hu, and X. Luo, "Optimization of dual-threshold independent-gate FinFETs for compact low power logic circuits," in *Proceedings of the 16th IEEE International Conference on Nanotechnology - IEEE NANO 2016*, pp. 529–532, Sendai, Japan, August 2016.

[8] Y. Singh Chauhan, S. Venugopalan, M. A. Karim et al., "BSIM Industry standard compact MOSFET models," in *Proceedings of the 42nd European Solid-State Device Research Conference, ESSDERC 2012*, pp. 46–49, Bordeaux, France, September 2012.

[9] Z. Guo, S. Balasubramanian, R. Zlatanovici, T.-J. King, and B. Nikolić, "FinFET-based SRAM design," in *Proceedings of the International Symposium on Low Power Electronics and Design*, pp. 2–7, San Diego, Calif, USA, August 2005.

[10] D. M. Fried, J. S. Duster, and K. T. Kornegay, "Improved independent gate N-type FinFET fabrication and characterization," *IEEE Electron Device Letters*, vol. 24, no. 9, pp. 592–594, 2003.

[11] C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, Prentice Hall, Upper Saddle River, NJ, USA, 2009.

[12] Y. Taur, "Analytical solution to a double-gate MOSFET with undoped body," *IEEE Electron Device Letters*, vol. 21, no. 5, pp. 245–247, 2000.

[13] Q. Chen, E. M. Harrell II, and J. D. Meindl, "A physical short-channel threshold voltage model for undoped symmetric double-gate MOSFETs," *IEEE Transactions on Electron Devices*, vol. 50, no. 7, pp. 1631–1637, 2003.

[14] H. A. El Hamid, J. Roig Guitart, and B. Iñíguez, "Two-dimensional analytical threshold voltage and subthreshold swing models of undoped symmetric double-gate MOSFETs," *IEEE Transactions on Electron Devices*, vol. 54, no. 6, pp. 1402–1408, 2007.

[15] J.-P. Colinge, *FinFETs and Other Multi-Gate Transistors*, Springer, 2008.

[16] G. Paasch and H. Übensee, "A Modified Local Density Approximation. Electron Density in Inversion Layers," *Physica Status Solidi (b) – Basic Solid State Physics*, vol. 113, no. 1, pp. 165–178, 1982.

[17] ITRS Reports, http://www.itrs2.net/itrs-reports.html.

[18] J. Westlinder, G. Sjöblom, and J. Olsson, "Variable work function in MOS capacitors utilizing nitrogen-controlled TiNx gate electrodes," *Microelectronic Engineering*, vol. 75, no. 4, pp. 389–396, 2004.

[19] Y. Liu, S. Kijima, E. Sugimata et al., "Investigation of the TiN gate electrode with tunable work function and its application for FinFET fabrication," *IEEE Transactions on Nanotechnology*, vol. 5, no. 6, pp. 723–728, 2006.

[20] L. Bolotov, K. Fukuda, T. Tada, T. Matsukawa, and M. Masahara, "Spatial variation of the work function in nano-crystalline TiN films measured by dual-mode scanning tunneling microscopy," *Japanese Journal of Applied Physics*, vol. 54, no. 4, Article ID 04DA03, 2015.

[21] A. Moshovos, B. Falsafi, F. N. Najm, and N. Azizi, "A case for asymmetric-cell cache memories," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 13, no. 7, pp. 877–881, 2005.

[22] UCB, "BSIM-IMG selected as FD-SOI standard model," http://bsim.berkeley.edu/bsim-img-as-fdsoi-model/.

[23] Y. S. Chauhan, D. Lu, S. Venugopalan, and S. Kh, *FinFET Modeling for IC Simulation and Design*, 2015.

[24] S. Khandelwal, J. P. Duarte, Y. S. Chauhan, and C. Hu, "Modeling 20-nm Germanium FinFET with the industry standard FinFET model," *IEEE Electron Device Letters*, vol. 35, no. 7, pp. 711–713, 2014.

[25] S. Khandelwal, J. P. Duarte, N. Paydavosi et al., "InGaAs FinFET modeling using industry standard compact model BSIM-CMG," in *Proceedings of the Nanotechnology 2014: MEMS, Fluidics, Bio Systems, Medical, Computational and Photonics - 2014 NSTI Nanotechnology Conference and Expo, NSTI-Nanotech 2014*, pp. 475–478, Anaheim, Calif, USA, June 2014.

[26] H. Yang, J. Hu, and H. Zhu, "Novel SRAM cells using dual-threshold independent-gate FinFETs," in *Proceedings of the 17th IEEE International Conference on Nanotechnology, NANO 2017*, pp. 358-359, Pittsburgh, Pa, USA, July 2017.

[27] L. Chang, D. M. Fried, J. Hergenrother et al., "Stable SRAM cell design for the 32 nm node and beyond," in *Proceedings of the 2005 Symposium on VLSI Technology*, pp. 128-129, Kyoto, Japan, June 2005.

[28] K. Ma, H. Liu, Y. Xiao et al., "Independently-controlled-gate FinFET 6T SRAM cell design for leakage current reduction and enhanced read access speed," in *Proceedings of the 2014 IEEE*

Computer Society Annual Symposium on VLSI, pp. 296–301, Tampa, Fla, USA, July 2014.

[29] K. Endo, S.-I. O'uchi, Y. Ishikawa et al., "Independent-double-gate FinFET SRAM for leakage current reduction," *IEEE Electron Device Letters*, vol. 30, no. 7, pp. 757–759, 2009.