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Research Article

An Architecture of 2-Dimensional 4-Dot 2-Electron QCA Full Adder and Subtractor with Energy Dissipation Study

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Quantum-dot cellular automata (QCA) is the beginning of novel technology and is capable of an appropriate substitute for orthodox semiconductor transistor technology in the nanoscale extent. A competent adder and subtractor circuit can perform a substantial function in devising arithmetic circuits. The future age of digital techniques will exercise QCA as preferred nanotechnology. The QCA computational procedures will be simplified with an effective full adder and subtractor circuit. The deficiencies of variations and assembly still endure as a setback in QCA based outlines, and being capricious and inclined to error is the limitation of these circuits. In this study, a new full adder and subtractor design using unique 3-input XOR gate with cells redundancy is proposed. This designs can be utilized to form different expedient QCA layouts. The structures are formed in a single layer deprived of cross-wiring. Besides, this study is directed to the analysis of the functionality and energy depletion possessions of the outlined full adder and subtractor circuits. For the first time, QCADesigner-Energy (QD-E) version 2.0.3 tool is utilized to find the overall depleted energy. The attained effects with QCADesigner have verified that the outlined design has enhanced functioning in terms of intricacy, extent, and latency in contrast to the earlier designs. Moreover, the redundant form of full adder and subtractor has uncomplicated and robust arrangement competing typical styles.

1. Introduction

Complementary Metal Oxide Semiconductor (CMOS) archetype based on current conventional transistors stays on Moores theory. This theory was intended in 1965 by Gordon Moore and forecasts that the figure of transistors positioned within a chip will multiply every 2 years. Thus, lessening transistor extent is desired to outline high-thickness, high-rapidity, and power-defeat circuits [1]. Nowadays, numerous cohesive circuits have been prepared on an extent of 0.230-0.330 microns; however, when the dimension of the circuit extends to 0.50 microns or less, substantial borders for instance power depletion and drawbacks with lithography and layout intricacy ascend [2]. Therefore, doubling the transistors number in a microchip every 2 years and doubling the clock rate every 3 years will not be potential. Therefore, to increase the functioning of arithmetic units, there is a requirement for additional archetypes [3]. As inheritor to typical CMOS, scientists have proposed a scheme where computations are executed with quantum dots. This model was entitled quantum-dot cellular automata (QCA), and, same as nowadays processers that transfer information within electrical flow from one site to another, the conduction of polarization level initiates information transmission. In nanoscale, QCA as a novel device paradigm is appropriate for nanometer computer architectures. The vital element in QCA is a four-dot squared cell, and two unoccupied identical charges are integrated in that cell. The activity of dots is organized transversely by these electrons that are the upshot of Coulombic connection. Unlike CMOS archetype, the comparative structure of the charges rather than current is applied to encrypt the binary information in QCA. Minimal energy utilization, firm operation, and small magnitudes are the entities of QCA circuit [4–8]. The

majority voter and inverter gate are the principal aspects of assembling QCA outlines [9]. Assembly time fault phases and functioning time defect degrees in nanotechnologies are practicable [10], and the malfunctioning performance of QCA designs has to be depicted with the fault-tolerant model of QCA circuits. The implementation of full adder and subtractor as the major component of the arithmetic procedures can precisely influence the functioning of the entire architecture. Full adder and subtractor have a notable role in assembling Arithmetic and Logical Unit (ALU) that is a processing subsystem [11–14]. QCA technology has very minimal energy dissipation [4–6]. The focal role of this work is to organize a novel outline for full adder and subtractor circuit based on three-input XOR gate deprived of wire crossing. The proposed circuits are assembled by the number of cellblocks in QCA and they achieve the anticipated functions. In an abridged practice, the foremost impacts of this study are as follows:

(i) designing an architecture for adder and subtractor by the minimal figure of cells, utilization area, and overall depleted energy,

(ii) assessing the organized layout with other contemporary outlines based on XOR gate and without XOR gate in terms of cell numbers, intricacy, and the expended area.

The succeeding organization will be conferred in the remainder of the study. A concise synopsis of the QCA technology is exhibited in Section 2. Section 3 spotlights existing works on adder and subtractor. In Section 4, the proposed designs are formed in terms of cells fabrication and input and output positions. Simulation outcomes with relative assessment are characterized in Section 5, and for the first time, dissipated energy is estimated with QD-E which is organized in Section 6. Decisively, specific concluding explanations and analysis of potential focuses are organized in Section 7.

2. Primitive Premises of Quantum-Dot Cellular Automata

Logic gates, wires, and clocking are elementary QCA views. These assessments are exercised to comprehend QCA technology sounder. Four dots are involved in QCA cells and a top-level figure of polarized QCA cells is shown in Figure 1. Every single cell is assembled in a quadrilateral outline by four quantum dots. Two electrons are permitted to channel between neighboring dots and these electrons are utilized to direct the cell. The electrons are positioned in opposed spots because of their reciprocal electrostatic revulsion. Figure 1 presents two corresponding organizations of electrons in the QCA and the organizations are symbolized as polarization P = +1 and P = 1, correspondingly. With polarization P = -1 to denote logic "0" and P = +1 to denote logic "1", binary figures can be recognized [11].

The entire logic functions are able to operate by ordering the groups of QCA cells. The polarization of adjoining cells is persuaded by Coulombic interfaces. The potential difficulties or barriers between the dots have outlined QCA architectures. The QCA architectures are clocked and coordinated

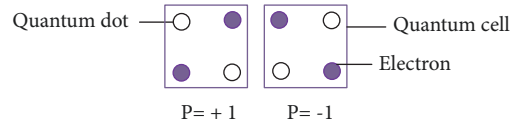

Figure 1: Cells in QCA.

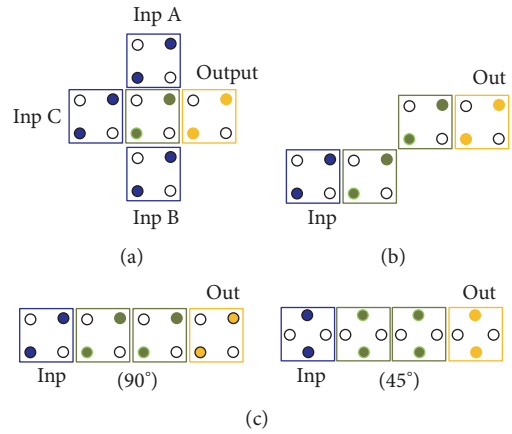

Figure 2: QCA structure cellblocks; (a) majority voter, (b) inverter gate, (c) 90° binary wires, 45° binary wires.

through barriers [7]. The communication of the cells and the performance of the entire architecture have been resolved by the QCA topology. The QCA cells are utilized to form all traditional logic circuits [15]. The formation of the majority voter is an essential part of QCA circuits as exhibited in Figure 2(a).

In the majority voter, three input cells are unified. One of the cells is in inside and persists the majority polarization because it signifies the minimal energy level. The other cell is the output cell. If one input is fixed to 1, the majority gate functions like OR. Similarly, if one input is fixed to 0, the gate acts as AND of the two additional inputs. The inverter has different arrangements in QCA and measured as the alternative vital gate. The resilient outline of the inverter is shown in Figure 2(b). Two neighboring cells have contradictory polarities while the energy level is minimal based on the Coulombic revulsion. The majority voter and inverter are incorporated to achieve all logical circuits. QCA wire performs a significant task in circuit design. The electrostatic contact between cells initiates the binary signal to read from input to output in the wire. Two sorts of wires are presented in Figure 2(c). The representation of a 90-degree binary wire is pointed out in the figure and the inverter chain is operated to reverse the input cells decently by rotated cells as pointed out in the figure.

The combinational and successive circuits need four sequential and definite segments to operate timing in QCA. The clocking operates the information stream and provides the genuine potential in QCA [11]. Four segments are Switch, Hold, Release, and Relax as integrated in QCA clock directed in Figure 3. The cell will be in a void position once the electrons are located in the central dots throughout relax

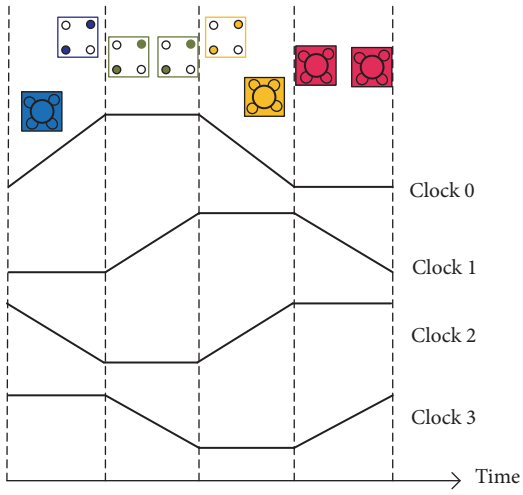

Figure 3: Clocking structure in QCA.

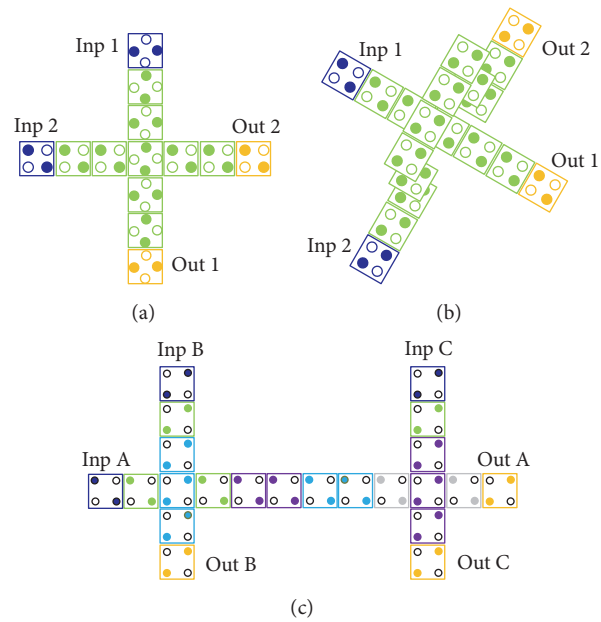

Figure 4: QCA crossing over: (a) coplanar crossing, (b) multilayer crossing, (c) logical crossing.

level. Through Switch phase, inner barriers of dots gradually emerge and push the electrons between the edges. At the time of Hold phase, the barriers are active and the cell persists in polarization and influences its adjacent. Finally, in Release segment, the barriers are downward and the electrons are drawn into the central dots [16, 17].

The QCA circuits are conceived by three sorts of crossover methods, namely, coplanar, multilayer, and logical crossing. In coplanar crossing, one of the wires utilizes only cell type one, whereas the other utilizes just cell type two, resulting in the wires functioning autonomously on the uniform fabrication layer as presented in Figure 4(a). All logic crossing is implemented on a particular QCA layer through this process with no requirement for a complement in the conventional technologies. A drawback of coplanar crossing is excessive manufacturing sensitivity. The regular assembly is certainly broken by cells which are not in position and, incidentally, an adverse coupling between two wires is transpired [18].

A customary multilayer crossing is developed as presented in Figure 4(b). The signal change from a particular layer to another is disallowed because of the outsized perpendicular space of wires. This approach is further lenient of misplaced cells than the coplanar crossing; however, several active QCA layers are required to implement the technology. The operation of multilayer technology is still not reasonable, and the assignment of single layer cell involves extreme accuracy that is very confronting [19] so this work is organized so as to only utilize the coplanar crossing.

A special sort of coplanar wire crossing is performed by Shin Jeon and Yoo [20] that specified as logical crossing. In this structure, wire crossing via interfering of clocking phases is achieved as shown in Figure 4(c).

QCA defects are divided into three arrangements, materializing through the fabrication of a circuit. Switching the cells from their anticipated positions is termed misalignment cells. The operation of the QCA circuit is not imitated by misalignment cells but, occasionally, there is an unanticipated result in a circuit. Another form of faults ensues once the cell is misplaced due to its defects. In this circumstance, the missed cell would have no impact on its adjacent and it influences the functionality of the design [21]. The last one ensues while cells are rotated corresponding to the other cells in the array that is termed dislocation cells, and in this instance, the design does not operate. Figure 5(a) organizes an omitted cell layout in which the circuit stops functioning. As present in Figure 5(b), a circuit may have an unanticipated result once the displacement cell has 45-degree rotation angle. Figure 5(c) presents misalignment cell in a design. Evidently, the direction of the cell association is not substantial because of symmetry.

3. Related Designs

The most elementary constituent in the outline of the arithmetic block is a full adder, and the succeeding equations are frequently reflected in the pattern of a full adder.

$$Sum\,(s) = A \oplus B \oplus C_{in} \tag{1}$$

$$Carry\,(cop) = AB + C_{in}\,(A \oplus B) \tag{2}$$

The output Sum is the binary addition of the inputs A, B, and C where A, B are the unique two binary inputs coupled with C which is the Carry out of the least significant bits. Cop signifies the produced Carry from the sum of the binary inputs A, B, and C. Table 1 presents the logical table of a full adder. In latest nanotechnology, study on the architecture of nanoscale full adder is considerably enlarged particularly in the QCA [22, 23]. An adder designed with two majority voters is presented in [22]. This design uses a five-input majority voter to produce Sum output. In [23], an outline of single-bit full adder with two inverters and three majority voters is

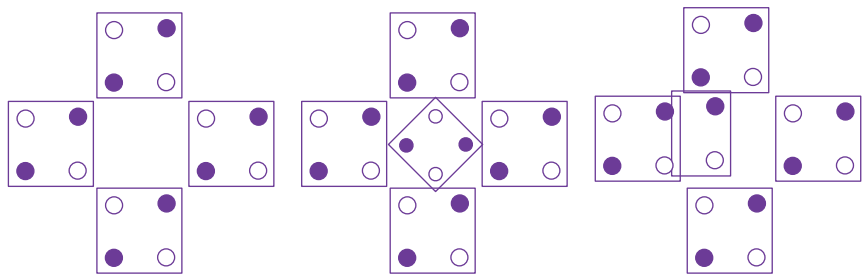

Figure 5: QCA defects: (a) omitted cell, (b) displacement cell, (c) misalignment cell.

Table 1: Truth table for full adder layout.

A	B	C	Sum	Cop
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	0	0	1

Table 2: Truth table for subtractor layout.

A	B	C	Diff	Borr
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

presented. Both of the designs in [22, 23] use cross-wiring and thus are not robust. In [24], the design of presented full adder contains two foremost components, the three-input XOR gate and the three-input majority voter. In this layout, the orthodox wire crossing technique is used to conduct two input values individually.

A subtractor is a circuit that subtracts two bits with considering the outcome of lower substantial phase. The truth table for subtractor is presented in Table 2, where A, B, and C are corresponding inputs, and Diff and Borr are outputs. Boolean expressions for Diff and Borr are presented as follows.

$$Diff = A \oplus B \oplus C \tag{3}$$

$$Borr = \overline{A}B + \overline{(A \oplus B)}C \tag{4}$$

In [25], a layout of full subtractor is proposed, which consists of 136 QCA cells with wire crossing. Another design is outlined in [26], where 62 cells are employed but with multilayer approach. Therefore, these designs are not robust. In the succeeding section, a new paradigm for the full adder and subtractor circuit based on the XOR gate [9] without cross-wiring is proposed.

4. Proposed Outline in QCA

To realize the performance of full adder and subtractor, circuit coulomb interaction is used. The geometry and accuracy of implantation are important to the appropriate operation of a device. As pointed out in Section 2, the blocks in the QCA are assembled with inverter and majority voter. Though, the most common majority voter has very inconsequential fault-tolerant performance against most of the common deficiencies. This section clarifies the outlined full adder and subtractor design. For this point, the structure of XOR gate is obtained from the design [9]; then define the architecture of the full adder and subtractor using QCA cells. The full adder structure has 28 cells. Three cells with labels A, B, and C are input cells. The output is termed as S and C, where S defines the Sum signal and C define the Carry signal. The remaining cells are labeled as device cells. The subtractor outline has 27 QCA cells. Three cells with labels A, B, and C are input cells. The output is entitled as Diff and Borr, where Diff state the Difference signal and Borr state the Borrow signal. Both of the architectures are conceived in a single layer and their latency is two clock zones, so the proposed designs are robust.

The schematic outline of the proposed full adder and subtractor design is shown in Figures 6(a) and 6(b), correspondingly. The full adder structure is comprised of one three-input XOR gate and one three-input majority voter.

Similarly, the subtractor design is comprised of one three-input XOR gate and one three-input majority voter with one inverter gate. As presented in Figure 7, the outlined designs are employed in a single layer. It uses only 90-degree QCA cells and does not use any coplanar wire crossing.

5. Testing of the Proposed Architectures with Comparative Assessment

In this section, QCADesigner ver. 2.0.3 is applied to simulate the outlined circuits. Simulation engines, features, and relative comparisons are explained in the remainder of this section.

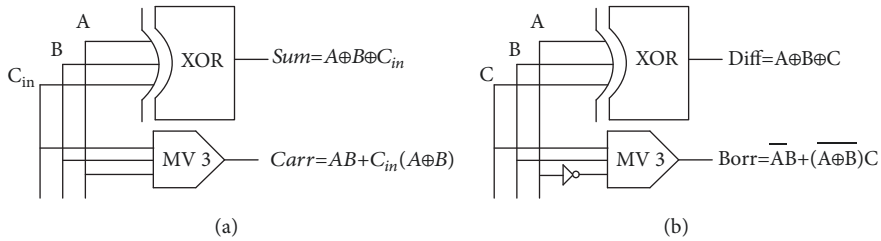

Figure 6: Schematic QCA outline: (a) full adder, (b) subtractor.

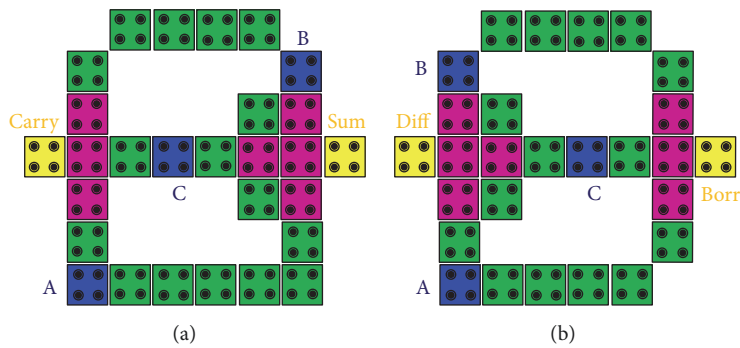

Figure 7: Architecture of proposed QCA outline: (a) full adder, (b) subtractor.

5.1. Simulation Engine and Features. QCADesigner is a recognized simulation engine mostly used for estimating QCA circuits. Bistable approximation and coherence vector simulation are measured as two distinct simulation tools. The bistable approximation tool analyses the position of a particular cell with a time-independent method by kink energy procedure that estimates the charge of two cells taking reverse polarization; thus simulation period in this tool is condensed. The coherence vector methodology thinks through the time-reliant status of a cell in collaboration with the other cells through the similar kink energy procedure [27]. Every cell in QCADesigner can perform in four ways, namely, input, output, fixed, and normal. The extent of the simple quantum cell is fixed at 18x18 with 5 nm thickness quantum dots. The center to center space was fixed at 20 nm for neighboring cells. The simulation tool is fixed to coherence vector form in QCADesigner engine with the simulation features being presented here: relaxation period 1.0e-015s, radius force 65 nm, relative permittivity 12.90, clock high-level 9.8e-22J, clock low-level, 3.8e-23J, separation of layer 11.50 nm, overall simulation period 7.0e-011s, and samples number 50000.

5.2. Accuracy Study. The proposed designs are simulated and Figure 8 presents the outcomes. Furthermore, for the input set {C B A} = {000, 001, 010, 011, 100, 101, 110, 111} all separate outcomes in the output Sum are attained: {01110001, 00001111, 11001100, 11010100, 01010101, 00101011, 10101010, 01001101, 00010111, 00110011}; similarly, all separate outcomes in the output Carry are attained: {11101000, 00110011, 00001111, 01001101, 10001110}. For adder circuit, if inputs A, B, and C are zero, the output values for Sum (S) and Carry (C) are 0, separately. For inputs A=0, B=0, and C=1, the output values for Sum (S) and Carry (C) are 1 and 0, individually. Likewise, for full subtractor, if the input values are A=B=C=0, then the output values for Difference (Diff) and Borrow (Borr) are both 0, individually. For inputs values, A=B=0 and C=1, the output values for Difference (Diff) and Borrow (Borr) are both 1, respectively.

5.3. Intricacy Study of the Proposed Architectures. The intricacy of the outlined designs is presented in Table 3. The full adder layout is achieved with one XOR gate, 28 QCA cells with an extent of $0.02\mu m^2$, and for subtractor layout one XOR gate, 27 QCA cells with an extent of $0.03\mu m^2$.

5.4. Comparison Study of the Proposed Architectures. The designed full adder is compared with the preceding three designs based on XOR gate presented in [22, 23, 28]. Execution outcomes are specified in Table 4 and the table covers the total figure of cells used for design, covered extent, and latency as well as wire crossing. The proposed design achieved 69, 52, and 32% progress in total cell count compared to the designs presented in [22], [23], and [28], correspondingly. The proposed structure achieved 78, 54, and 50% progress in covered area compared to the designs organized in [22], [23], and [28], correspondingly. Besides, the number of clock zones has lessened by 60 and 50% contrasted to the designs organized in [22], [23], and [28], correspondingly. The outlined design does not employ any cross-wiring. Similarly, for subtractor design, a firm improvement is achieved. The proposed subtractor attained 48, 80, 88, and 90% improvement in total cell count compared to the designs organized in [25], [26], [29], and [30], respectively. An improvement of 23, 82,

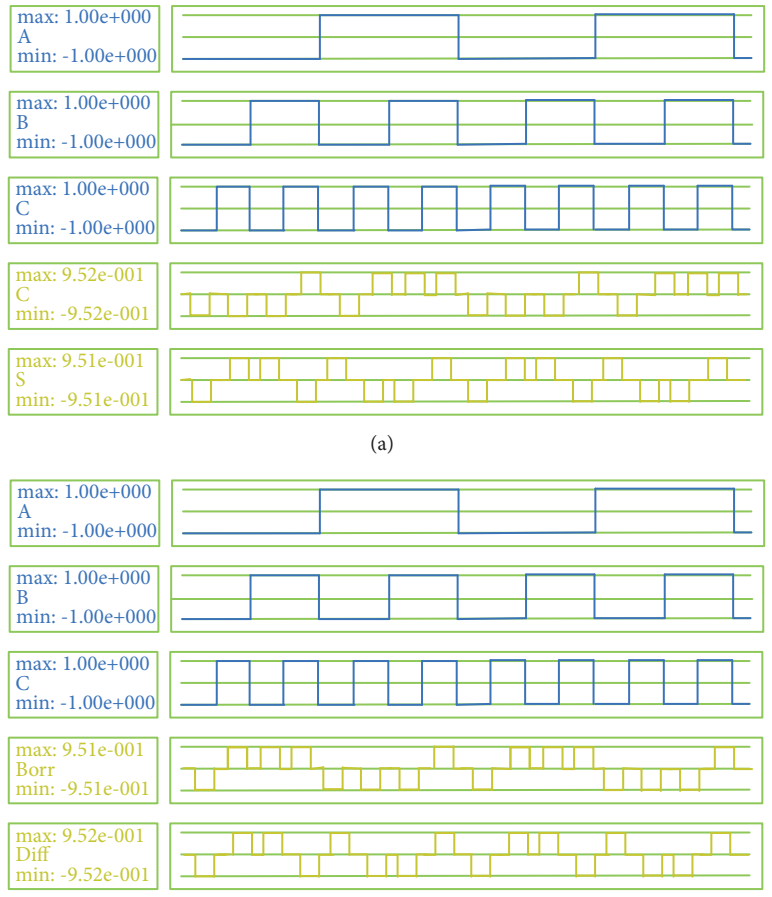

Figure 8: Simulation outcomes of the proposed designs: (a) full adder, (b) subtractor.

Table 3: Complexity study of proposed architectures.

Proposed design	XOR gate	Cell used	Covered area in μm^2	Cell area in μm^2	Area usage (%)	Latency
Full adder	1	28	0.02	0.0090	45.00	2
Full subtractor	1	27	0.03	0.0087	29.00	2

Table 4: Implementation outcomes of the proposed full adders and subtractors.

QCA architecture		Cell intricacy	Extent in μm^2	Latency	Wire crossing
Adders	Presented in [22]	93	0.09	5	Yes
	Presented in [23]	59	0.043	4	Yes
	Presented in [28]	41	0.03	4	No
	Proposed	28	0.02	2	No
Subtractors	Presented in [25]	136	0.168	7	Yes
	Presented in [26]	52	0.039	2	Yes
	Presented in [29]	233	0.132	8	Yes
	Presented in [30]	272	0.44	9	Yes
	Proposed	27	0.03	2	No

Table 5: Power dissipation in (eV) by the designed full adder.

E_bath_total (E_{btx})	E_clk_total (E_{ctx})	E_Error_total (E_{Etx})	Sum_bath (S_b)	Avg_bath (A_b)	Sum_clk (S_c)	Avg_clk (A_c)
1.95e-03	1.74e-03	-1.99e-04				
2.48e-03	-1.57e-05	-2.55e-04				
2.04e-03	1.56e-03	-2.11e-04				
1.85e-03	1.02e-03	-1.89e-04				
1.60e-03	1.02e-03	-1.61e-04	2.31e-02	2.10e-03	1.19e-02	1.08e-03
2.05e-03	1.56e-03	-2.15e-04	(Er: -2.38e-03)	(Er: -2.16e-04)		
2.47e-03	-1.58e-05	-2.56e-04				
2.19e-03	1.74e-03	-2.26e-04				
1.95e-03	1.74e-03	-1.99e-04				
2.48e-03	1.57e-05	-2.55e-04				
2.04e-03	1.56e-03	-2.11e-04				

Table 6: Power dissipation in (eV) by the designed full subtractor.

E_bath_total	E_clk_total	E_Error_total	Sum_bath	Avg_bath	Sum_clk	Avg_clk
2.48e-03	1.15e-03	2.62e-04				
1.46e-03	1.16e-03	-1.44e-04				
2.40e-03	1.77e-04	-2.46e-04				
1.99e-03	1.09e-04	-2.06e-04				
1.79e-03	1.09e-04	-1.87e-04	2.30e-02	2.09e-03	7.65e-03	6.96e-04
2.41e-03	1.77e-04	-2.53e-04	(Er: -2.37e-03)	(Er: -2.16e-04)		
1.44e-03	1.16e-03	-1.42e-04				
2.67e-03	1.15e-03	-2.81e-04				
2.48e-03	1.15e-03	-2.62e-04				
1.46e-03	1.16e-03	-1.44e-04				
2.40e-03	1.77e-04	-2.46e-04				

77, and 93% is achieved in covered area compared to the designs presented in [25], [26], [29], and [30], respectively. Moreover, the number of clock zones has reduced by 71, 75, and 77% compared to the layouts presented in [25], [29], and [30], respectively. The subtractor design does not use any cross-wiring. The overall outcomes specify that the proposed architectures are superior to earlier outline in all of the factors.

6. Power Consumption of the Proposed Architectures

An extension of QCADesigner ver. 2.0.3 is QCADesigner-E (QD-E) of Konrad Walus [27]. It performs the assessment of the power depletion of QCA logic circuits based on the study presented in [31]. It works as a simulation block that is based on the Coherence Vector Simulation Engine. Besides, QD-E is completely well-suited to QCA layouts formed with the QCADesigner ver. 2.0.3. Tables 5 and 6 present the total power dissipated by the adder and subtractor design.

In the table, E_{btx} is the figure of complete energy transfers to the bath of all cells divided for each clock cycle, E_{ctx} is the total energy moves between QCA cells and the clock divided for each clock cycle, and E_{Etx} is for each clock cycle the figure of all errors of the cells energy assessment. The error follows from the theory that the total of all energy movements of a QCA cell is zero over an entire clock cycle, where error = E_{bath} - (E_{clock} + E_{IO}). As well, S_b is the sum of total energy transfers to the bath through the entire simulation and S_{bE} is the associated error. A_b is the average standards of the energy moves to the bath and the error for every clock cycle. S_c is the figure of the energy moves to or from the clock throughout the entire simulation, whereas A_c is the average energy movement through a clock cycle. To complete the entire simulation process, the adder takes 7 iterations and the subtractor takes 6 complete simulations.

Evaluation of the temperature influence on the output polarization of outlined designs is performed and the output polarization is apprehended at different temperature by QCADesigner tool. The average output polarization (AOP) for each QCA cell is evaluated from [32] and organized in Figure 9. Both architectures operate competently in the temperature range of 1-10 K, and the AOP for each cell is slightly changed in this measure. The AOP is measured in Joule (J).

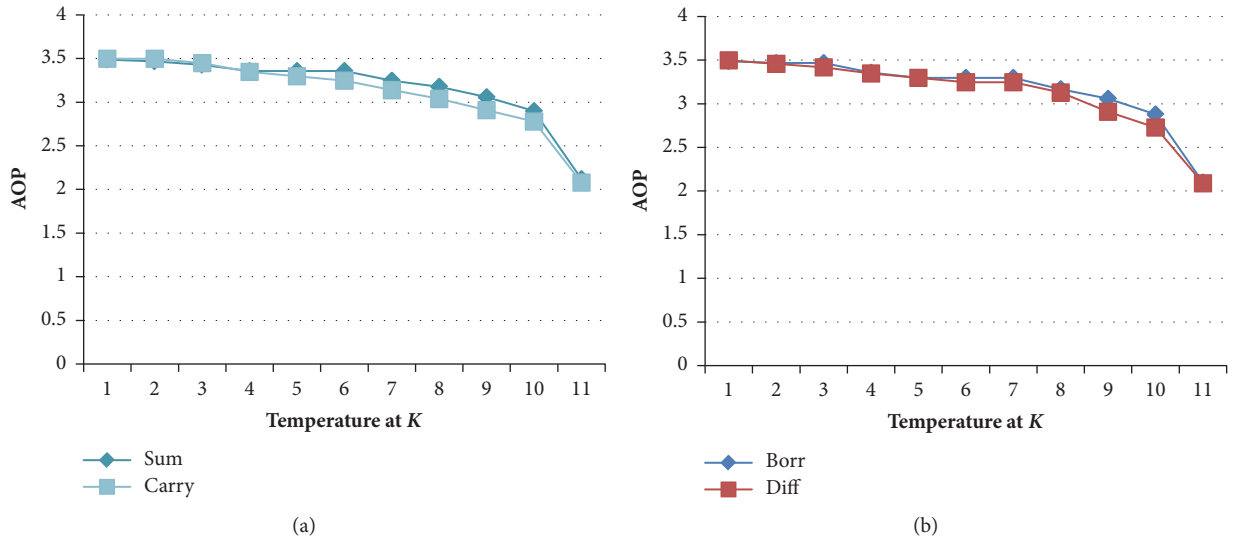

Figure 9: Temperature concern on AOP of designed (a) full adder and (b) full subtractor.

Table 7: Comparison of dissipated power by the proposed and existing circuits.

Design		Sum_bath	Avg_bath	Sum_clk	Avg_clk
Adders	layout in [22]	3.52e-02 (Er: -3.08e-03)	3.20e-03 (Er: -2.80e-04)	-1.39e-02	-1.26e-03
	layout in [23]	2.16e-02 (Er: -1.93e-03)	1.97e-03 (Er: -1.75e-04)	8.60e-03	7.82e-04
	layout in [28]	3.00e-02 (Er: -2.87e-03)	2.73e-03 (Er: -2.61e-04)	-7.85e-03	-7.13e-04
	Proposed layout	2.31e-02 (Er: -2.38e-03)	2.10e-03 (Er: -2.16e-04)	1.19e-02	1.08e-03
Subtractors	layout in [25]	7.46e-02 (Er: -7.27e-03)	6.78e-03 (Er: -6.61e-04)	-2.12e-02	-1.93e-03
	layout in [26]	2.28e-02 (Er: -2.26e-03)	2.07e-03 (Er: -2.05e-04)	2.26e-02	2.06e-03
	layout in [29]	4.91e-02 (Er: -3.80e-03)	4.46e-03 (Er: -3.45e-04)	-3.25e-02	-2.96e-03
	layout in [30]	6.35e-03 (Er: -6.97e-04)	5.77e-04 (Er: -6.33e-05)	1.63e-02	1.48e-03
	Proposed layout	2.30e-02 (Er: -2.37e-03)	2.09e-03 (Er: -2.16e-04)	7.65e-03	6.96e-04

A comparison of power dissipation among proposed and existing designs is presented in Table 7. The outlined circuits dissipated very low power compared to existing designs.

7. Conclusion

New full adder and subtractor based on XOR gate are organized in this work. The proposed architectures are used to acquire the high-performance logic element and it gets robustness and adeptness through the attained outcomes. The outlined single layer architectures are expressively more robust than the typical full adder and subtractor. This study has exhibited the new full adder and subtractor layout that can be applied to a competent building unit for higher blocks to design more complex circuit in the future. For the first time, QD-E is utilized in this work to estimate total power dissipation of QCA architectures. An n-bit adder is acquired by connecting the designed QCA full adder; in this respect, the employed hardware is reduced by occupying the regular clocking configuration and parallel arrangement of the original procedure.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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