

Research Article

Semianalytical Modelling and 2D Numerical Simulation of Low-Frequency Noise in Advanced N-Channel FDSOI MOSFETs

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Thorough investigations of the low-frequency noise (LFN) in a fully depleted silicon-on-insulator technology node have been accomplished, pointing out on the contribution of the buried oxide (BOX) and the Si-BOX interface to the total drain current noise level. A new analytical multilayer gate stack flat-band voltage fluctuation-based model has been established, and 2D numerical simulations have been carried out to identify the main noise sources and related parameters on which the LFN depends. The increase of the noise at strong inversion could be explained by the access resistance contribution to the $1/f$ noise. Therefore, considering uncorrelated noise sources in the channel and in the source/drain regions, the total low-frequency noise can simply be obtained by adding to the channel noise the contribution of the excess noise originating from the access region (Δr). Moreover, only two fit parameters are used in this work: the trap volumetric density in the BOX, and the $1/f$ access noise level originating from the access series resistance, which is assumed to be the same for the front and the back interfaces.

1. Introduction

Fully Depleted (FD) Silicon-On-insulator (SOI) is considered as one of the candidates for the future sub 14 nm CMOS generations. The use of ultrathin body and thin buried oxide (UTBB) enables to enhance the technology scalability, providing a very good control of the short-channel effect (SCE), as well as back-to-front gate coupling effects useful for threshold voltage V_{th} control with efficient body bias effect [1, 2].

The study of low-frequency noise (LF) in the UTBB FDSOI is of great interest because it is a key issue for the technology evaluation for identifying the traps possibly introduced during the device processing. Moreover, it is not only limiting the analog circuit operation, but it should also jeopardize the digital circuit functioning for aggressively scaled devices.

The analysis of LF noise in FD-SOI devices is a more complicated task compared to their bulk ancestors. In SOI instead of one interface, as in bulk devices, there are two interfaces, the so-called front and back ones, that can

influence the noise behaviour due to the strong electrostatic coupling between them.

It is now well accepted that the LF $1/f$ noise in FDSOI and multigate devices mostly stems from the fluctuations of the inversion charge nearby the two interfaces [3–11]. For UTBB devices, the gate oxide thickness reaches dimensions as small as nanometers, leading to larger surface roughness scattering playing an important role on carrier mobility and drain current fluctuations [12].

Many studies in the past have already emphasized that the LFN should be affected by the coupling effect between the back and the front interfaces [3–11], but none of them has shown precisely by means of 2D numerical simulation the contribution of each interface on the measured total drain current noise, depending on the biasing conditions and various effective gate lengths.

In this work, our aim is first to present a rigorous investigation of the impact of back/front interface coupling effect on the low-frequency noise in UTBB FDSOI structures. For that purpose, we extend the existing carrier number fluctuations with correlated mobility fluctuations

(CNF+CMF) model [11], by considering a multilayer front gate stack with existing traps in both high-k (HK) layer and an interfacial layer (IL), which are uniformly distributed in the energy gap and space.

This new model, although simple, is applied successfully to strongly coupled FDSOI devices, including correlated mobility fluctuations for the channel noise and the access noise originating from the Source and Drain regions (CNF+CMF+ Δr), thus significantly going beyond previous works [3–11].

2. Experimental Details

The MOS devices used in this study are n-channel FDSOI fabricated by ST Microelectronics (France) with interfacial layer/high-k (IL-HK) and metal gate which were made on (100) SOI wafers with 25 nm BOX. The silicon film thickness under the gate is 7 nm. The IL-HK gate oxide stack has a capacitance equivalent thickness (CET) of about 1.6 nm [13]. The gate mask width is 1 μm , and mask gate length is varying from 30 nm to 1 μm . A typical cross section of the FDSOI structure is shown in Figure 1 [13].

Static I–V measurements were carried out as a function of drain and gate voltages using an HP 4156b semiconductor parameter analyzer. The FDSOI parameters have been extracted in linear regime ($V_d = 20$ mV) using the McLarty technique [14], especially designed for extracting the MOSFET parameters with strong mobility degradation quadratic factor θ_2 . In addition, the C–V measurements were taken out from HP 4294A impedance-meter with a 40 mV small signal at 1 MHz, which allows extraction of the gate length reduction $\Delta L = 15$ nm for such devices [15].

The LF noise measurements were carried out at room temperature using a programmable Pin-Probe Noise Measuring System (3PNMS) with Elite 300 probe station. The noise measurement bandwidth is from 1 Hz to 10 kHz. Note that the noise data below 10 Hz are not meaningful due to AC filtering in the noise measuring system.

3. Static Characterization of FDSOI Devices

With the front gate conduction mode, in linear region, the drain current for front gate (noted as 1), operated from weak to strong inversion, is given by

$$I_{d1} = \frac{W}{L} \cdot \mu_{\text{eff}1} \cdot Q_{i1} \cdot V_d, \quad (1)$$

where W and L are the effective channel width and length, respectively, Q_{i1} is the inversion charge density, $\mu_{\text{eff}1}$ is the effective mobility, and V_d is the drain voltage.

In order to consider either surface roughness effects which increase rapidly with vertical field, phonon scattering effects, and series resistance effects, the effective mobility $\mu_{\text{eff}1}$ can be expressed as [12]

$$\mu_{\text{eff}1} = \frac{\mu_0}{1 + \theta_1(V_{g1} - V_{\text{th}1}) + \theta_2(V_{g1} - V_{\text{th}1})^2}, \quad (2)$$

where μ_0 is the low field mobility, θ_1 and θ_2 are the mobility degradation parameters, and $V_{\text{th}1}$ is the threshold voltage.

Table 1 illustrates static parameters for 0 V back gate, extracted for various mask gate lengths L_M and gate mask width W_M of 1 μm . It is worth noting that the mobility degradation parameter θ_1 is affected by series resistance and is given by the following relation [16]: $\theta_1^* = \theta_1 + G_m \cdot R_{\text{SD}}$, where $G_m = C_{\text{ox}} \mu_0 W/L$. Therefore, the plot of θ_1^* as a function of G_m give a straight line, from which the slope provides parasitic resistance R_{SD} and y-axis intercept factor θ_1 . Note that, looking at Table 1, the negative value of θ_1 is representative of an increasing mobility at small gate voltage drive due to significant Coulomb scattering contribution [12]. Moreover, θ_2 varies only on a very small range between 0.521 and 0.667, leading to a quasicontant surface roughness effects for the transistors various gate lengths (L_m (nm) = 30, 35, 40, 120, 300, 1000), and a fixed gate width ($W_m = 1$ μm).

4. Low-Frequency Noise in FDSOI Devices at Ohmic Operation

4.1. Semianalytical (CNF+CMF+ Δr) 1/f Noise Model. By using the flat-band voltage fluctuations theory [17], $\delta V_{\text{fb}1,2} = -\delta Q_{\text{ox}1,2}/C_{\text{ox}1,2}$ due to the oxide and/or interface charge fluctuations $\delta Q_{\text{ox}1,2}$ as well as to the effective mobility fluctuations $\delta \mu_{\text{eff}1,2}$, and also taking into account the access series resistance fluctuations, one gets for the drain current variations δI_d for each interface [8, 10, 12]:

$$\begin{aligned} \delta I_d = & \delta V_{\text{fb}1,2} \cdot \frac{\partial I_d}{\partial V_{\text{fb}1,2}} \Big|_{\mu_{\text{eff}1,2}, R_{\text{SD}}} + \delta \mu_{\text{eff}1,2} \cdot \frac{\partial I_d}{\partial \mu_{\text{eff}1,2}} \Big|_{V_{\text{fb}1,2}, R_{\text{SD}}} \\ & + \delta R_{\text{SD}1,2} \cdot \frac{\partial I_d}{\partial R_{\text{SD}1,2}} \Big|_{V_{\text{fb}1,2}, \mu_{\text{eff}1,2}}. \end{aligned} \quad (3)$$

The effective mobility $\mu_{\text{eff}1,2}$ is given by [10]

$$\frac{1}{\mu_{\text{eff}1,2}} = \frac{1}{\mu_{\text{eff}01,2}} + \alpha_{1,2} \cdot Q_{\text{ox}1,2}, \quad (4)$$

where $\alpha_{1,2}$ is the Coulomb scattering parameter. Knowing that the transconductance definition is $g_{m1,2} = \delta I_d / \delta V_{g1,2} = -\delta I_d / \delta V_{\text{fb}1,2}$, equations (7a)–(8) yield

$$\begin{aligned} \delta I_d = & \left(1 + \alpha_{1,2} \mu_{\text{eff}1,2} \cdot C_{\text{ox}1,2} \frac{I_d}{g_{m1,2}} \right) \cdot g_{m1,2} \cdot \delta V_{\text{fb}1,2} \\ & + \left(\frac{I_d}{V_d} \right) \cdot \delta R_{\text{SD}1,2}. \end{aligned} \quad (5)$$

After accounting for the noise in the access resistance as in [18], the normalized spectral density of drain current can then be expressed as [8, 10]

$$\begin{aligned} \frac{S_{I_d}}{I_d^2} = & S_{V_{\text{fb}1,2}} \left(\frac{g_{m1,2}}{I_d} \right)^2 \left(1 + \alpha_{1,2} \mu_{\text{eff}1,2} \cdot C_{\text{ox}1,2} \frac{I_d}{g_{m1,2}} \right)^2 \\ & + \left(\frac{I_d}{V_d} \right)^2 \cdot S_{R_{\text{SD}1,2}}, \end{aligned} \quad (6)$$

where $S_{R_{\text{SD}1,2}}$ is the power spectral density (PSD) of source-drain series resistance for front and the back gate interfaces.

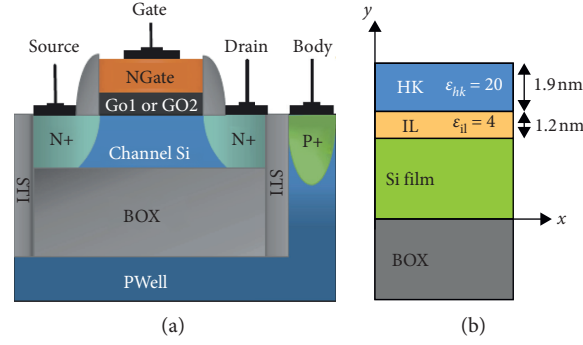


FIGURE 1: (a) Typical structure of 14 nm NMOS FDSOI device featuring a gate stack TiN on bilayer oxide HfSiON + SiON with Si channel and P-Well substrate. (b) Two-dimensional bilayer FDSOI structure.

TABLE 1: Extracted main static MOSFET parameters (Uncertainty estimation: $\pm 5\%$).

L_m (nm)	μ_0 (cm ² /V.s)	Θ_1^* (1/V)	Θ_2 (V ⁻²)	V_{th} (V)	$R_{sd} W_M$ (Ω -cm)
1000	147.66	-0.548	0.667	0.33	$125 \cdot 10^{-4}$
300	145.00	-0.436	0.659	0.334	"
120	142.36	0.083	0.521	0.333	"
40	74.93	0.458	0.521	0.297	"
35	67.30	0.193	0.619	0.265	"
30	59.66	0.081	0.636	0.237	"

Since the access resistance R_{SD} is the same for interface 1 and 2, then $S_{Rsd1} = S_{Rsd2} = S_{Rsd}$.

As the multilayer front gate stack contains a high-k layer (HK), and an oxide interfacial layer (IL), traps are in both layers, so the tunnelling distance and trap volumetric density should be considered accordingly. Hence, the flat-band spectral density is split into two terms, each referring to a given layer. Thereby, our new model is modified in order to include the effect of both gate stack layers having different charge centroid such as

$$S_{Vfb1} = \frac{q^2 \cdot N_{t1,il} \cdot kT \cdot \lambda_{il}}{f \cdot W \cdot L \cdot C_{ox1}^2} + \frac{q^2 \cdot N_{t1,hk} \cdot kT \cdot \lambda_{hk}}{f \cdot W \cdot L \cdot C_{1,hk}^2}, \quad (7a)$$

$$S_{Vfb2} = \frac{q^2 \cdot N_{t2} \cdot kT \cdot \lambda_{il}}{f \cdot W \cdot L \cdot C_{ox2}^2}, \quad (7b)$$

where $C_{1,hk}$ refers to the capacitance of the HK layer, $N_{t1,ox}$ is the volumetric oxide trap densities in the oxide interfacial layer, $N_{t1,hk}$ the volumetric oxide trap densities in the high k dielectric layer, N_{t2} is the volumetric oxide trap density in the BOX, λ_{il} and λ_{hk} are the tunnelling distances in the oxide IL and KH layer, respectively, q is the electron charge, kT is the thermal energy and f is the measuring frequency. In our 2D simulations analysis, we have assumed that N_{t2} is equal to $N_{t1,il}$ because the BOX is a pure silicon oxide as the IL. Furthermore, the traps are considered uniformly distributed in energy. The front gate stack consists of TiN/Hf-based oxide dielectric with equivalent oxide thickness $t_{ox} = 1.6$ nm, while the silicon film thickness t_{Si} is 7 nm, and the BOX thickness is 25 nm [13].

5. 2D Numerical Simulation

5.1. FDSOI Devices under Study. To verify the accuracy of the proposed semianalytical (CNF + CMF + Δr) $1/f$ noise model, the electric potential V , and the quasi-Fermi level U_c distribution, within the silicon film (Si), both along the channel (x -direction), and along the depth of the Si film (y -direction), are simulated using FlexPDE software, which solves partial differential equations based on finite elements method [19]. The program solves numerically the 2D Poisson equation coupled to drift-diffusion current continuity equations, within a specific mesh, and corresponding boundaries conditions of the structure described in Figure 1(b). Quantum confinement effects for the carriers within the two interfaces are taken into account thanks to the H ansch model adapted to the FDSOI structure [20].

For an appropriate comparative study, three devices with a gate width equal to $1 \mu m$ and different effective channel lengths ($L = 985, 105$, and 15 nm). Based on the extracted parameters of Table 1, the 2D simulation results of $I_{ds}-V_{gs}$ characteristics is shown in Figure 2 and exhibit very good agreement with experimental data.

Note from Figure 2(b) that the 2D potential distribution of the shortest transistor induces unwanted short-channel effect such as degradation of $I_{ds}-V_{gs}$ transfer characteristics below threshold voltage. In addition, the rising contribution of series resistance causes a drastic decrease in mobility, by impacting the intrinsic factor θ_1 . Therefore, reducing the series resistance of the source-drain junction is a major concern for improving the performance of the advanced FDSOI MOSFET.

5.2. 2D Numerical Modelling of Remote Coulomb Scattering. In order to account for CMF in (4), it is suitable to consider the remote Coulomb scattering (RCS) parameter, across the silicon film, proper for each interface. Thus, we consider the RCS coefficient $\alpha_{1,2}$ for both interfaces given by [21]

$$\alpha_1 = \alpha_0 \cdot \left(1 + \frac{y}{\lambda_c} \right)^{-2}, \quad (8)$$

$$\alpha_2 = \alpha_0 \cdot \left(\frac{\lambda_c + y}{\lambda_c + t_{SI} - y} \right)^{-2},$$

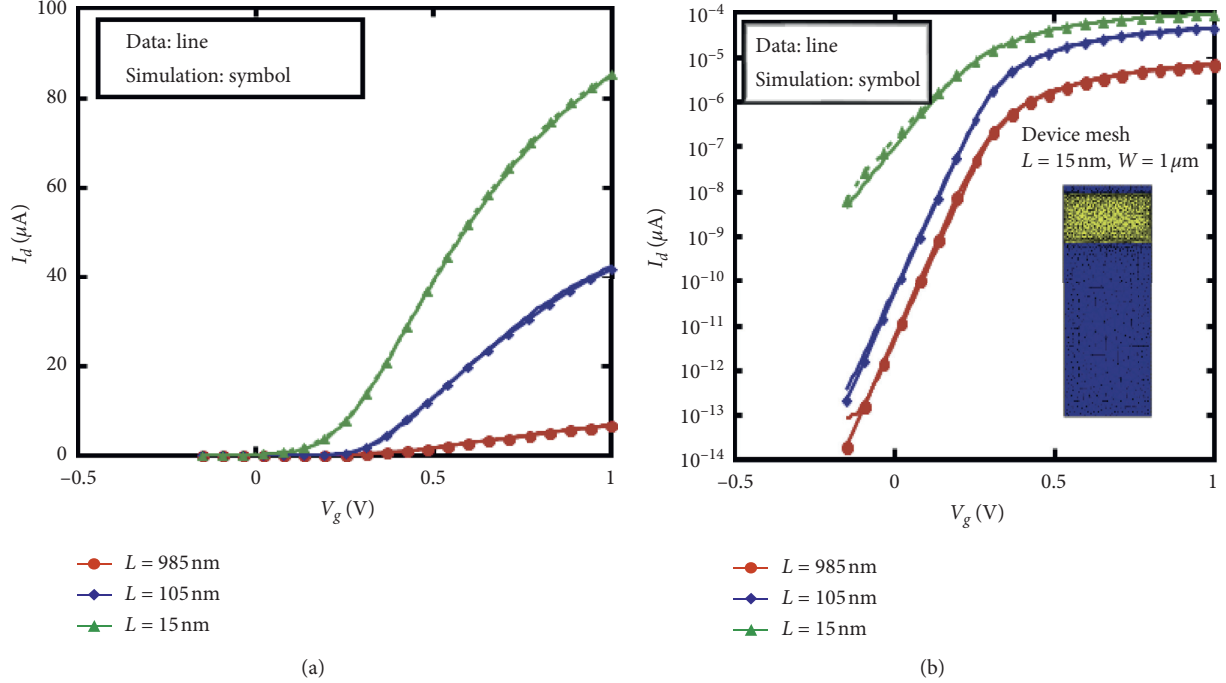


FIGURE 2: 2D simulation results of I_{ds} - V_{gs} characteristics for various gate effective lengths and $W_m = 1 \mu\text{m}$. Graph (a) is the linear variations, and graph (b) is semilogarithmic variations, the insert is the meshed structure of FDSOI ($L = 15 \text{ nm}$).

where a_0 is approximately 10^5 Vs/C for this UTBB SOI technology [21], and $\lambda_c = 1.2 \text{ nm}$, y is the average distance between the inversion charge distribution centroid and the front interface, whereas $t_{SI} - y$ is the distance of the inversion charge distribution centroid from the back interface.

A clear overview of the RCS factors variations as a function of V_{FG} are shown in Figure 3. Since the front gate conduction mode is considered, the charge is mostly concentrated near the front interface, giving rise to an increase of α_1 , as much as the transistor is shorter (Figure 3(a)). Regarding α_2 (Figure 3(b)), on the contrary, it decreases as much as the size of the transistor is smaller, when V_{FG} goes from weak to strong inversion. Thus, antagonistic roles are played by α_1 and α_2 in this front gate mode of operation, giving rise to α_1 values, which are, at least, an order of magnitude greater than those of α_2 .

Therefore, Figure 4 shows $\alpha_{1,2}$ RCS parameters from which a strong coupling effect between the two interfaces is evidenced, even when the back gate is grounded ($V_{BG} = 0 \text{ V}$).

5.3. 2D LF Noise Numerical Results and Discussion. The noise measurements was carried out for various devices from 1 Hz to 10 KHz, with drain voltage $V_d = 20 \text{ mV}$ and gate voltage varied from weak to strong inversion. Figure 4 illustrates typical $1/f$ normalized drain current PSD for NMOS FDSOI with effective gate length $L = 105 \text{ nm}$, and for different V_{GF} , and $V_{GB} = 0 \text{ V}$. The general LFN behaviour exhibits $1/f'$ behaviour, with γ exponent ≈ 0.9 – 1.1 , for all the range of V_{GF} going from 0.15 V to 0.65 V , for frequency lower than 100 Hz , and for not very short-channel devices.

At first sight, the normalized drain current noise versus drain current characteristics (Figure 5(a)) measured in front

gate mode follows the overall evolution of the squared transistor gain $(g_{m1,2}/I_{d1,2})^2$ [17, 18], indicating that the LF noise can mostly be interpreted by CNF noise model.

Figure 5(b) illustrates the corresponding front input-referred voltage noise and following the general S_{Id}/g_{m1}^2 tendency. Previous works have shown that the LF noise in FDSOI devices should be influenced by coupling effect between back and front interfaces [3–11]. Due to this coupling, it is difficult to predict precisely the contribution of each interface on the measured overall noise level, or contribution of back interface with respect to that of front interface. Therefore, analytical study of the noise sources and their dependence on the bias conditions is critical for the UTBB FDSOI MOSFETS.

In order to show and discuss the 2D numerical simulation results of LF noise, it is suitable to input from Table 2 the main parameters which are required by the TCAD tool. In fact, only two fitting parameters are used in this study in order to fit the experimental data. The parameters N_{t1} for each transistor are taken from [10, 13], while the corresponding N_{t2} are used as fitting parameters. The second fitting parameter is the access resistance noise level K_r .

We can notice that the volumetric trap density associated to IL/HK layer is approximately two orders of magnitude higher than the ones associated to the BOX layer, which is widely reported in many papers [3–10, 22, 23], in state-of-the-art devices.

Our aim is to compare the two 2D numerical LF noise models (CNF + Δr) and (CNF + CMF + Δr), on one hand, and, on the other hand, the semianalytical model, which is based on equations (1)–(7b) of Section 4, with experimental data. Note that the two models include the LF noise

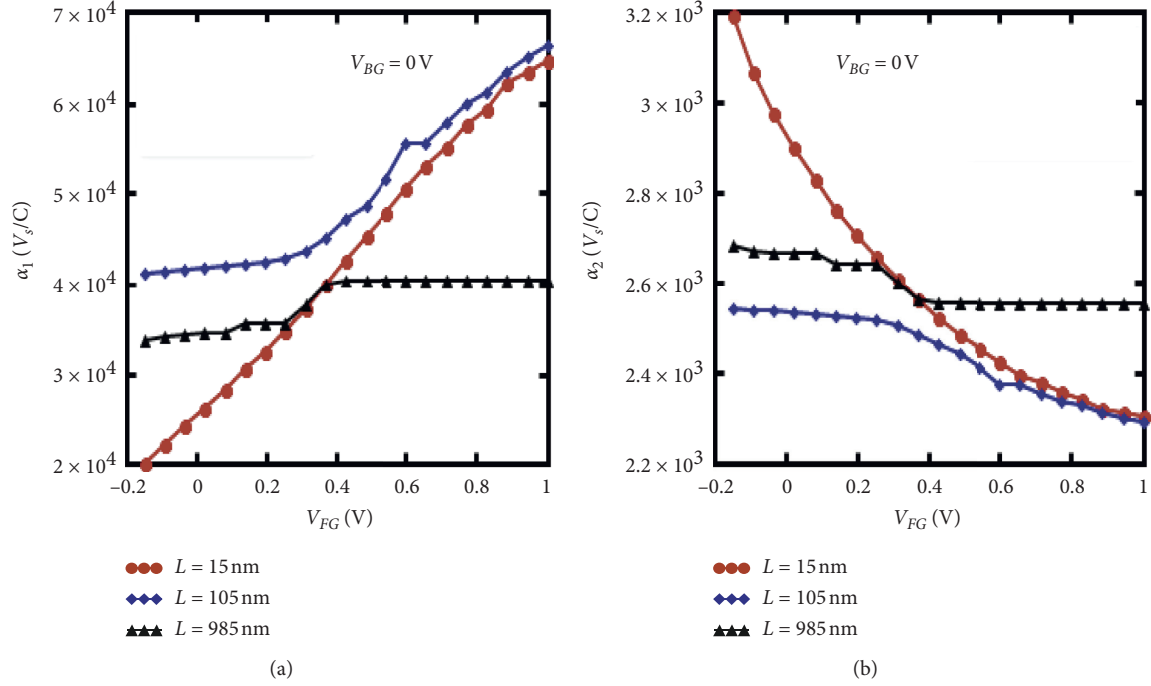


FIGURE 3: Numerical calculation results of RCS factors for (a) front gate interface, and (b) back gate interface, versus front gate voltage V_{FG} , for various effective gate lengths, and fixed $W = 1 \mu\text{m}$, with $V_{BG} = 0$ V and $V_d = 20$ mV.

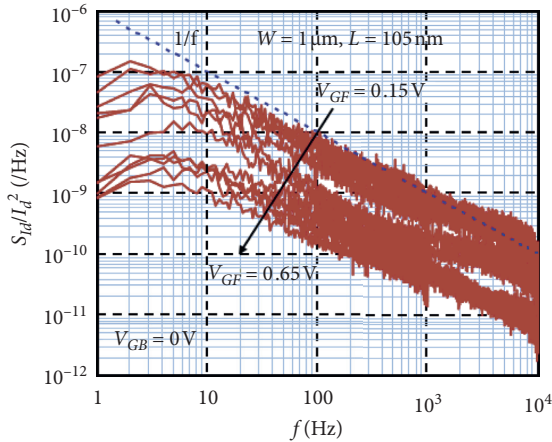


FIGURE 4: Normalized drain current power spectral density under front gate mode, for nMOS FDSOI with $W = 1 \mu\text{m}$ and $L = 105$ nm.

originated from the access series resistance R_{SD} , whose impact should become increasingly important for next generations, sub 10 nm FDSOI devices.

Figure 6 represents the normalized current noise spectral density (S_{Id}/I_d^2) for the front channel, where (a) 2D numerical models (CNF+ Δr), and (b) (CNF+CMF+ Δr) are both compared to data, whereas in (c), the semianalytical model is also compared to data.

As indicated in equation (6), a very important parameter for flicker noise analysis in MOSFETs is the squared transistor gain $(g_{m1,2}/I_d)^2$, computed here in 2D simulation for front gate operation, with $V_{BG} = 0$ V, as a function of drain current. As it is usual, it exhibits (Figure 6) a plateau in weak

inversion, before dropping above threshold in strong inversion, indicating that the LF noise is due fundamentally to carrier number fluctuations [17, 18].

Furthermore, a very useful parameter in FDSOI devices is the coupling factor c_2 which expresses the relative impact of each interface on LF noise level. It is given by [3, 4, 8–10]

$$c_2 = \left(\frac{g_{m2}}{g_{m1}} \right)^2. \quad (9)$$

As it can be seen from Figure 7, the coupling factor c_2 is about 1.24 and 1.15 at drain current $I_{d1} = 5 \mu\text{A}$, for devices with gate length $L = 105$ nm, and 985 nm, respectively, with the back interface biased in depletion mode, whereas the front interface goes from weak to strong inversion. This feature points out the great importance of the back interface LF noise contribution. Moreover, we can notice that c_2 decreases very quickly for the shortest device passing from about 0.49 at $I_{d1} = 5 \mu\text{A}$, to 0.03 at $80 \mu\text{A}$, indicating that the short-channel effects may affect the back LF noise contribution, making it less predominant at strong inversion. However, for a better understanding, the latter observation needs to be validated by other experiments and simulations on different advanced FDSOI devices.

Thus, although the coupling factor c_2 , at $I_{d1} = 5 \mu\text{A}$, appears to be lying between 1.24 and 1.12 for the effective gate lengths $L = 105$ nm and $L = 985$ nm, respectively, it becomes more important when multiplied by the S_{Vfb2}/S_{Vfb1} ratio, showing the importance of the coupling effect in these devices, when the front interface is stepping from weak to strong inversion, and the back interface is biased at zero volt.

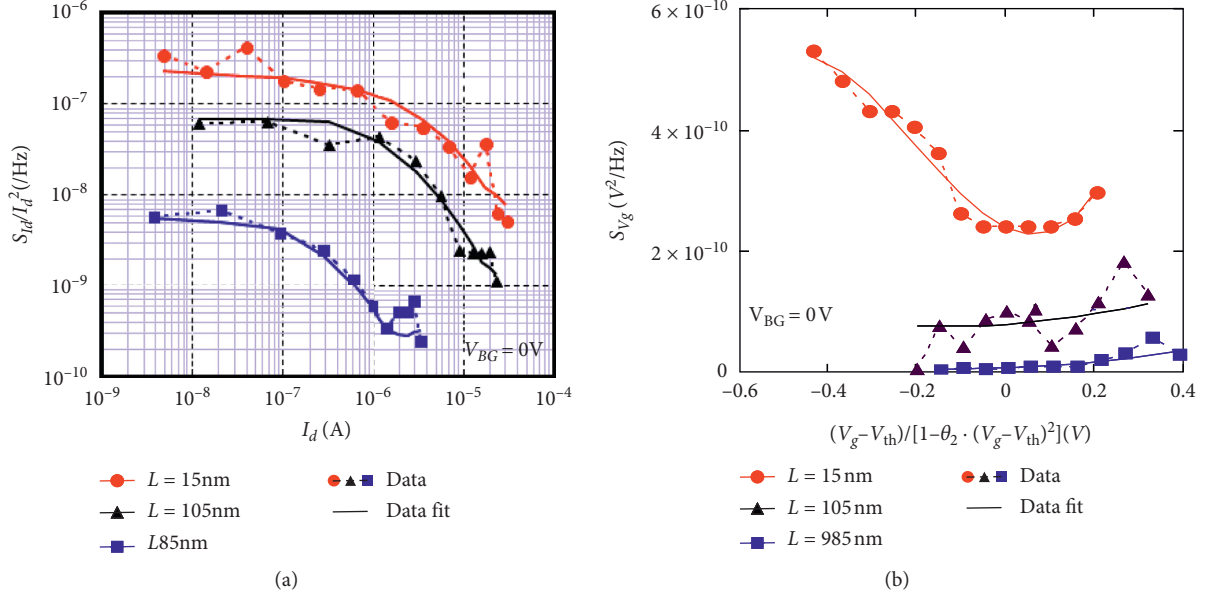


FIGURE 5: (a) Plots of S_{Id}/I_d^2 experimental data versus I_d , at frequency 10 Hz, and in front gate mode and (b) plots of S_{Vg} experimental data versus $(V_g - V_{th})/[1 - \theta_2 \cdot (V_g - V_{th})^2]$ with corresponding data fit lines.

TABLE 2: Extracted main noise fitting parameters (uncertainty estimation: $\pm 5\%$).

L(nm)	N_{t1} (/eV/cm ³)	N_{t2} (/eV/cm ³)	Kr
985	2.53×10^{17}	1.15×10^{15}	2×10^{-7}
105	2.29×10^{17}	1.55×10^{15}	1×10^{-8}
15	1.43×10^{17}	2.75×10^{15}	5×10^{-7}

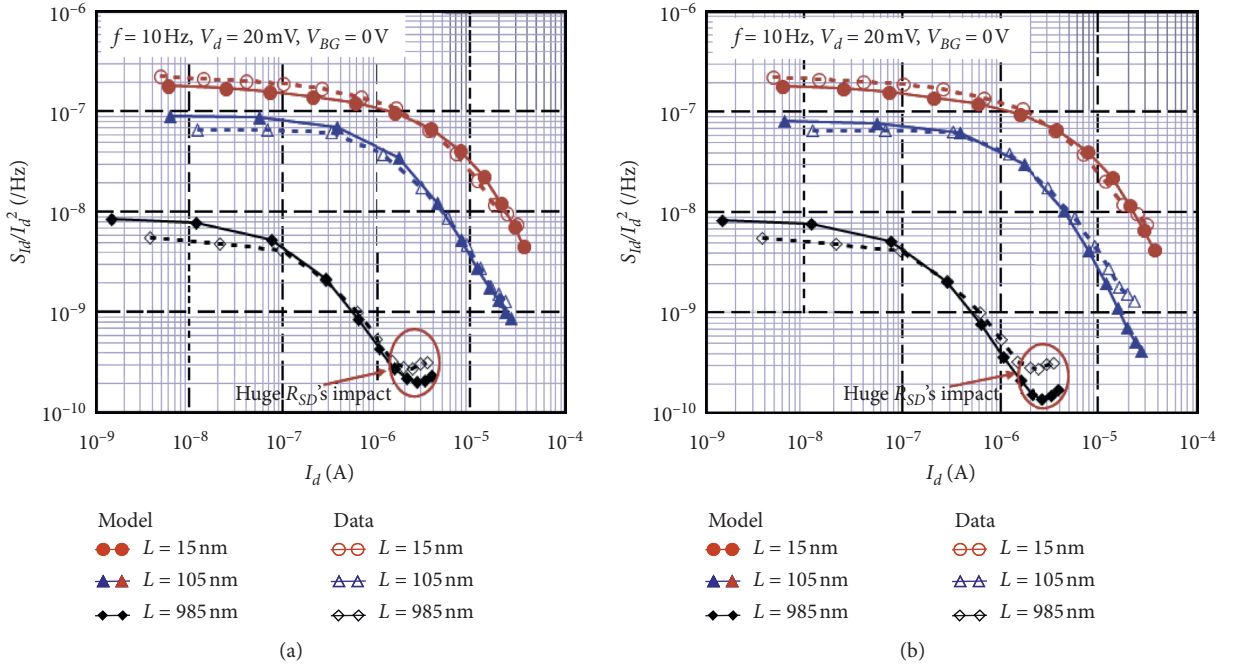


FIGURE 6: Comparison of experimental normalized drain current PSD versus I_d with (a) CNF + CMF + Δr , 2D numerical simulation results, with RCS parameters, and with (b) CNF + CMF + Δr , semianalytical model results for 14 nm FDSOI samples, for some effective gate lengths.

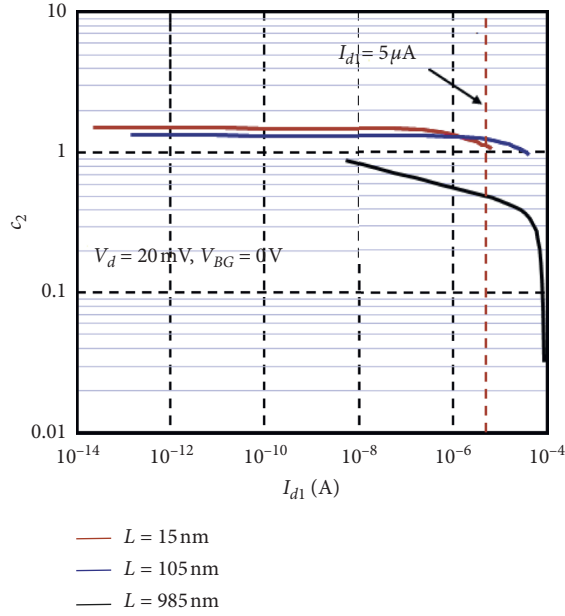


FIGURE 7: Coupling factor c_2 for various gate lengths as a function of drain current I_{d1} , at $V_d = 20$ mV and $V_{BG} = 0$ V.

Looking at Figure 7, it will be noted that, in general, the coupling factor c_2 tends to decrease as a function of the I_{d1} current, showing that, in strong inversion, the decoupling of the back interface becomes more and more important. This effect is even more pronounced for the shorter transistor. However, when operating in back gate mode, this situation is reversed completely, and the back gate contribution becomes more significant at strong inversion.

Regarding Figure 6, the two 2D numerical simulations results from CNF + CMF + Δr , and CNF + Δr models, and the semianalytical model based on the CNF + CMF + Δr model are presented. Thus, using RCS formulation of equation (8) in the CNF LF noise model of equation (6) leading to CNF + CMF noise model, on one hand, and including also LF noise originated from the access series resistance R_{SD} , on the other hand (CNF + CMF + Δr), the variations of S_{Id}/I_d^2 with drain current are well described, and agree perfectly well with the experimental data.

Recalling that only two physical entities are used as fitting parameters, the other parameters are either taken from Tables 1–3 or extracted from experimental data. Using these parameters also enables to describe well the dependence of the normalized drain current noise S_{Id}/I_d^2 as a function of drain current I_d for V_g varying from weak to strong inversion regions as shown in Figure 6. Note that the buried oxide traps which are lying in the range of $1\text{--}3 \times 10^{15}/\text{eV}/\text{cm}^3$ are extremely low, confirming the very good quality of a pure thermal oxide, and the front interface traps density are almost two decades higher due to the IL/high-k/metal gate stack [3–10, 22, 23].

For the sake of the modelling precision, Figure 8 shows the comparison between experimental plots of S_{Vg} versus $(V_g - V_{th})/[1 - \theta_2 \cdot (V_g - V_{th})^2]$ with (a) CNF + CMF + Δr , 2D numerical simulation results, with RCS parameters, and (b)

TABLE 3: Data of coupling factor c_2 weighted by S_{Vfb2}/S_{Vfb1} for various gate lengths (Uncertainty estimation: $\pm 5\%$).

L (nm)	c_2 (at $I_{d1} = 5 \mu\text{A}$)	S_{Vfb2}/S_{Vfb1}	$c_2 \times (S_{Vfb2}/S_{Vfb1})$
985	1.15	51.96	59.75
105	1.24	77.16	95.68
15	0.49	215.78	105.73

with the corresponding semianalytical model, just as in Figure 7.

We can notice that the 2D simulation corresponding to Figure 8(a) is very similar to the model corresponding to Figure 8(b) and presents the best results for the overall tested devices.

At the lowest applied front gate voltage ($V_g < V_{th}$), the total input-referred noise S_{Vg} for $L = 105$ nm and $L = 985$ nm is quasiconstant, clearly indicating that the carrier number fluctuations due to carrier trapping in the oxide layer dominate the $1/f$ noise [17, 18]. The increase of the noise in strong inversion could be explained by the correlated mobility fluctuations (CNF + CMF). The huge rise in noise level can be attributed to the influence of the access series resistance R_{SD} [18]. For the shortest device, one can notice a decrease in the noise level in weak inversion, and this feature is probably due to the importance of coupling factor c_2 weighted by S_{Vfb2}/S_{Vfb1} as shown in Table 3.

5.4. Front Interface Noise Level to the Total Noise Level Ratio R_1 . Figure 9 illustrates the R_1 factor defined as the ratio of contribution of the front interface noise level to the total noise level ones: $(S_{Id}/I_d^2)_1/(S_{Id}/I_d^2)_{\text{tot}}$, according to the (CNF + Δr) model (Figure 9(a)), and then according to (CNF + CMF + Δr) model (Figure 9(b)).

In Figure 9(a), for the CNF + Δr model, it can be seen that for all channel geometries, the ratio R_1 varies between 0.1% in weak inversion, up to about 50% in strong inversion, showing a more significant contribution of the front interface, at high gate voltage, but without exceeding the noise level related to the back interface.

For the CNF + CMF + Δr model, illustrated in Figure 9(b), the situation is quite similar to that of the previous case, except that the noise contribution percentage has somewhat changed. Now it passes from 0.2% to 75%, showing that an additional 25% arises here, compared to the previous case, in strong inversion, from the correlated mobility fluctuations phenomena. These results therefore confirms the general feature of the normalized PSD at 10 Hz of the drain current fluctuations induced by each interface oxide traps density and the total normalized drain current fluctuations as is illustrated for one gate length in Figure 10, by plotting S_{Id}/I_d^2 versus drain current, in the front gate operating mode [8–10].

Figure 10 shows the normalized drain current fluctuations extracted at 10 Hz, induced by each oxide traps related to both interfaces 1 and 2, and the total normalized drain current fluctuations. These simulations were performed with volumetric trap densities and gate lengths geometries which

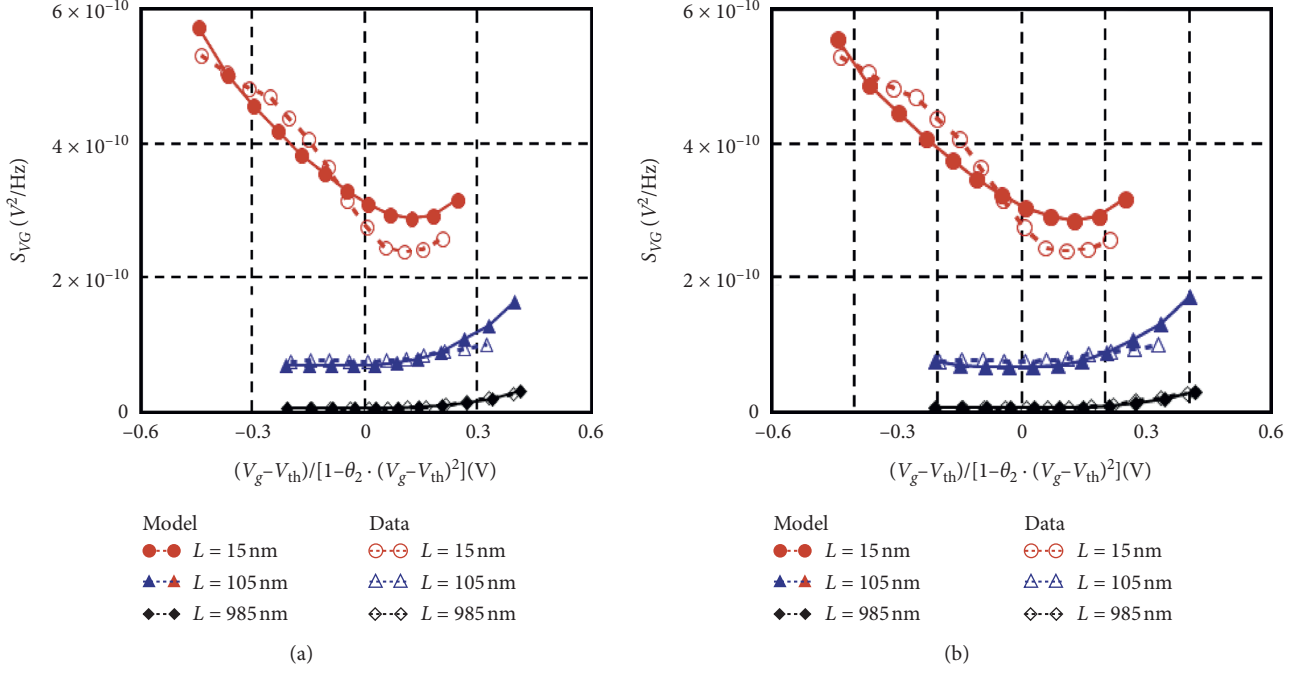


FIGURE 8: Comparison of experimental plots of S_{VG} versus $(V_g - V_{th})/[1 - \theta_2 \cdot (V_g - V_{th})^2]$ with (a) CNF + CMF + Δr , 2D numerical simulation results, with RCS parameters, and with (b) CNF + CMF + Δr , semianalytical model results for advanced FDSOI samples, with some effective gate lengths.

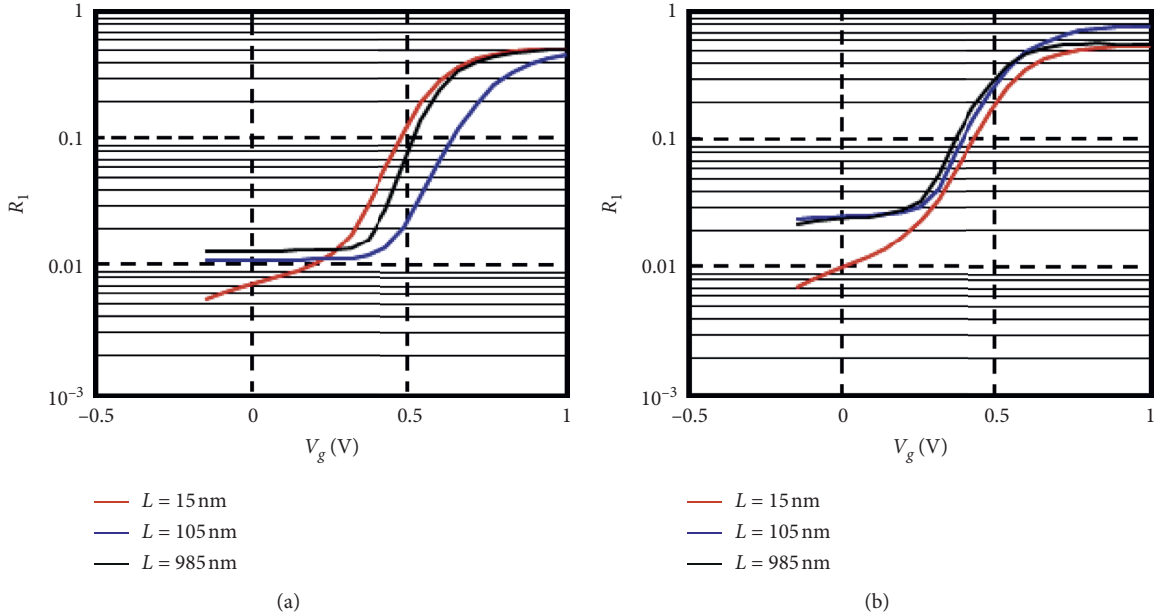


FIGURE 9: Ratio R_1 of contribution of the front interface noise level to the total noise level in the case of front channel conduction mode: (a) CNF+ Δr model and (b) CNF + CMF + Δr model.

are mentioned in Table 2. The front gate operating mode is considered.

As a result, though the front interface trap density are almost two decades higher to those of the back interface, the total noise level is completely dominated by the back interface noise contribution in the weak and intermediate

inversion operation, whereas the situation tends to reverse or at least to balance in strong inversion operation as shown in Figure 10.

Note again that the plateau observed in weak inversion, for all the studied devices, indicates that the CNF model due to carrier trapping in the oxide layer dominates, whereas in

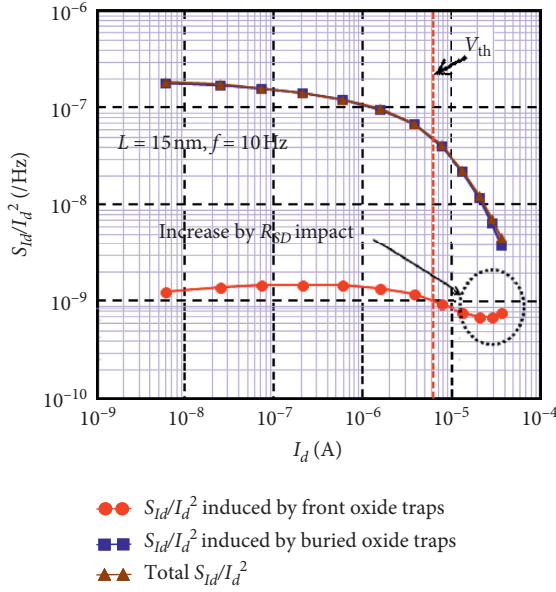


FIGURE 10: 2D numerical simulation of S_{Id}/I_d^2 , with (CNF + CMF + Δr)-based model, of front and buried oxide noise sources as a function of drain current for a gate length $L = 985$ nm. The front gate operating mode is considered.

the intermediate and strong inversion, the CNF + CMF model is more appropriate. From onset until the end of the strong inversion operation, the level noise increase is perfectly explained by the access resistance contribution to the $1/f$ noise.

6. Conclusion

A new extended $1/f$ noise model (CNF + CMF + Δr) related to double-layer high- k gate stacks devices has been formulated, considering the trap volumetric density in both IL and HK dielectric layers. The previous models [8–11] remain valid overall, but only if the IL thickness is large compared to that of the HK one, which is not the case for our studied devices.

Moreover, a detailed analysis both in semianalytical modelling and 2D numerical simulations has been carried out to identify the main noise sources and related parameters in advanced FDSOI devices. Thus, this improved semi-analytical $1/f$ noise model called (CNF + CMF + Δr) is based on the carrier number fluctuations with correlated mobility fluctuations enhanced with LF noise originated from the access series resistance R_{SD} . It has been successfully validated through experimental data and 2D numerical simulation results obtained on FDSOI devices. Finally, we have pointed out that the total noise is dominated by the buried oxide noise level contribution, for the whole voltage range of the front gate operation mode, as a result of the strong back-to-front coupling in such UTBB FDSOI devices.

Data Availability

The figure data used to support the findings of this study are not available.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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References

- [1] K. Cheng, A. Khakifirooz, N. Loubet et al., "High performance extremely thin SOI (ETSOI) hybrid CMOS with Si channel NFET and strained SiGe channel PFET," *2012 International Electron Devices Meeting*, 2012.
- [2] L. Grenouillet, M. Vinet, J. Gimbert et al., "UTBB FDSOI transistors with dual STI for a multi-Vt strategy at 20nm node and below," *2012 International Electron Devices Meeting*, 2012.
- [3] E. Simoen and C. Claeys, "The low-frequency noise behaviour of silicon-on-insulator technologies," *Solid-State Electronics*, vol. 39, no. 7, pp. 949–960, 1996.
- [4] S. Haendler, J. Jomaah, and F. Balestra, "On the $1/f$ noise in $0.15\ \mu\text{m}$ fully depleted soi/mos transistors," *Fluctuation and Noise Letters*, vol. 2, no. 3, pp. L253–L256, 2002.
- [5] M. von Haartman, J. Hallstedt, J. Seger, B. G. Malm, P. E. Hellstrom, and M. Ostling, "Low-frequency noise in SiGe channel pMOSFETs on ultra-thin body SOI with Ni-silicided source/drain," in *Proceedings of the Noise and Fluctuations: 18th International Conference on Noise and Fluctuations-ICNF*, Salamanca, Spain, September 2005.
- [6] J. El Hussein, F. Martinez, J. Armand et al., "New numerical low frequency noise model for front and buried oxide trap density characterization in FDSOI MOSFETs," *Microelectronic Engineering*, vol. 88, no. 7, pp. 1286–1290, 2011.
- [7] S. D. dos Santos, B. Cretu, V. Strobel et al., "Low-frequency noise assessment in advanced UTBOX SOI nMOSFETs with different gate dielectrics," *Solid-State Electronics*, vol. 97, pp. 14–22, 2014.
- [8] C. G. Theodorou, E. G. Ioannidis, F. Andrieu et al., "Low-frequency noise sources in advanced UTBB FD-SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 61, no. 4, pp. 1161–1167, 2014.
- [9] C. G. Theodorou, E. G. Ioannidis, S. Haendler et al., "Front-back gate coupling effect on $1/f$ noise in ultra-thin Si film FDSOI MOSFETs," in *Proceedings of the International Semiconductors Conference Dresden-Grenoble (ISCDG)*, Dresden, Germany, 2012.
- [10] E. G. Ioannidis, C. G. Theodorou, T. A. Karatsori, S. Haendler, C. A. Dimitriadis, and G. Ghibaudo, "Drain-current flicker noise modeling in nMOSFETs from a 14-nm FDSOI technology," *IEEE Transactions on Electron Devices*, vol. 62, no. 5, pp. 1574–1579, 2015.
- [11] E. G. Ioannidis, C. G. Theodorou, T. A. Karatsori, S. Handler, C. A. Dimitriadis, and G. Ghibaudo, "Drain-current noise modelling in nMOSFETs from 14-nm FD-SOI Technology," *IEEE Transactions on Electron Devices*, vol. 62, pp. 1574–1579, 2015.
- [12] T. Boutchacha and G. Ghibaudo, "Improved modeling of low-frequency noise in MOSFETs-focus on surface roughness effect and saturation region," *IEEE Transactions on Electron Devices*, vol. 58, no. 9, pp. 3156–3161, 2011.

- [13] M. Shin, M. Shi, M. Mouis et al., "In depth characterization of electron transport in 14 nm FD-SOI CMOS devices," *Solid-State Electronics*, vol. 112, pp. 13–18, 2015.
- [14] P. K. McLarty, S. Cristoloveanu, O. Faynot, V. Misra, J. R. Hauser, and J. J. Wortman, "A simple parameter extraction method for ultra-thin oxide MOSFETs," *Solid-State Electronics*, vol. 38, no. 6, pp. 1175–1177, 1995.
- [15] I. Ben Akkez, A. Cros, C. Fenouillet-Beranger et al., "New parameter extraction method based on split C-V measurements in FDSOI MOSFETs," *Solid-State Electronics*, vol. 84, pp. 142–146, 2013.
- [16] G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Electronics Letters*, vol. 24, no. 9, pp. 543–545, 1988.
- [17] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, and J. Brini, "Improved analysis of low frequency noise in field-effect MOS transistors," *Physica Status Solidi (A)*, vol. 124, no. 2, pp. 571–581, 1991.
- [18] G. Ghibaudo and T. Boutchacha, "Electrical noise and RTS fluctuations in advanced CMOS devices," *Microelectronics Reliability*, vol. 42, no. 4-5, pp. 573–582, 2002.
- [19] FlexPDE Software, <http://www.pdesolutions.com>.
- [20] W. Hänsch, T. Vogelsang, R. Kircher, and M. Orłowski, "Carrier transport near the Si/SiO₂ interface of a MOSFET," *Solid-State Electronics*, vol. 32, no. 10, pp. 839–849, 1989.
- [21] G. Ghibaudo, "Mobility characterization in advanced FD-SOI CMOS Devices," in *Semiconductor-On-Insulator Materials for NanoElectronics Applications*, pp. 307–322, Springer, Berlin, Germany, 2010.
- [22] S. P. Devireddy, B. Bigang Min, Z. Çelik-Butler et al., "Low-frequency noise in TaSiN/HfO/sub 2/nMOSFETs and the effect of stress-relieved preoxide interfacial layer," *IEEE Transactions on Electron Devices*, vol. 53, no. 3, pp. 538–544, 2006.
- [23] B. Min, S. P. Devireddy, Z. Celik-Butler, A. Shanware, L. Colombo, and K. Green, "Impact of interfacial layer on low-frequency noise of HfSiON dielectric MOSFETs," *IEEE Transactions on Electron Devices*, vol. 53, pp. 1459–1466, 2006.