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Research Article

A Low Threshold Voltage Ultradynamic Voltage Scaling SRAM Write Assist Technique for High-Speed Applications

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With the percentage of embedded SRAM increasing in SoC chips, low-power design such as the near-threshold SRAM technique are getting increasing attention to reduce the entire chip energy consumption. However, the descending operating voltage will lead to longer write latency and a higher failure rate. In this paper, we present a novel low Vth ultradynamic voltage scaling (UDVS) 9T subthreshold SRAM cell to improve the write ability of SRAM cells. The proposed Low Vth UDVS SRAM cell is demonstrated with a low threshold voltage speed-up transistor and an ultradynamic voltage scaling circuit implemented in 16 nm low-leakage CMOS technology. This wide supply range was made possible by a combination of circuits optimized for both subthreshold and abovethreshold regimes. This write assist technique can be operated selectively to provide write capability at very low voltage levels while avoiding excessive power overhead. The simulation findings reveal that with 16 nm technology, the write ability is improved by 33% over the normal case at 0.9 V supply voltage.

1. Introduction

SRAMs account for a significant portion of a chip's total area and energy in modern integrated circuits due to the trend of integrating additional on-chip memory on a die. Since large active and leakage power reductions can be gained by voltage scaling, it is crucial to design a memory with dynamic voltage scaling (DVS) capability [1]. Nevertheless, due to competing trade-offs between low-voltage and high-voltage transistor properties, optimizing circuit operation over a wide voltage range is not simple. Particularly, the functionality of the different help circuits needed for the low-voltage operation could have a significant negative impact on high-voltage performance. Reconfigurable voltage-scalable circuits provide the necessary adaptability for circuits to adapt to the demands of the voltage range in which they are operating [2]. In essence, read assist refers to retaining the data when the static random access memory (SRAM) cell is at a low-voltage supply with a reduced size. Also, write assist refers to writing new data in the cell at a low supply voltage with a reduced size of the transistor. Write failures (write ability) or read failures (readability) are causing limitations on the minimum supply voltage means minimizing the supply voltage, causing hurdles in writing and reading data [3]. When using write assist at low voltage, the main issue is that the cell flips and prevents the data from being written [4]. This effect gets more pronounced as the size of the transistor is being reduced day by day as per consumer demand. As a result, it assists SRAM to write operations with better performance and stability. Each bit is stored in a semiconductor memory called an SRAM using bistable latching circuitry [5]. A wide variety of high-speed applications in the electronics industry were made possible by SRAM's speed advantage over other memories [6]. The speed of the SRAM can be increased in a variety of ways. The optimal methods for lowering the power consumption in SRAM are UDVS (ultradynamic voltage scaling) and transient negative bit line voltage (T-NBLV) approaches [7]. This research aims to assess the performance effectiveness of the UDVS and T-NBLV approaches for enhancing the speed in 6T SRAM cells and find a new

technique to overcome the shortcomings of existing approaches. The major contribution of this paper is organized as follows. Conventional write failures in the 6T SRAM design are presented in Section 2. The UDVS approach for 6T SRAM is described in Section 3. The T-NBLV-based SRAM design is found in Section 4. The proposed write assist circuit is discussed in Section 5. Results, explanations, and simulated waveforms are included in Section 7.

2. Write Failures in SRAM

The 6T SRAM cell, as its name indicates, has six transistors, of which two are access transistors and the other two serve as back-to-back inverters, as shown in Figure 1 [8]. Two inverters are built using pull-up and pull-down sections, and two access transistors can access them [1]. PMOS and NMOS transistors make up the pull-up and pull-down sections, respectively. Access transistors can be used to regulate read and write processes. Word lines are in full control of the access transistors. With the supply voltage VDD applied, the transistor can store data if WL is low, and read and write operations can be carried out if WL is high. The access transistors are turned on as a result of the write, which raises the WL value. Through bit and bit-bar lines, the read or write can be performed. SRAM write failure happens if the node stores $Q = 1$ and $QB = 0$. While the word line (WL) is still active, the voltage at node Q must be reduced to the trip point of the inverter connected to node QB (i.e., PU2-PD2) in order to write the value "0" to that node. Due to process variations, the discharge of node Q becomes more challenging if PU1 becomes stronger and/or PG1 becomes weaker. Moreover, the trip point of PU2-PD2 decreases as PU2 and PG2 are weaker and PD2 gets stronger. Thus, node Q might not decrease below the PU2-PD2 trip point, leading to a write failure as depicted in Figure 2. In general, weaker pull-up devices PU2/PU1 and/or stronger access devices (PG2/PG1) increase the cell's write ability. Nevertheless, weaker pull-up devices or stronger access cause read-disturb failures. In order to simultaneously prevent all types of failure, dynamic adjustments of cell terminal voltages, depending on the type of operation, are more adaptable. Higher word-line voltages (stronger access devices) or lower cell supply voltages (weaker pull-up devices on the selected row during a write operation) can both increase the write ability of SRAM cells. However, the half-select stability is reduced by both of these methods. Using a column-based control, where the selected column's cell supply is decreased throughout the write operation, can prevent this failure [9]. This method necessitates separate supply lines for various columns, which lowers each supply line's capacitance and lowers the supply voltage drop. The complexity of design and testing is also increased by using two distinct stable voltages (for word line or cell supply) for read and write operations.

3. SRAM Using the UDVS Technique

Figure 3 depicts the 6T SRAM cell with a UDVS architecture. It combines an SRAM cell, a write circuit, a UDVS circuit, and a read circuit [10]. The data values can be written to the bit line using the write driver circuitry. Figure 4 depicts the circuitry for the write driver. A gated inverter is a device that is connected in series by four vertical components. The transistors in write driver circuits are standardized in terms of dimensions.

The data from the SRAM cell is read using the read circuit. A precharge circuit, isolation circuit, and sense amplifier are all included in the read circuit. The precharge circuit, shown in Figure 4, is the major component of the read circuitry. The two transistors can be used to precharge the bit lines.

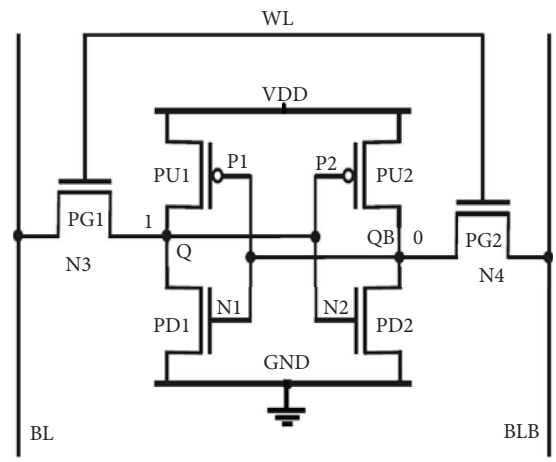


Figure 1: 6T SRAM cell.

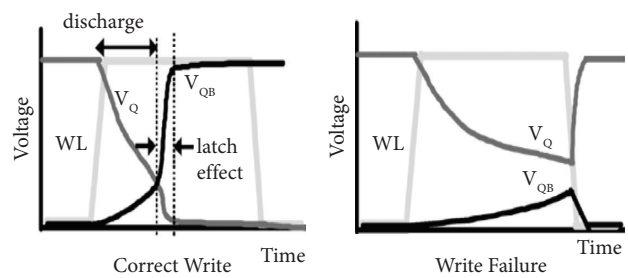


Figure 2: Write failures in the SRAM cell.

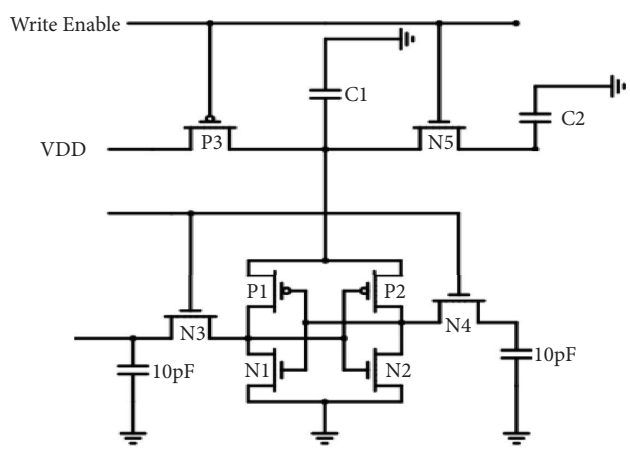


Figure 3: UDVS SRAM write assist circuit.

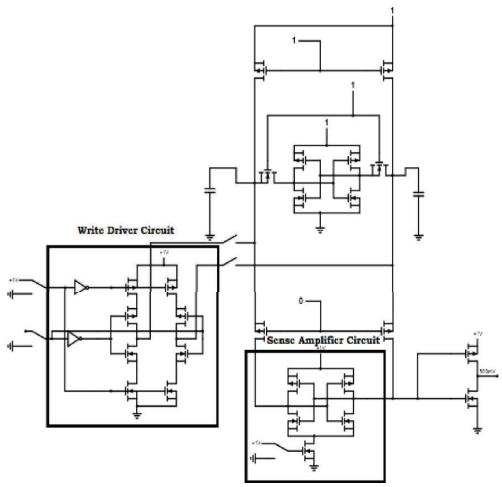


Figure 4: SRAM cell with write and read circuit.

This approach states that by weakening the pull-up transistor relative to the pass-gate transistor, the word-line voltage VWL can be lowered. It also gets simpler to write new data to the bit cell if the pull-up transistor is weaker. Without using an external voltage power source, this write assist technology is implemented using a series of coupling capacitances. VDD decreasing write assistance is depicted graphically in Figure 5.

4. SRAM Using the T-NBLV Technique

Another approach for writing assistance is the T-NBLV method. This will speed up the write operation. When WL is high, this technique applies a negative voltage to the transistor terminal. The channel bandwidth between the source and drain terminals of the pass transistor is widened by the gate voltage and the negative voltage. The wider channel improves the write operation [11].

Here, $Vgs = Vg - Vs$. In the case of a negative source voltage, $Vgs = Vg - (-Vs) = Vg + Vs$. Channel width results from an increase in both Vgs and Id. Figure 6 depicts the write and read circuit for 6T SRAM cells utilizing a transient negative bit line technique. Both write and read circuits are present in the circuit. Two capacitors are used in write circuits to implement coupling [12]. One end of the capacitor is attached to BL and BLB, and the other end is connected to BIT-EN (BE). Capacitors are connected in series. The capacitive coupling will produce a negative voltage if the BIT-EN is low; in this case, one end of the capacitor will be set to "0," while the other end will continue to maintain VDD, as shown in Figure 7. If the positive terminal is "0," the negative terminal will at least be high for a while due to the capacitor's slow discharge. The high gate-to-source and WL voltage values make it the width to access the transistor channel. More data can be easily transmitted into the SRAM cell if the channel width is larger. This boosts the effectiveness of SRAM cells' write operations [13, 14]. Figure 8 illustrates the T-NBL SRAM cell's read and write operations.

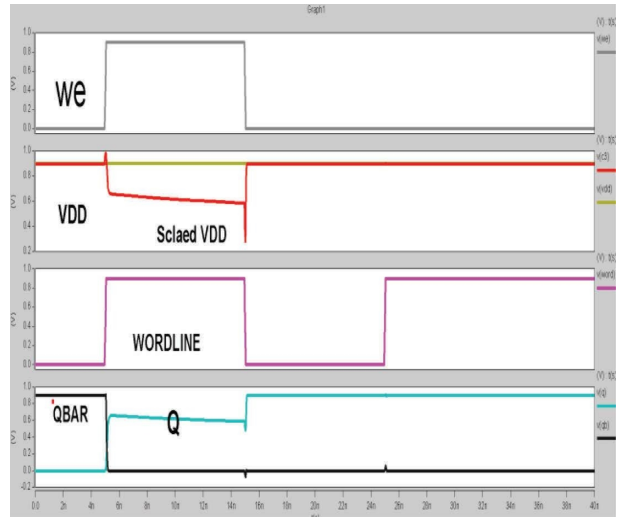


Figure 5: Voltage scaling during a write operation.

5. Proposed Low Vth UDVS Write Assist Technique

The proposed low Vth UDVS SRAM write assist circuit uses a low Vth to speed the performance and an UDVS scheme to weaken the SRAM cell, as shown in Figure 9. The write driver circuit is used to write the data into the cell. When WE is LOW, P3 and N5, and N6 are OFF and VDD is supplied to the cell and no write operation is performed. When WE is HIGH, P3 is OFF and N5 and N6 are ON, and supply voltage VDD is reduced based on the capacitor value. In addition, due to the low Vth N6 transistor, the speed of the circuit is increased in Figure 10. It is observed that whenever the write enable is asserted, the voltage is scaled down and the cell becomes weak and it is easy to write the data into the SRAM cell. Moreover, the switching operation takes longer due to the presence of low Vth NMOS transistor N6.

5.1. Data Retention Voltage. The data retention voltage (DRV) is the minimum power supply voltage required to retain the data at complimentary nodes *Q* and QB when the SRAM cell is in standby mode. Figure 11 depicts the most common graphic representation of the static noise margin (SNM) for an SRAM cell with inverse VTC-1 of inverter 1 and the voltage transfer characteristic (VTC) of Inverter 2. Reduce the power supply voltage until the flip state or content of the SRAM cell remains constant. When vdd is decreased to DRV, the internal inverters' voltage transfer curves degenerate to the point where the SRAM cell's SNM is zero. The cell becomes unstable at 0.6 v. To retain the data in the cell the power supply vdd should be maintained above 0.6 v.

All the above designs such as CMOS 6T SRAM cells are simulated using the synopsys HSPICE tool with predictive technology Model [15] at 16 nm technology node and are compared and studied.

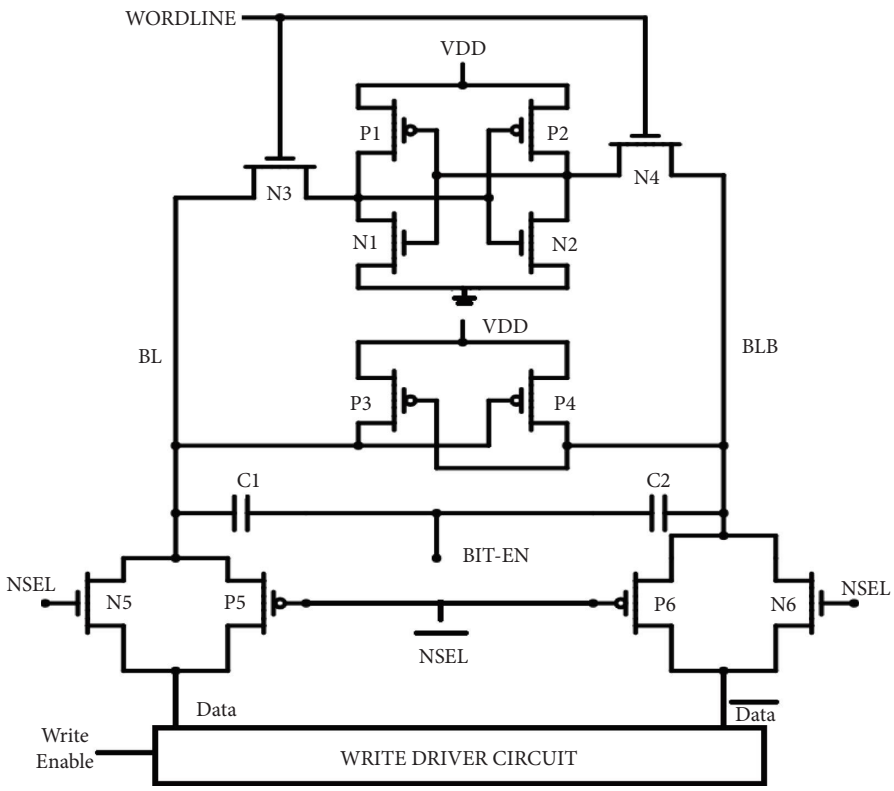


Figure 6: T-NBLV SRAM write assist circuit.

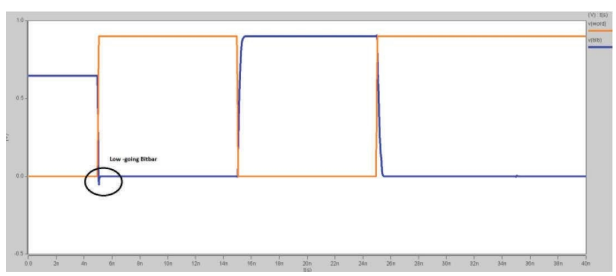


Figure 7: Negative bitline during write operation.

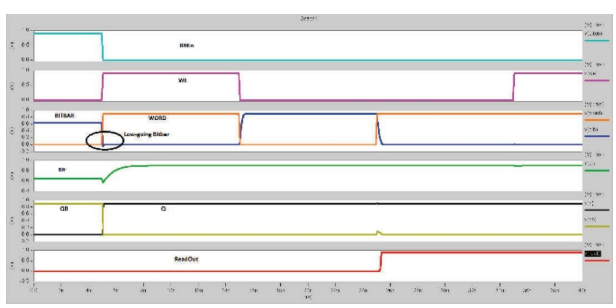


Figure 8: TNBL write and read operations.

6. Results and Discussions

The synopsys HSPICE tool is used to implement the design in 16 nm technology. Figures 12–14 demonstrate the output results for simple 6T SRAM, UDVS SRAM, T-NBLV SRAM, and Low Vth UDVS SRAM cells, respectively, in 16 nm technology node. In terms of performance parameters, Table 1 compares and contrasts the UDVS, T-NBLV, and low Vth UDVS approaches with simulation parameters tabulated in Table 2.

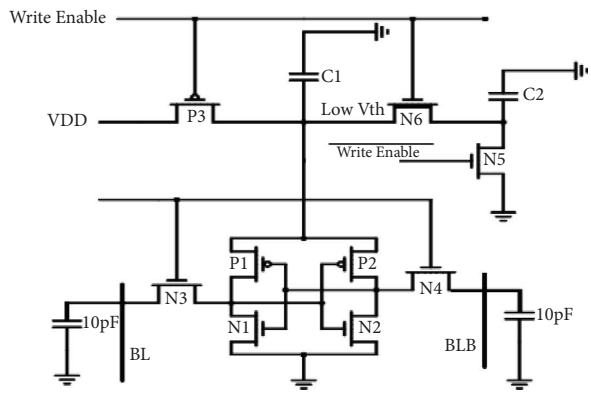


Figure 9: Low Vth UDVS SRAM write assist circuit.

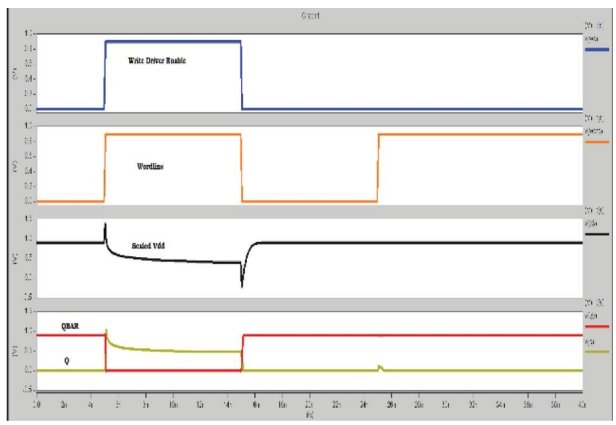


Figure 10: Low Vth UDVS write operation waveforms.

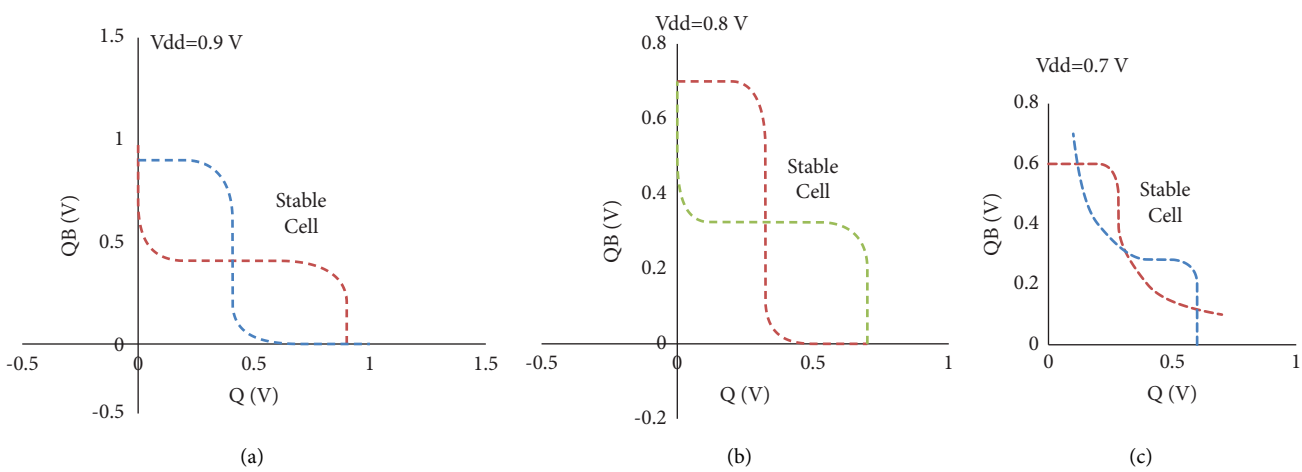
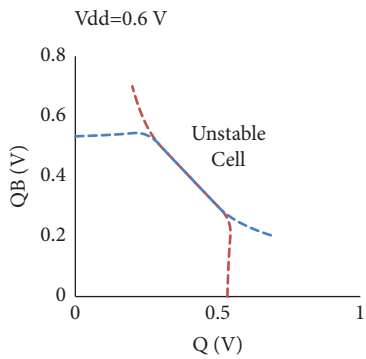
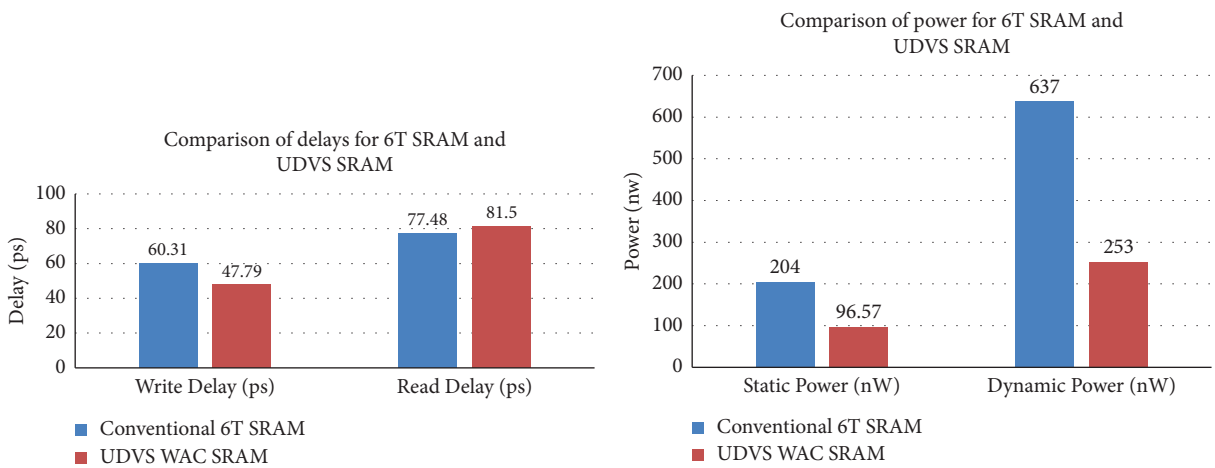


Figure 11: Continued.



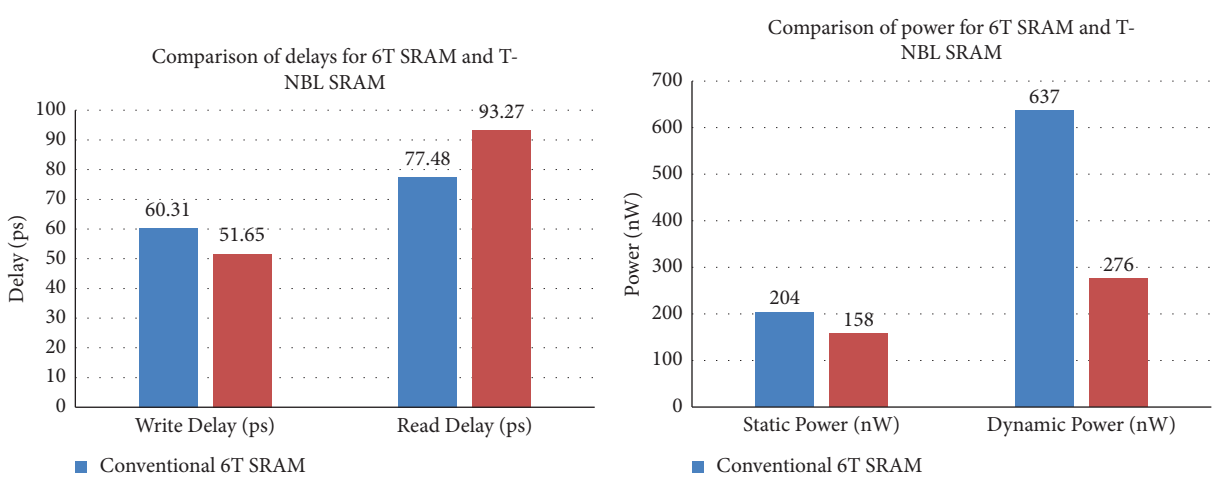
(d)

Figure 11: VTC curve for the proposed SRAM cell. (a) VTC curve at vdd = 0.9 v and (b) VTC curve at vdd = 0.8 v (c) VTC curve at vdd = 0.7 v (d) VTC curve at vdd = 0.6 v.



(a) (b)

Figure 12: Comparison graph for 6T SRAM and UDVS SRAM (a) write and read delays and (b) static and dynamic powers.



(a) (b)

Figure 13: Comparison graph for 6T SRAM and TNBL SRAM (a) write and read delays and (b) static and dynamic powers.

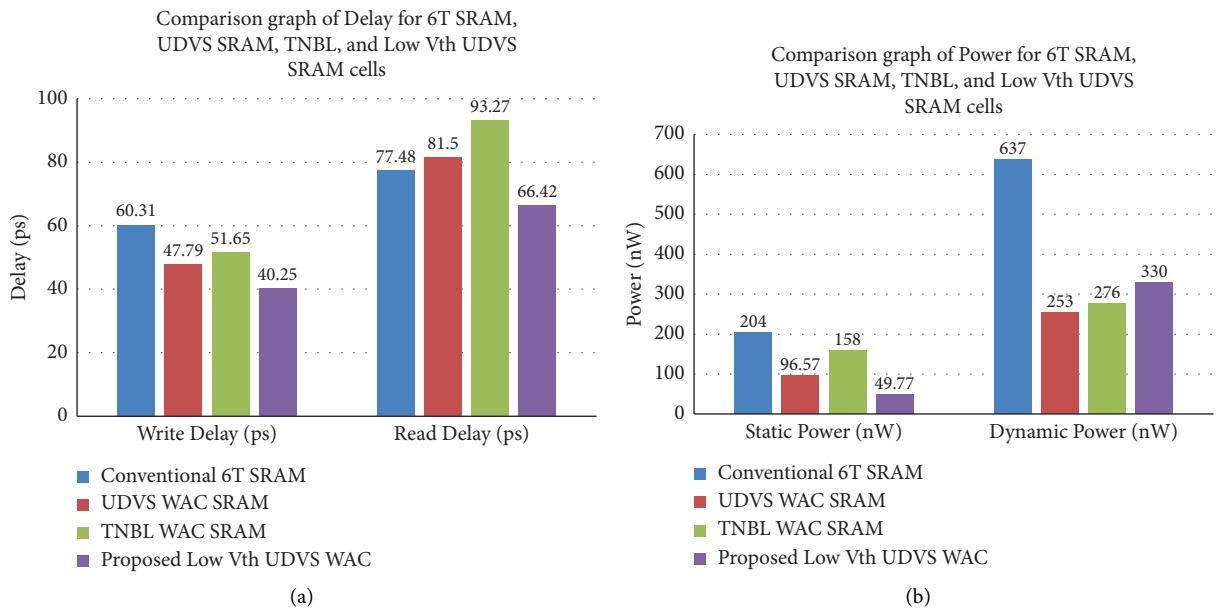


Figure 14: Comparison graph for 6T SRAM, UDVS, TNBL, and low Vth UDVS SRAM cells: (a) write and read delays and (b) static and dynamic powers.

Table 1: Simulation results of different write assist techniques.

Parameters	6T SRAM cell	UDVS WAC SRAM cell	TNBL WAC SRAM cell	Proposed low Vth UDVS WAC SRAM cell
Write delay (ps)	60.31	47.79	51.65	40.25
Read delay (ps)	77.48	81.5	93.27	66.42
Static power (nW)	204	96.57	158	49.77
Dynamic power (nW)	637	253	276	330

Table 2: Simulation parameters.

Supply voltage (V)	Normal threshold voltage (mV)	Low threshold voltage (mV)
0.9	0.681	0.525

The obtained results show that the proposed technique gives a better improvement in write delay/speed is improved by 33% and read delay by 14%. Also, static power is also reduced by 75%, but this technique dissipates more power than the UDVS and TNBL techniques. The proposed speed improvement technique gives a better improvement in write delay or speed.

7. Conclusion

This article presents a technique for ultradynamic voltage scaling that combines a speed-up transistor with a low threshold voltage for high performance with low energy operation for low-performance scenarios. The design is implemented using the 16 nm Synopsys HSPICE tool. While maintaining the advantages of bit line- (or column-) based control and obviating the need for extra voltage levels, low Vth UDVS can reduce write failure more than tran-negative bit-line voltage (T-NBLV) and UDVS techniques. The SRAM constructed utilizing the UDVS and T-NBLV techniques are contrasted with the simulation settings that have been examined. The obtained results indicate that SRAM implemented using the low Vth UDVS technique outperforms SRAM implemented using the UDVS and T-NBLV techniques in terms of performance. Over 6T SRAM, UDVS, and T-NBLV SRAM cells, the write operation speed is increased by 33%, 15%, and 20%, respectively. In addition, both static and dynamic power are decreased. Therefore, the proposed Low Vth UDVS approach can be very beneficial in low-power and reliable SRAM architecture for high-speed applications.

Data Availability

The simulation result data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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