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Research Article

A 0.9 V, 8T2R nvSRAM Memory Cell with High Density and Improved Storage/Restoration Time in 28 nm Technology Node

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Combining with a static random-access memory (SRAM) and resistive memory (RRAM), an improved 8T2R nonvolatile SRAM (nvSRAM) memory cell is proposed in this study. With differential mode, a pair of 1T1R RRAM is added to 6T SRAM storage node. By optimizing the connection and layout scheme, the power consumption is reduced and the data stability is improved. The nvSRAM memory cell is realized with UMC CMOS 28 nm 1p9m process. When the power supply voltage is 0.9 V, the static noise/read/write margin is 0.35 V, 0.16 V, and 0.41 V, respectively. The data storage/restoration time is 0.21 ns and 0.18 ns, respectively, with an active area of 0.97 μm^2.

1. Introduction

SRAM is a well-known high-speed and low-power cache. However, when the system is powered off, the data of the storage node cannot be saved, which limits the use of SRAM in applications. For ATM, railway controller, and other equipment, it is necessary to store real-time data in case of power failure. After the power supply of the system rises, the data can be restored to the original state. EEPROM, EPROM, Flash, and other nonvolatile memories can store data in real time, but they all have some performance problems. In recent years, in order to solve the volatile problem of SRAM, academia and industry have begun to study nvSRAM. Compared with traditional SRAM, nvSRAM has the same performance and nonvolatile function, which provides guarantee for high-end instruments and equipment to store data in real time.

As a new nonvolatile memory, RRAM has the advantages of high density, low-power consumption, and compatibility with the CMOS technology. Therefore, based on the nonvolatile and high stability of RRAM, various nvSRAM memory cell structures combined with RRAM are proposed. Table 1 summarizes the advantages and disadvantages of the four mainstream NVMs.

Garbin et al. proposed the 6T2R nvSRAM structure [5], which parallels a pair of RRAMs on the storage nodes and uses the high- and low-resistance states of RRAM to realize data storage. But the stability of SRAM will also decline, and the existence of DC short-circuit current will increase power consumption. An 8T2R nvSRAM cell is presented in [6], which controls the conduction branch by adding two MOS transistors in series with RRAM, so as to avoid DC short-circuit current of 6T2R structure. The structure adopts differential mode and has good data restoration efficiency. Turkyilmaz et al. proposed a RRAM-based FPGA solution [7], integrating the nonvolatile RRAM into the configuration unit and register, so as to restore FPGA data immediately. The scheme adopts 22 nm LETI-FDSOI process and nvSRAM with 8T2R structure. The increased control signal will increase the chip area in this structure. Wei et al. proposed a 7T1R structure [8]. This scheme adopts single mode and directly adds a 1T1R memory cell to the storage node of SRAM. Compared with the structure of 8T2R, this structure has higher integration and high-fault margin in data restoration, but MOS and NVM devices are greatly affected by the process. In the 6T2R nvSRAM [9], the load PMOS of SRAM is replaced by RRAM, and the access transistor is replaced by the transmission gate. The cell has

Table 1: Four mainstream NVMs.

NVM	FERAM [1]	MRAM [2]	PCM [3]	RRAM [4]
Read speed	20–80 ns	3–20 ns	20–50 ns	10–50 ns
Write/erase speed	50/50 ns	3–20 ns	50/ 120 ns	10–50 ns
Resistance ratio	>8	2	>10	>10
Power consumption	Low	High	Low	Low
Supply voltage	2-3 V	3 V	1.5–3 V	1.5–3 V
Process compatibility	Incompatible	Low	High	High
Integration	Low	High	High	High

fast read-write speed and low-static power consumption, but the introduction of transmission gate may cause destructive operation when reading data.

In view of the above shortcomings, an improved 8T2R nvSRAM memory cell is proposed and implemented by a UMC 28 nm process in this study. By optimizing the RRAM connection mode and using the differential data storage/restoration mode, the structure not only reasonably optimizes the area but also improves the data storage ability. It also obtains better noise margin and fast data storage/restoration time.

2. Memory Cell Design

The memory cell of nvSRAM is mainly composed of SRAM and nonvolatile cells. SRAM adopts the traditional 6T SRAM structure, as shown in Figure 1. Transistors MP1 and MN1 form a left inverter, and MP2 and MN2 form a right inverter. The two inverters are crosscoupled to store data. MN3 and MN4 are access transistors. Storage nodes Q and QB are, respectively, connected to BL and BLB through access transistors. WL is the gate control signal of access transistors. Only when WL is turned on can the memory be read and written. The previous nvSRAM memory cell mainly includes 6T2R, 7T1R, and 8T2R. The structure of 6T2R adds a pair of RRAM to the storage nodes. In case of system failure, the data are directly stored in RRAM to avoid data loss. Due to the DC path between storage node and RRAM, the leakage of memory and the increase of power consumption are caused. 7T1R structure adds a 1T1R nonvolatile memory to its storage node, which isolates the RRAM from the storage node through MOS transistor and solves the problems of leakage and power consumption in 6T2R cell. But the single-ended data writing will result in high-fault tolerance rate, and its asymmetry will affect the density of memory array. 8T2R cell adopts differential structure, which has high stability when storing data. However, when RRAM performs set and reset operations, higher operating voltage is required, which brings some challenges to the design of peripheral circuits.

The improved 8T2R nvSRAM memory cell proposed in this study is shown in Figure 2. Different from the previous 8T2R cells, in the 1T1R structure, one end of the

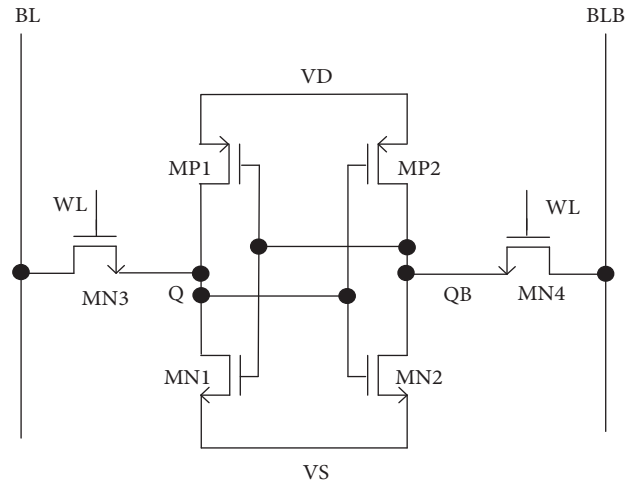

Figure 1: 6T SRAM.

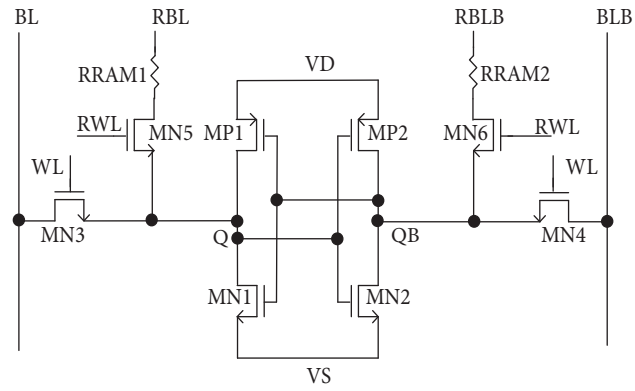

Figure 2: 8T2R nvSRAM.

NMOS transistor is connected to the storage node and the other end is connected to the lower electrode of the RRAM. The transistor gate is controlled by the new signal RWL, and the upper electrode of the RRAM is controlled by the new signal RBL and RBLB, respectively, and CMOS 28 nm 1p9m process is adopted which makes the core device have great driving ability and good stability. Since bipolar RRAM is used, when RRAM performs set and reset operations, different voltages are applied to its upper and lower electrodes to control the resistance change. The upper electrodes of RRAM are introduced into independent control signals, respectively, and the resistance value of RRAM is controlled through driving circuit and power control circuit. Only when the RWL signal is turned on can the data of SRAM and RRAM be transmitted, so that the static power consumption is zero when the NVM is not working.

During normal operation, nvSRAM only performs read and write. When the power supply voltage drops or turns off, the system switches to data storage mode and the data are stored to RRAM. When the voltage of SRAM recovers, the data start to restore, and the data in RRAM will be restored to the storage node of SRAM.

The data storage operation is shown in Figure 3. When $Q = 0$, QB = 1, RRAM1 and RRAM2 are in the state of high- and low-resistance, respectively. When the system power supply of nvSRAM fails, nvSRAM switches to data storage mode. At this time, VD switches to RVD. The voltage of node QB rises to RVD with the change of VD, and Q is always low. Meanwhile, RBL and RBLB are high. When RWL is turned on, the upper and lower electrodes of RRAM1 have a large voltage difference. A set operation is carried out, and the resistance of RRAM2 remains unchanged. When both RBL and RBLB are low and RWL is turned on, RRAM2 performs reset operation. Then, RRAM1 resistance remains unchanged. By controlling RBL, RBLB, and the system power supply of nvSRAM, the bipolar RRAM resistance value can be changed, so as to achieve the purpose of data storage.

The data restoration operation is shown in Figure 4. The two RRAMs are in the state of low- and high-resistance, respectively. At this moment, the power supply voltage is low and no data is stored in the storage node. When the power supply gradually rises from 0 to VD and RWL is turned on, the voltage of RBL and RBLB becomes low through the control of read drive circuit. When decoded by the clock control circuit and the address decoding control circuit, the RWL is high, making MN5 and MN6 turn on. The conduction of MN6 makes the voltage of RRAM2 gradually higher, while the conduction of MN5 makes the voltage of RRAM1 gradually lower. When the power supply is restored, the voltage of the two storage nodes is restored to low and high, respectively.

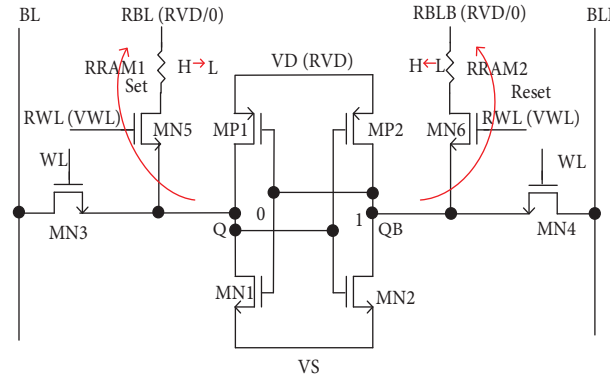

Figure 3: Data storage operation.

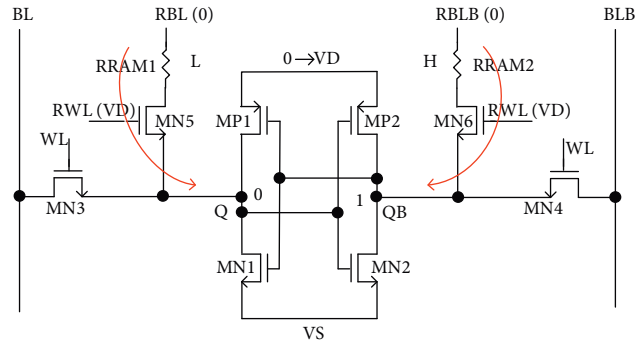

Figure 4: Data restoration operation.

3. Memory Cell Size Analysis

In reading process, if the memory cell is not designed properly, it will make data read incorrectly. This phenomenon is called destructive reading problem. In order to avoid this problem, the transistor size of memory cell must meet certain requirements. The read operation of nvSRAM is shown in Figure 5. When $Q = 1$ and QB = 0, the voltages of the two-bit lines and WL are high, MN3 and MN4 are on at this time, and BLB, MN4, and MN2 form a path from power supply to ground. If the size of MN4 is larger than MN2, it is equivalent to two transistors dividing the voltage of BLB, and the large size of MN4 makes the storage node QB have a large voltage. When the voltage of Vn2 is greater than the threshold of MN1, the voltage of the storage node will flip, resulting in the loss of original data.

To avoid the problem of destructive readout, when designing memory cell size, it must ensure that the voltage of Vn2 is less than the flip threshold Vs of the left inverter. In the best case, the voltage of Vn2 is less than the threshold of transistor MN1 to avoid turning on MN1. At this time, when the voltage of bit line BLB is approximately equal to power supply voltage VDD and node QB does not make an error, the voltage of Vn2 is less than the flip threshold Vs of the left inverter. By analyzing the state of each transistor at the critical point, it can be seen that MN3 works in the

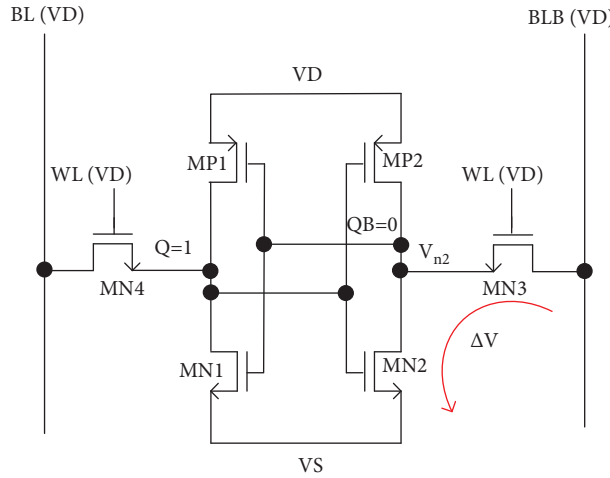

Figure 5: Read operation.

saturation region and MN2 works in the linear region. Assuming that the flip threshold Vs of the inverter is half of the power supply voltage, that is, Vn2 = Vs = VDD/2, and VBLB = VD. Then, substitute it into the current equation of the transistor. Since the currents of MN3 and MN2 are the same, equation (1) is obtained. Meanwhile, the cell ratio (CR) of the memory cell is defined, as shown in equation (2).

$$\frac{k_{n,MN3}}{2}\left(\frac{V_{DD}}{2}-V_{Tn}\right)^2 = k_{n,MN2}\left[\left(V_{DD}-V_{Tn}\right)\frac{V_{DD}}{2}-\frac{V_{DD}^2}{8}\right]. \quad (1)$$

$$CR = \frac{\left(W_{MN2}/L_{MN2}\right)}{\left(W_{MN3}/L_{MN3}\right)}. \quad (2)$$

To calculate the two equations, the CR value must meet the conditions greater than 1.5 in order to avoid destructive reading operation. Moreover, with the increasing value of CR, the voltage of Vn2 is closer to zero, and the reading capacity of the memory cell is stronger. Similarly, write operation is shown in Figure 6. When BL is high and BLB is low, in internal storage nodes $Q = 0$ and $QB = 1$, respectively, so there are two paths in the memory at this time. One is formed by BL, MN4, MN1, and Vs, and the other is formed by power supply VD, MP2, MN3, and BLB. During the read operation, the size of MN2 must be larger than MN3, which will make the high voltage on BL unable to be written to the storage node Q. Therefore, the key path of write operation is the path between the power supply and BLB. Only when the size of MN3 is large, MN3 and MP2 divide the voltage. At present, the voltage Vn2 of the storage node is less than the threshold of MP1. When the voltage of storage node is pulled down, MP1 will turn on, so as to ensure the correct writing of data.

Considering the process mismatch and other problems, the voltage of Vn2 should preferably be less than the threshold of the transistor. Meanwhile, both transistors MP2 and MN3 operate in the linear region. Consistent with the assumption in read operation, it is assumed that the flip threshold of the inverter is half of the power supply voltage, so equation (3) can be obtained. The pull up ratio (PR) on memory cell is defined, as shown in equation (4).

After calculation, the PR must be less than 1.5 before the cell can be successfully written, and the smaller the PR value is, the stronger the writing ability of the cell is. Through theoretical analysis and circuit simulation, the size of each device in the memory is shown in Table 2.

$$k_{n,MN3}\left[\left(V_{DD}-V_{Tn}\right)\frac{V_{DD}}{2}-\frac{V_{DD}^2}{8}\right] = k_{n,MP2}\left[\left(V_{DD}-\left|V_{Tp}\right|\right)\frac{V_{DD}}{2}-\frac{V_{DD}^2}{8}\right], \quad (3)$$

$$PR = \frac{\left(W_{MP2}/L_{MP2}\right)}{\left(W_{MN3}/L_{MN3}\right)}. \quad (4)$$

The size of memory cell is mainly related to its stability, and the noise margin is an important parameter for the stable storage of data in the memory cell. The noise margin of nvSRAM mainly includes static noise margin (SNM) [10], read noise margin (RNM) [11–13], and write noise margin (WNM) [14]. The three-noise margin represents the anti-noise ability of the memory cell in three modes: data storage, reading, and writing. The measurement method of noise margin is mainly evaluated by voltage transfer curve (VTC).

For memory cell, CR determines the reading noise margin [15]. PR determines the write noise margin [16]. In order to avoid the occurrence of destructive read problem, CR must be greater than a certain value, so that the voltage of storage node Q is low and too high voltage will flip the data of reverse storage node. Therefore, a large CR is required in size design, so there is a large RNM. But a large CR will increase the leakage and layout area. In order to have enough WNM during write operations, a smaller PR is required. Therefore, in this memory cell, CR proposed is 2.2 and PR is 1.2.

4. Experimental Result

The memory cell was fabricated with the CMOS 28 nm 1p9m process. Figure 7 shows the micrograph of test chip and memory cell layout. The layout design of memory cell must conform to both the standard CMOS process rules and the basic rules of RRAM. Each column and row share bit line and word line, so the word line and bit line will have large parasitic capacitance. In our work, four memory cells are taken as a whole with a common centroid and mirror layout. In this way, control signal lines can be multiplexed, and three layers of metal can realize high-density memory array.

As shown in Figure 8, RRAM is formed by resistive material. The lower electrode of RRAM is connected to metal 1 through Short VIA, and then connected to MOS transistor. The RRAM device in the middle is short circuited by a special mask layer. The upper electrode of RRAM is connected to RBL and RBLB through metal 2 [17].

The size of memory is 0.69 μm * 1.41 μm with three-layer metal structure. Metal 1 is mainly used for internal wiring. Metal 2 is used for longitudinal wiring of BL, BLB, VD, VS, RBL, and RBLB, and Metal 3 is used for transverse wiring of WL and RWL. Limited by the process, the RRAM cell can only use metal 1 and metal 2. The bit line signal is wired with metal 2, which reduces the area of memory cell.

8T2R nvSRAM memory cell is improved based on traditional 6T SRAM. In order to verify the impact of adding RRAM on SRAM, the noise margin of 8T2R nvSRAM and 6T SRAM memory cell is verified. Adopting the VTC measurement method, the noise margin is shown in Figure 9. When the power supply voltage is 0.9 V, SNM is 0.35 V, RNM is 0.16 V, and WNM is 0.41 V. The noise margin of 6T SRAM memory cell is almost consistent with

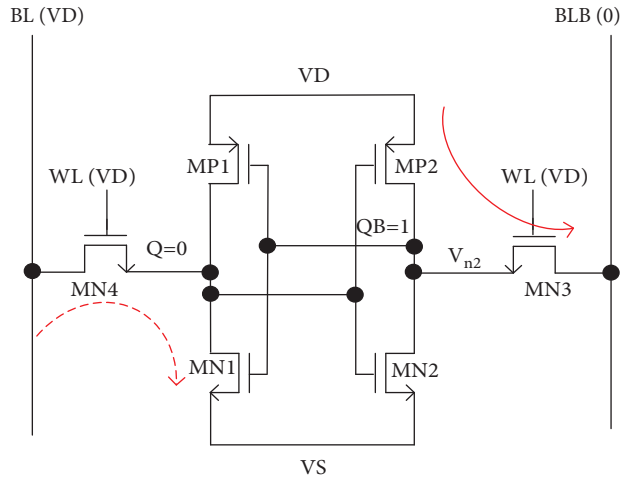

Figure 6: SRAM write operation.

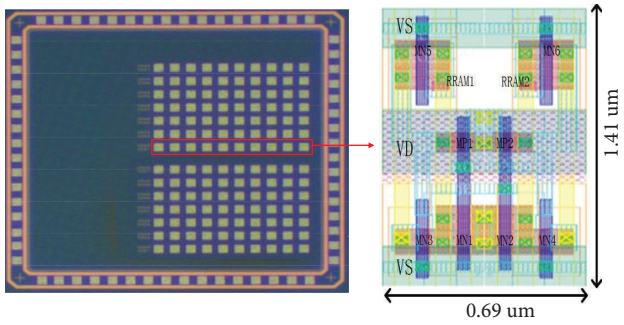

Figure 7: Micrograph of test chip and memory cell layout.

Table 2: Device size of nvSRAM memory cell.

	MN1 (MN2)	MP1 (MP2)	MN3 (MN4)	MN5 (MN6)	RRAM1 (RRAM2)
W/*L*	245/40	100/45	110/40	245/40	110/80
CR ratio			2.2		
PR ratio			1.2		

the 8T2R nvSRAM. It is verified that the proposed memory cell with RRAM still has good data anti-interference ability.

The write operation result is shown in Figure 10. When BL is low and BLB is high, the initial value of storage node *Q* is high, and WL increases from 0 to VDD. When the voltage of WL is 0.653 mV, the data of storage node flip to complete the write 0 operation. Similarly, when BL is high and BLB is low, the initial value of storage node *Q* is low, and the write 1 operation is finished.

Figure 11 shows the read operation. When reading is 0, BL and BLB are high, and the initial storage node *Q* is low. When WL increases from 0 to VDD, the voltage of *Q* rises to 0.104 mV, and the voltage of QB remains unchanged. During read 1 operation, BL and BLB are high, and the initial storage node *Q* is high. When WL increases from 0 to VDD, the voltage at QB rises to 0.104 mV.

The simulation result of writing data is shown in Figure 12. The data are written to 8 cells on one BL. DIN is the data writing port. When WE is high, CE and CLK are valid, the data DIN are written to 8 memory cells.

The result of reading data is shown in Figure 13. The data of 8 memory cells are read simultaneously. When CLK and CE are valid and OE is high, the data are output to DOUT.

The results of data storage and restoration circuit are shown in Figure 14. First, the system writes data 1 to SRAM. When power supply fails, the system enters into the storage mode. By controlling the peripheral driver module, the RRAM performs set and reset operations, respectively, and

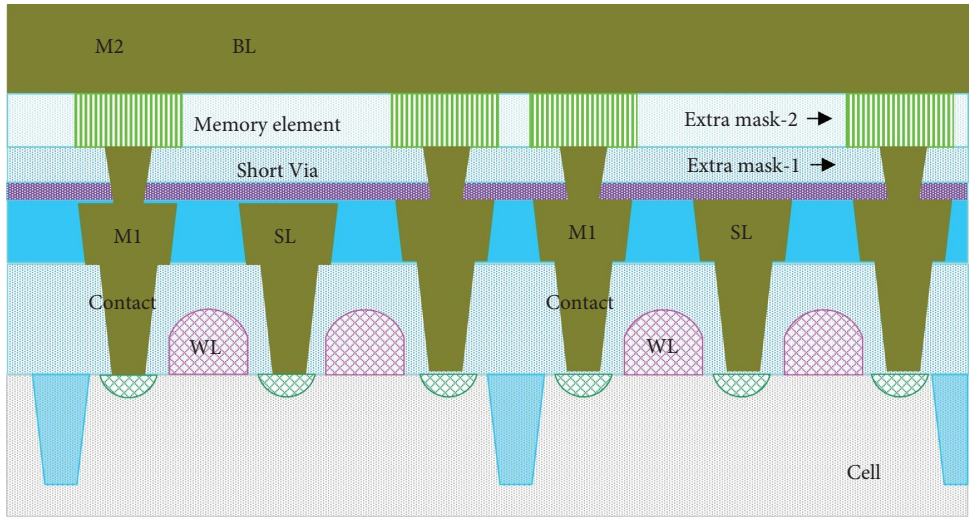

Figure 8: The fabrication steps.

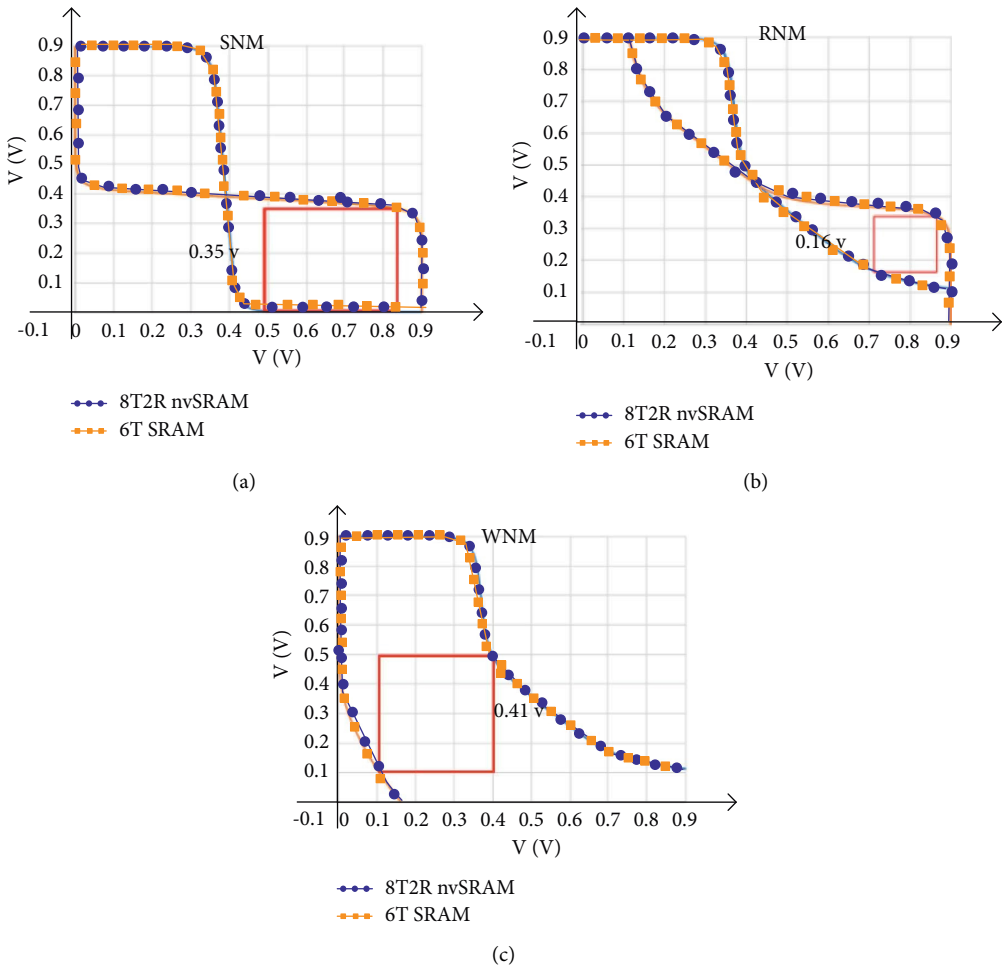

Figure 9: Three noise margins: (a) static noise margin (SNM); (b) read noise margin (RNM); and (c) write noise margin (WNM).

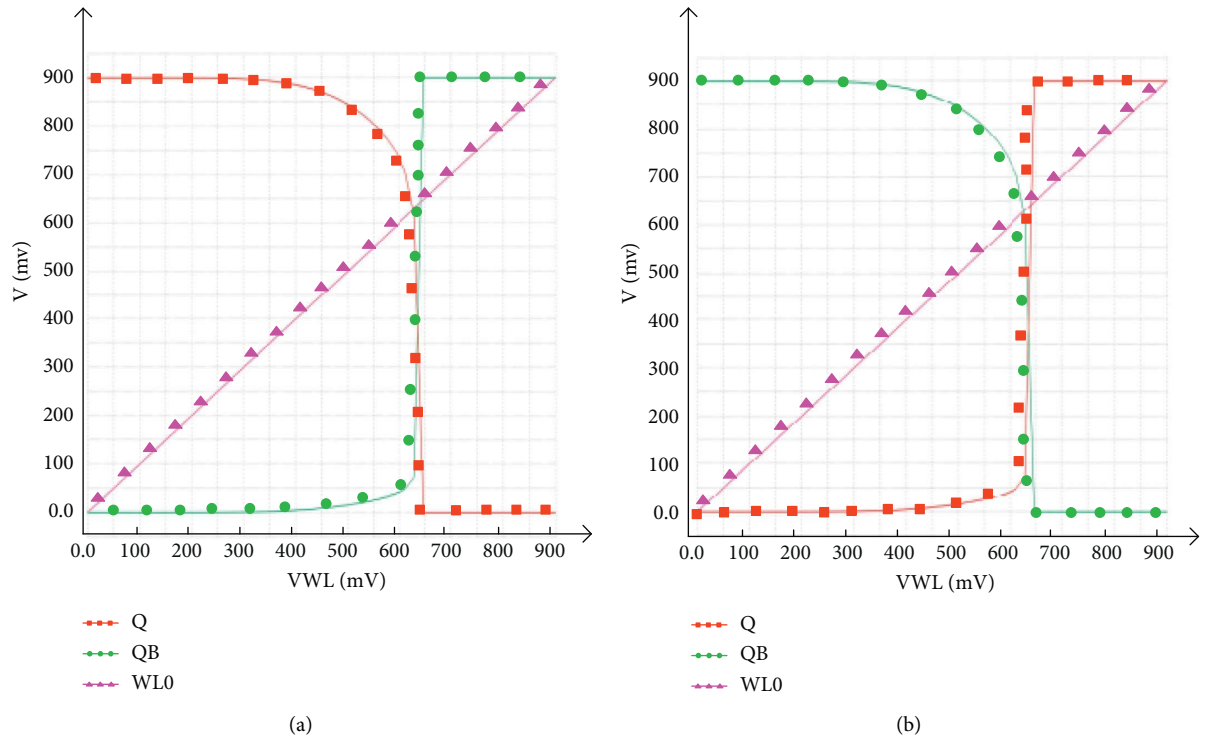

Figure 10: (a) Write 0 operation; (b) write 1 operation.

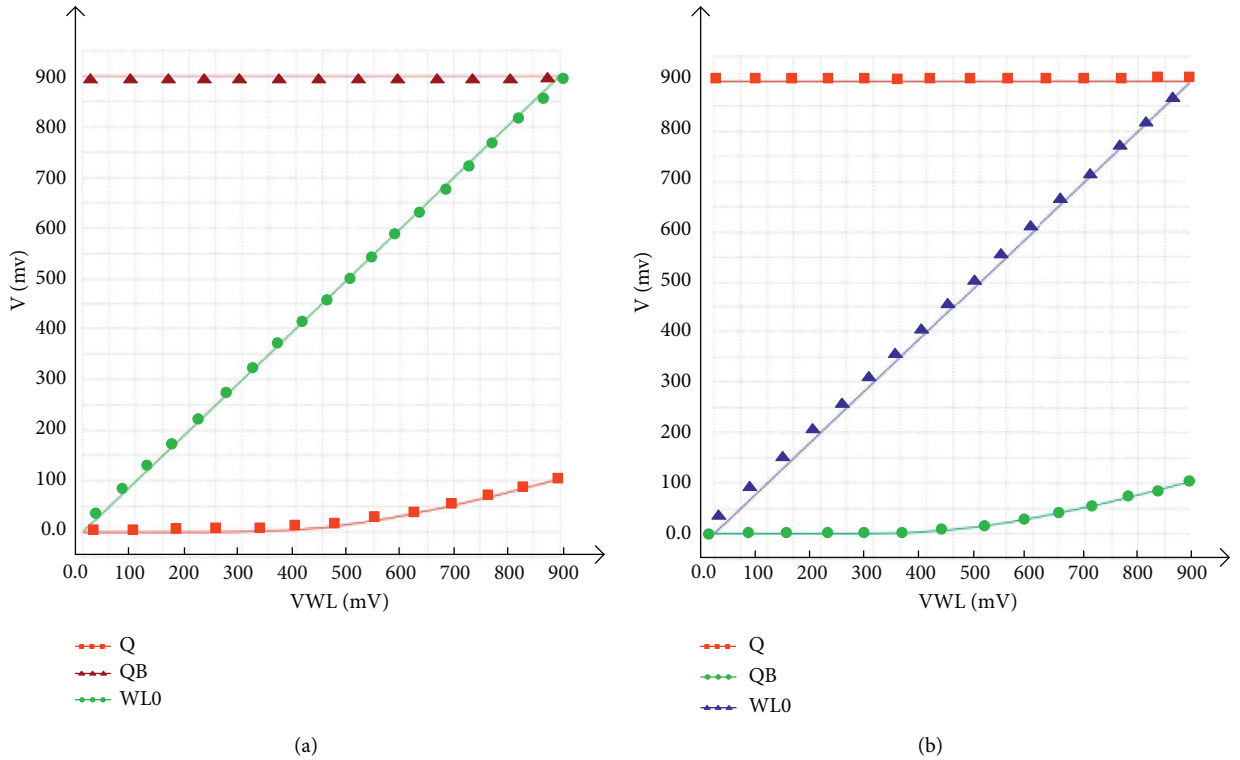

Figure 11: (a) Read 0 operation; (b) read 1 operation.

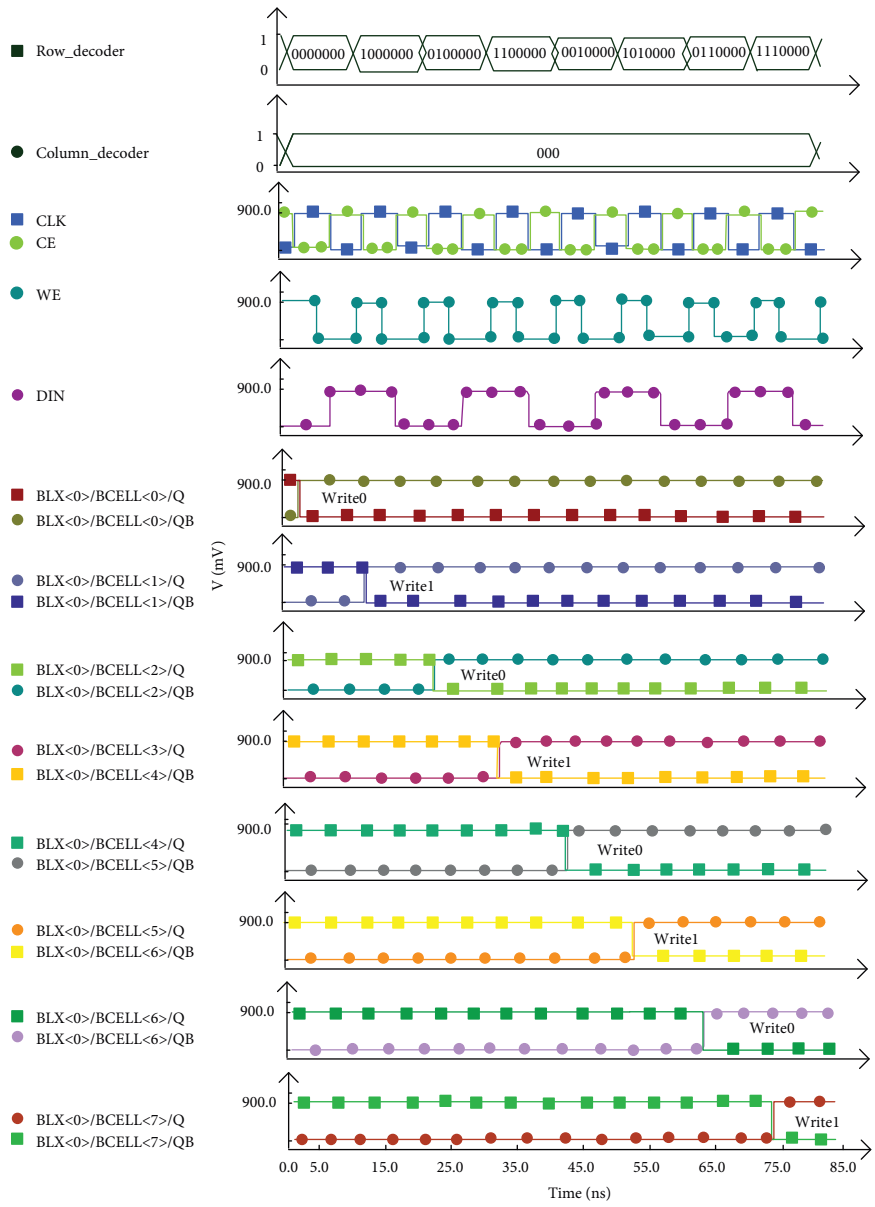

Figure 12: Result of writing data to 8 cells.

writes the data of the storage node to RRAM. When system enters the precharge mode, the data of SRAM storage node are lost. While entering restoration mode, the data are restored to the storage node of SRAM through the control circuit module and RBL drive module.

The performance comparison between our work and others is shown in Table 3. With the lowest power supply voltage, it adopts differential mode and has high density, and its characteristic size is the second smallest. It also has faster data storage and restoration time, which makes the data storage and restoration operation more efficient and reduces the risk of data loss.

The design of Reference [16] connects the upper electrode of RRAM to the latch node of SRAM and the lower electrode to the source of MOS transistor. At the same time, the drain is multiplexed with BL and BLB, respectively. The reuse of bit lines leads to the increase of parasitic capacitance, which increases the read delay of memory cell. In Reference [20], the upper electrode of RRAM is connected to drain, and the lower electrode is led out as a control signal. The high forming voltage will lead to high punch through voltage, which may damage the transistors. The 8T2R structure proposed parallels a pair of 1T1R RRAM cells on the latch nodes of 6T SRAM. The source of MOS transistor is

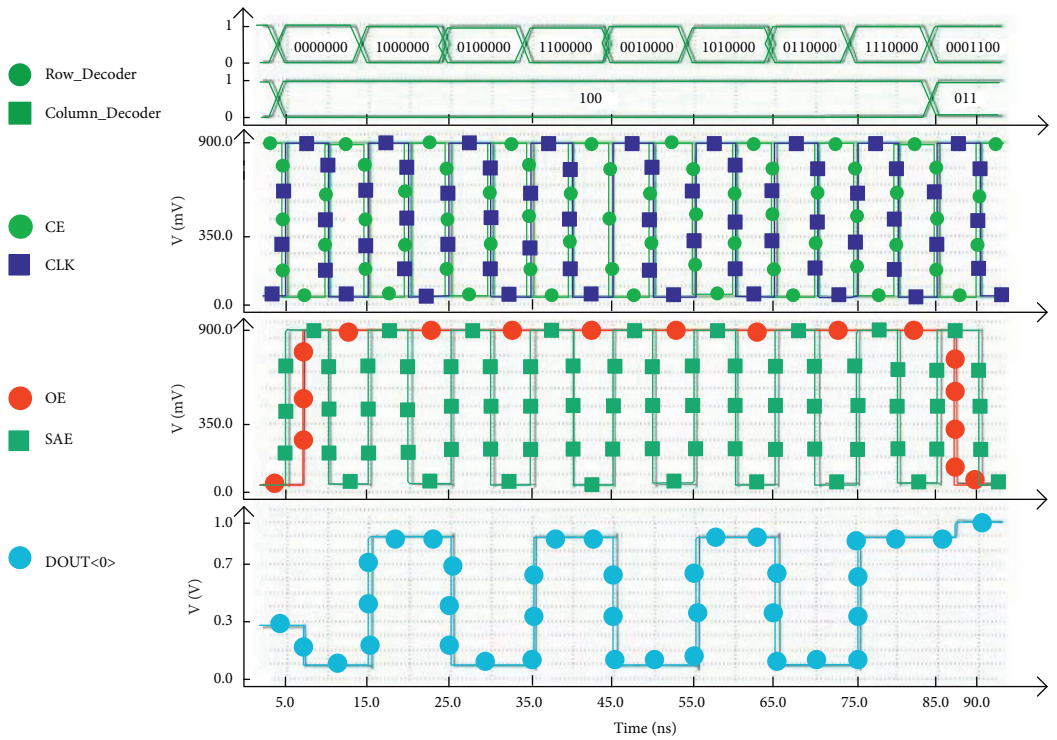

Figure 13: Result of reading data.

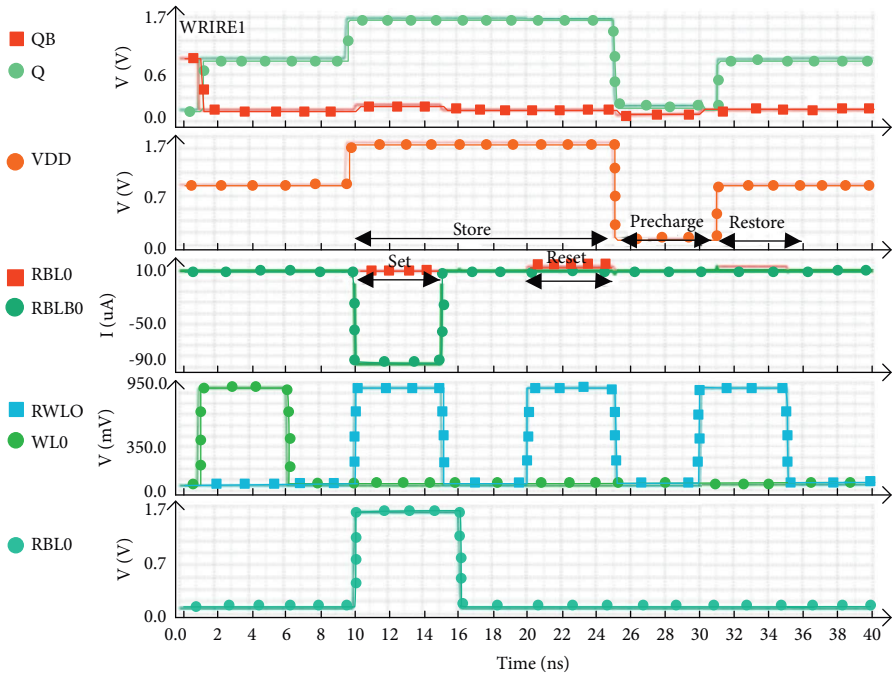

Figure 14: Result of data storage and restoration.

connected to the latch node of SRAM, and the drain is connected to the lower electrode of RRAM. The short current of the memory cell is suppressed by controlling the switch of MOS transistor. Meanwhile, the upper electrode of RRAM is directly used as the control signal (RBL and RBLB) to avoid damage to the device caused by excessive forming

Table 3: Performance comparison of different nvSRAM memory cells.

	This work	[7]	[9]	[18]	[19]
Memory cell	8T2R	8T2R	10T1R	7T1R	4T2R
Technology	28 nm CMOS	22 nm FDSOI	130 nm STM	90 nm CMOS	90 nm CMOS
Power supply	0.9 V	1 V	1.8 V	1 V	4 V
Restoration mode	Differential	Differential	Differential	Single	Differential
Nonvolatile mode	Before power failure	Before power failure	Before power failure	Before power failure	Real time
Store time	0.21 ns	0.24 ns	NA	10 ns (set + reset)	1.45 ns
Restoration time	0.18 ns	0.22 ns	NA	4 ns	0.02 ns
Current (when storing data)	0–200 μA	0–40 μA	0–50 μA	NA	0–230 μA
Voltage (when storing data)	1.6 V	1.0 V	1.8 V	1.5 V	1.5 V
Memory cell size	0.97 μm^2	5.44 μm^2	41 μm^2	1 μm^2	0.6 μm^2

voltage. The physical characteristics of RRAM are related to process. When the process deviates, the RRAM will initially be in a low-resistance state, resulting in device damage. During the layout design, dummy RRAM of different sizes will be added around the memory array to reduce the impact of process on RRAM. Affected by the advanced process, the development of Flash on the 28 nm node has also reached a bottleneck, so the RRAM technology of advanced process can make up for this shortcoming.

5. Conclusion

This study presents an improved 8T2R nvSRAM memory cell based on the RRAM technology for new nonvolatile and high-density memory applications. The memory cell is implemented with a UMC CMOS 28 nm 1p9m process. The experimental results show that when the power supply voltage is 0.9 V, the static noise margin is 0.35 V, the read noise margin is 0.16 V, and the write noise margin is 0.41 V. Its data store time is 0.21 ns and the data restoration time is 0.18 ns with an active area of only 0.97 μm^2. It shows that the overall performance is better than the current similar nvSRAM memory cells.

Data Availability

The raw/processed data required to reproduce this work cannot be shared at this time as the data also form part of an ongoing study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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