Hindawi
Active and Passive Electronic Components
Volume 2023, Article ID 3371599, 17 pages
https://doi.org/10.1155/2023/3371599

Research Article

Performance and Stability Analysis of Built-In Self-Read and Write Assist 10T SRAM Cell

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Received 17 February 2023; Revised 16 April 2023; Accepted 16 June 2023; Published 30 June 2023

Academic Editor: Gerard Ghibaudo

This work presents the performance and stability analysis of the proposed built-in self-read and write assist 10T SRAM (BSRWA 10T) for better performance in terms of thermal stability and fast write access, which is suitable for military and aerospace applications. The performance of the proposed SRAM cell dominates the previous SRAM cells, i.e., conventional, fully differential 10T-ST (FD 10T-ST), single stacked disturbance-free 9T-ST (SSDF 9T-ST). The proposed SRAM cell dominates the SSDF 9T-ST SRAM cell in terms of write ability. The built-in self-read and write assist structure of the memory cell also dominates the improved write ability of SSDF 9T-ST SRAM by assist circuits such as negative bit line, ultra-dynamic voltage scaling (UDVS), write assist combining negative BL, and V_{DD} collapse. The impact of assist circuits on write performance of memory cells is observed using Monte Carlo simulation for write margin (WM) parameter. WM of SSDF 9T-ST SRAM is improved by 15% and 25% by adding UDVS assist circuit and write assist combining negative BL and V_{DD} collapse circuit. But BSRWA SRAM cell itself can improve WM by 32% without any assist circuit. The impact of temperature variation on the performance of memory cells is observed using Monte Carlo simulation for the HSNM parameter. The deviation of HSNM for 15°C to 55°C is 14%, 5%, 4%, and 1% in conventional SRAM cell, FD 10T SRAM cell, SSDF 9T SRAM cell, and proposed BSRWA 10T SRAM cell, respectively. The proposed SRAM cell is designed at a 22 nm CMOS technology node and verified in the Synopsys Custom compiler. MC simulation results are monitored on Synopsys Cosmo-scope wave viewer.

1. Introduction

An SRAM cell is typically designed using nanoscale transistors to achieve a high integration density. As a result, SRAM's stability and write capabilities continuously deteriorate, and achieving a suitable yield with planar bulk metal-oxide semiconductors in 22-nm technology and beyond is extremely difficult [1].

The construction of a conventional 6T SRAM cell is quite simple. But the read and write stability of 6T SRAM has decreased due to increased threshold voltage fluctuations brought on by global and local process changes in modern CMOS processes. The major field of research for creating cutting-edge memory applications on chip SOC has long been energy-efficient and fast-accessing memory cell architectural design. Particularly, in military and aerospace applications, accurate memory operations are expected to be performed across a variety of temperature and resource limitations. Low power consumption and quick memory access are the two most important requirements for such applications [2]. Fast read and write operations are indeed critical factors in designing memory, and in this aspect, write assist circuits should be included in memory architecture. But it leads to area overhead. The area overhead is reduced by proper cell design with an in-built assist circuit to improve the access speed. The proposed BSRWA 10T SRAM cell is designed by taking reference from a shared-pass-gate 11T [3], low standby power 10T (LP10T) [4], energy-

efficient single-ended 10T (SE10T) [5] SRAM cells. The second criteria of designing the cell are the handling capability of half-select write failure issues. Half-select write failure issue occurs when a neighboring memory cell is unintentionally programmed along with the target cell. This can result in errors and data corruption, especially in high-density memory arrays. The proposed BSRWA 10T SRAM cell is proposed with proper design with a bit of interleaving structure to mitigate this issue.

ST-based inverter-structured SRAM cell is strong in terms of holding the data. The high HSNM cell structure of ST SRAM faces an issue with write ability. Write margin of SRAM cell needs to be improved along with HSNM and RSNM improvement. The performance improvement by the proposed SRAM is explained clearly using all circuit parameters such as read static noise margin, hold static noise margin, write margin, write trip current, write tip voltage, and data retention voltage. The data retention voltage parameter was extracted through HSNM plots.

This paper is organized as follows. The proposed built-in self-read and write assist 10T (BSRWA 10T) SRAM cell design and comparison with previous SRAM cell's operation are observed in Section 2. Write performance analysis of proposed BSRWA 10T, improvement of WM, write accessing speed, and thermal stability using MC simulations are observed in Section 3.

2. Proposed Built-In Self-Read and Write Assist 10T (BSRWA 10T) SRAM Cell Design and Comparison with Previous SRAM Cell's Operation

This section is organized as follows: read operation of BSRWA and stability analysis, which is compared by previous SRAM cells as shown in Section 2.1 [6, 7], hold operation of BSRWA and hold stability analysis, which is compared by previous SRAM cells as shown in Section 2.2 [8, 9], about write operation and write ability of proposed SRAM cell comparison with previous cells as shown in Section 2.3 [10, 11].

2.1. Proposed BSRWA 10T SRAM Cell's Read Mode of Operation. In advanced technology nodes, data retention of the memory cell is a crucial functional constraint during read access.

Lowering the supply voltage in the advanced technology nodes makes the memory cell less stable. Here, read SNM (RSNM) as a design metric is considered for stability analysis of memory cell operated in read mode. Read stability analysis for conventional, FD 10T-ST [12], SSDF 9T-ST, and proposed BSRWA 10T SRAM cells is performed. SRAM cells with high read stability can withstand the read disturbance. So read stability through "RSNM" is calculated by the SNM test model. SNM test model is created by updating the cell with two to four memory nodes (D, Db to D, Db, Db, Ddb) by breaking the feedback loop. Then, DC voltage transfer curves are plotted by keeping noise sources.

Figure 1(a) illustrates the read operation of the conventional memory cell, precharged BIT, and BITB lines able to disturb the core memory cell (D, Db) during an active WL signal. The read disturbance (Δv) is analyzed with the adjustment of cell ratio and observed as "$\Delta v'$" is brought to minimum through maximizing cell ratio. So pull-down transistor (MPDL) with maximum size may protect the cell from read disturbance, but it has a penalty as a write failure [13] and consuming area.

Figure 1(b) illustrates the read operation of the FD 10T-ST SRAM cell [12]; here, cell configuration focuses on stabilizing the inverter pair to withstand the read disturbance [12]. ST inverters have 2 levels of switching thresholds, and feedback transistors (MFBL, MFBR) attached to increase the switching threshold range for each inverter, which can improve the cell read stability. But "$\Delta v'$" can make MFBL conducts to a stacked node, which will reduce the conducting capacity of the stacked pull-down transistor. So chances of cell getting disturbed are more, which is strongly justified by the simulation shown in Figure 1(b). It is observed from VTC that they are not touching level-"0" when node-Db is maintained at a high level.

Figure 1(c) illustrates the read operation of the SSDF 9T-ST SRAM cell [14], and when the word line is active, precharged bit lines can disturb the core cell by accessing the transistor (MAXL). The strength of read disturbance (Δv) should not cross the level of the trip voltage; otherwise, read failure is caused.

SSDF 9T-ST SRAM cell configuration has one stacked conventional inverter and another ST inverter with a high switching threshold connected in a regenerative loop. Figure 1(c) illustrates the RSNM histogram for the proposed memory cell and corresponding butterfly curves (VTC of cross-coupled inverters). It is observed that node-D is strongly pulled to ground with transfer curves touches level-"0" when node-Db is maintained at a high level. So read failure is minimum in this proposed cell, which is also justified through the simulation result of the RSNM histogram shown in Figure 1(c). The Schmitt-Trigger (ST) inverter has enhanced the read stability of the FD 10T-ST [12] and SSDF 9T-ST SRAM cells. The proposed BSRWA 10T SRAM cell has better read stability when compared to the conventional, FD 10T-ST, SSDF 9T-ST. This is due to the following reasons.

Figure 1(d) illustrates the read operation of the proposed BSRWA 10T SRAM cell. WL is active, and the BIT line is precharged to "V_{DD}" as per the test bench setup for a read operation from the core memory cell. The precharged bit line does not disturb the node-SD through MAXR, M_{NR1} when it holds "1." But in the case of node-SDb holds "0," the strength of "Δv" depends on "ON" resistance of M_{NR1}. "Δv" may disturb the memory cell in the conventional structure, but build-in self-read assist in the proposed memory cell has strong pull-down mechanism through M_{NR2} when M_{NR1} offers high "on" resistance in the worst case. So node-D is strongly pulled down to logic level-0 which strongly holds the SD node also at logic level-0 through the feedback network. Node-D (at level-0) holds the node SDb at logic level-1. So pull-up network becomes very weak (M_{PRS} is off)

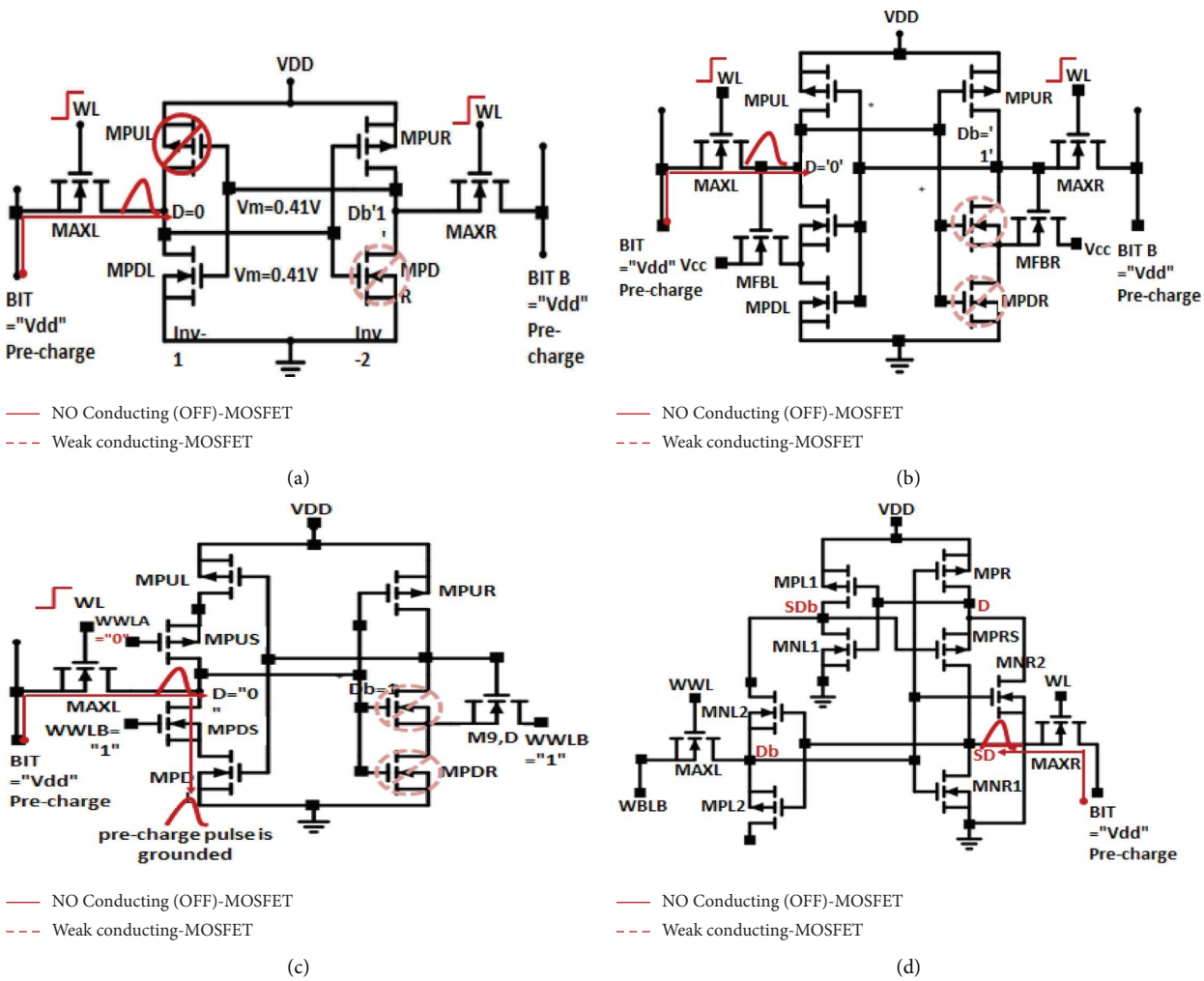

Figure 1: Operation of different memory cells during read mode: (a) conventional memory cell, (b) FD 10-ST memory cell, (c) SSDF 9T-ST memory cell, and (d) proposed BSRWA 10T memory cell.

to boost the node-SD; simultaneously, node-Db also makes the pull-down strong. So the read disturbance is reduced by read assist cell architecture.

Histogram plot of RSNM and VTC of conventional, FD 10T-ST, SSDF 9T-ST, and proposed BSRWA 10T SRAM cells is plotted and observed in Figures 2(a)–2(d), respectively. These VTC are plotted on V (D), V (Db) axis, now shifted into v (U), V (V). Butterfly curves are generated by using VTC plotted on V (D), V (Db) and inverted VTC plotted on V (U), V (V) (for swapping).

From Figures 2(a)–2(d), it is observed that node-SDb strongly pulled to the ground and transfer curves touch level-"0" when node-D/SD maintained at a high level for SSDF 9T-ST and proposed BSRWA 10T SRAM cells only. So read failure is minimum in this proposed cell.

2.2. Proposed BSRWA 10T SRAM Cell's Standby Mode of Operation. In advanced technology nodes, data retention of the memory cell is a crucial functional constraint during standby. Lowering the supply voltage in the advanced technology nodes makes the memory cell less stable. So hold SNM (HSNM) is considered as a design metric for stability analysis of memory cells operating on standby. Hold stability analysis for conventional, FD 10T-ST, SSDF 9T-ST, and proposed BSRWA 10T SRAM cells is performed using HSNM. HSNM is calculated using the SNM-test model and butterfly plots (DC voltage transfer characteristic curves) as shown in Figure 3. The hold stability of a conventional SRAM cell is observed as 0.35 V for supply voltage at 1 V. Hold stability is improved by the design of SRAM cells with ST inverters. ST inverters have multiple switching thresholds.

So disturbance at one end of the inverter may not disturb the other end inverter easily. So FD 10T-ST and SSDF 9T SRAM cells are designed with better HSNM as 0.46 V and 0.68 V. But sharing voltage across each transistor is reduced due to increasing the count of stacked transistors from supply to the ground (M_{PDL}, M_{PUL}, and stacked transistor in FD 10T, M_{PUL}, M_{PUS}, M_{PDS}, and M_{PDL} in SSDF 9T). HSNM is not maximum due to the limited driving strength of memory nodes. The proposed BSRWA SRAM cell design is suitable for maintaining better stability as 0.72 V avoiding stacking structure and adding a strong pull-down path through transistor M_{NR2}.

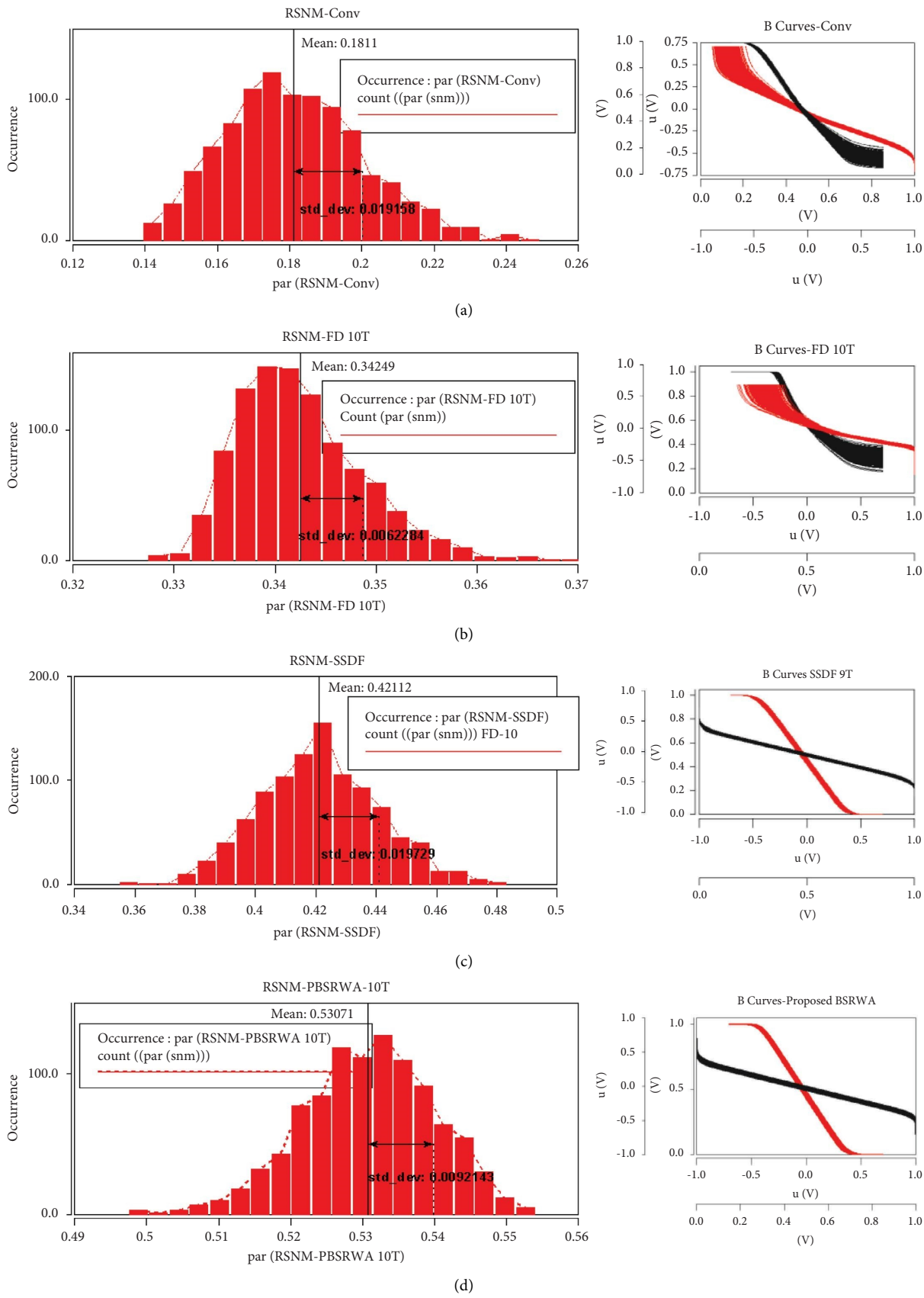

Figure 2: Histogram plot of RSNM from Monte Carlo simulation (1K samples) along read disturbance analysis using VTC of (VTC's) of (a) conventional memory cell, (b) FD 10-ST memory cell, (c) SSDF 9T-ST memory cell, and (d) proposed BSRWA 10T memory cell.

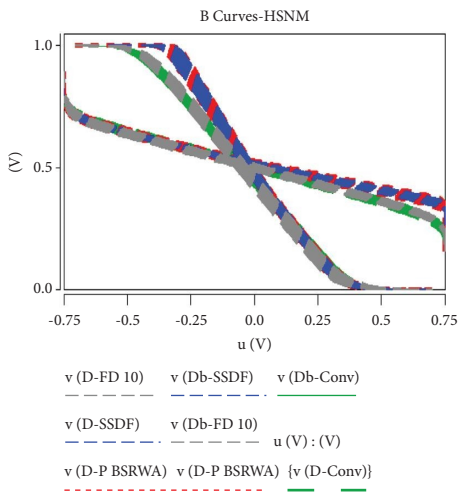

Figure 3: Hold mode-VTC of cross-coupled inverters of each SRAM cell as butterfly plots to calculate HSNM.

HSNM under super threshold ($V_{DD} = 0.6$ V) and near-threshold ($V_{DD} = 0.4$ V) is observed as supply voltage reduces hold stability is reduced. This feature of varying HSNM with supply operating voltage is used for the fast write operation. This concept is explained in Section 3.

2.3. Proposed BSRWA 10T SRAM Cell's Write Mode of Operation. Write operation is performed for conventional, FD 10-ST, SSDF 9T-ST memory cells. Memory nodes of each memory cell are updated with write data during the write operation. Ultradynamic voltage scaling (U-DVS), negative bit line (NBL) [15], and write assist combining negative BL and V_{DD} collapse [16] circuits are designed to improve the write performance. Write operation for SSDF 9T-ST SRAM cell using write assist combining negative BL and V_{DD} collapse is shown in Figure 4. The control signals are Colgen, Boost1, and Boost2 are generated at the architecture level throughout row and column by row and a column address decoder. Supply scaling and negative bit line mechanisms are introduced during the write operation. Transistors (P1, P2, N1, N2, N3) are turned "on" and "off" by control signals in the assist circuit to provide a scaled supply voltage (V_{COL}) to reduce the stability, and simultaneously, the assist circuit is also provided negative bit line voltage to increase the driving strength of accessing transistor ($V_{GS\text{-}AXR} = V_{WL} - V_{BIT} =$ increased, when V_{BIT} is negative).

The write performance of the previous SSDF 9T-ST SRAM cell is improved by the assist circuit as shown in Figure 4 [17]. But generating controlling signals (colgen, boost1, boost2) by the external circuit is becoming complex. The proposed BSRWA 10T SRAM cell, by virtue of its integrated self-write assist feature, can enhance write performance on its own. Thus, the overhead of the external write assist circuit and control signals is optimized. Figure 5(a) illustrates the write-"0" operation of the proposed BSRWA 10T SRAM cell.

Enabling WL, WWL, and WBLB with logic-"1" and BL with logic-"0" are the initial conditions for performing the write-"0" operation. Active WBLB tries to bring the node-Db to a high level, which turns off the M_{PR}. So node-D discharges freely and strongly pulled down through M_{NR2} without having any disturbance from the charging path. Strongly pulled-down node-D turns M_{PL1} on and generates strong logic-1 at node-SDb. The strong logic-1 at SDb turns off the M_{PRS}, so node-SD discharges freely and is strongly pulled down through M_{NR1} without any disturbance from the charging path. So memory node (D) and stacked memory node (SD) are written with logic-0. Similarly, enabling WL, WWL, and BL with logic-"1" and WBLB with logic-"0" are the initial conditions for performing the write-"1" operation. Active low WBLB tries to bring the node-Db to the low level, which turns on the MPR and turns off the M_{NR1}. So node-D charges freely and strongly pulled up through MPR without having any disturbance from discharging path through M_{NR1} and M_{NR2}. Node-D at logic-"1" turns M_{NL1} on and generates strong logic-0 at node-SDb. The strong logic-0 at SDb turns on the MPRS, so node-SD is also pulled down through MPRS. So memory node (D) and stacked memory node (SD) are written with logic-1. Figure 5(b) illustrates the write-"1" operation of the proposed BSRWA 10T SRAM cell. Enabling WL, WWL, and BL with logic-1 and WBL with logic-"0" are the initial conditions for performing the write-"1" operation.

V_{SS} is pulled to the high level, which turns off the M_{PRS}. Active word line makes M_{AXR} turn on, which allows node-D charge from BL. When node-D is charged, M_{PL2} gets turned off which allows the node-Db discharges to WBL through M_{AXL}. So node-Db with logic-0 turns on the M_{PR} which can boost the node-SD. Boosted node-SD discharges node-SDb using M_{PL1}, M_{NL1} inverter.

Pull-down path for write-0 in SSDF 9T-ST SRAM cell

$$\begin{aligned} \mathbf{V_{BL}} &= \mathbf{V_{ODMAXR}} + \mathbf{V_D}, \\ \mathbf{V_D} &= \mathbf{V_{ODMPDSL}} + \mathbf{V_{ODMPDL}}. \end{aligned} \tag{1}$$

Pull-down path for write-0 in proposed SRAM cell

$$\begin{aligned} \mathbf{V_{BL}} &= \mathbf{V_{ODMAXR}} + \mathbf{V_{SD}}, \\ \mathbf{V_{SD}} &= \mathbf{V_{ODMNR1}}, \\ \mathbf{V_D} &= \mathbf{V_{ODMNR2}}. \end{aligned} \tag{2}$$

Due to the stacking of multiple transistors (M_{PDSL} and M_{PDL}), the pull-down path is not strong towards the ground. So write bit voltage change is not strongly reflected across node-D in the SSDF-9T SRAM cell [14]. This problem is avoided in the proposed SRAM cell with a single transistor clamped at bias ground level in a pull-down path. So write bit voltage change is strongly reflected in the proposed SRAM cell.

The transient response of the proposed BSRWA 10T SRAM cell during a write operation is shown in Figure 6. There is a successful write operation along with write failure cases depending on the adjustment of oxide thickness of M_{PL2}, $M_{NL2.}$ Smaller oxide thickness (T_{OX}) gives a higher oxide capacitor (C_{OX}) and a higher gate capacitance (C_G), so control of the gate on a channel is more in this case for thin-box-SOI as shown in Figure 7. So node-Db responds immediately to node-D changes [18].

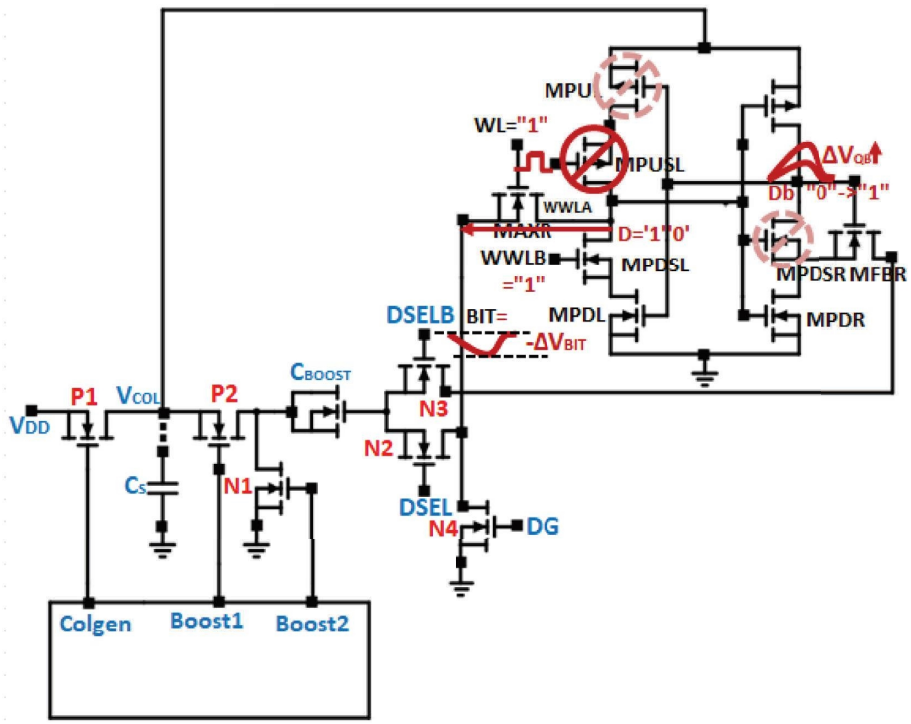

Figure 4: Write operation of SSDF 9T-ST SRAM cells with assist circuits.

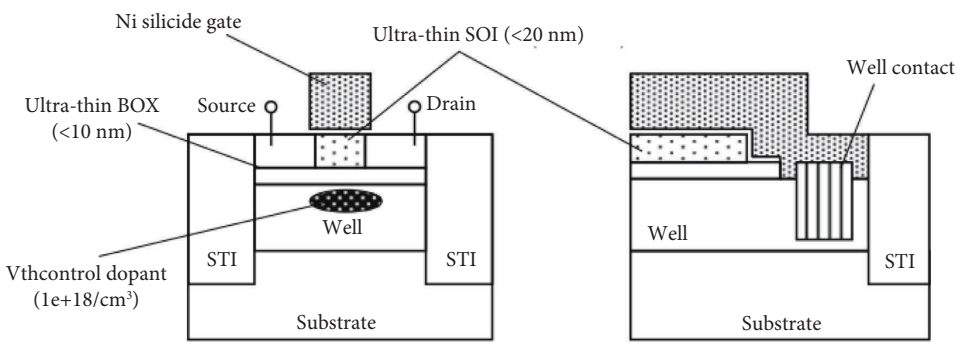

Figure 5: Thin-box FD-SOI (thin buried oxide, fully depleted silicon on insulator).

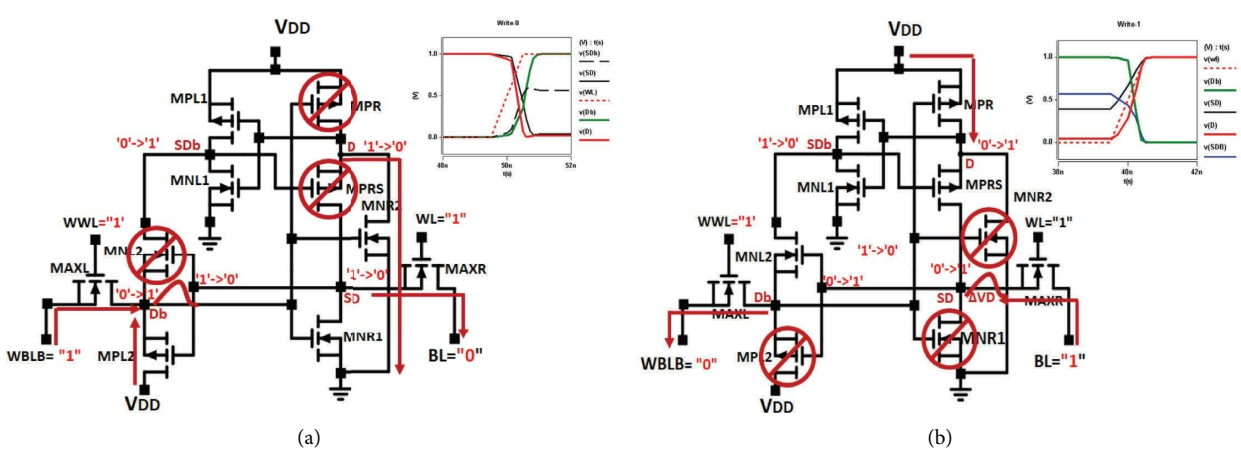

Figure 6: Proposed BSRWA 10T memory cells: (a) write "0" operation and (b) write "1" operation.

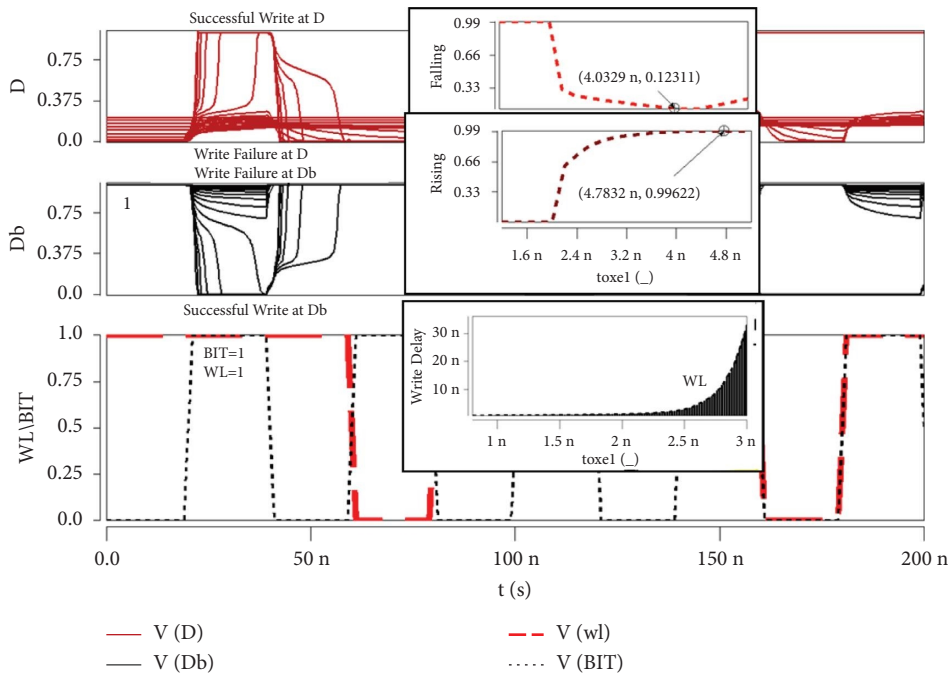

Figure 7: Timing diagram of successful write operation along with write failure cases under the observation of oxide layer thickness variation.

Figure 6 illustrates the successful write-"1" operation with node-D, node-Db updated with logic-"1," logic-"0," respectively. But some write failure cases and maximum delays are observed for increasing the value of T_{OX} ($T_{OX} > 1.7$ nm).

$$V_{TH} = \frac{\sqrt{2qN_A\varepsilon(2\varnothing_B)}}{C_{OX}} + 2\varnothing_B + V_{FB},$$
$$\sigma_{Vth\_shift} = \frac{2.45X10^{-9}}{\sqrt{WXL}}, \tag{3}$$
$$V\text{th}_{\text{shift}} = \text{agauss}\left(v\text{th}, 3X\sigma_{V\text{th}_{\text{shift}}}, 3\right).$$

The Gaussian distribution function of threshold voltage variation is considered as a sample for MC simulation (σ_{Vth_shift}). Occurrence plots are extracted with respective environmental and device parameters [19].

3. Results and Discussion

In this section, the performance of the proposed BSRWA 10T SRAM cell is analyzed using the following parameters. The proposed BSRWA 10T SRAM cell results are compared with previous SRAM cells with assist circuits. This section concludes that the proposed SRAM cell's performance is better than previous SRAM cells through the following simulation results. This section also concludes that the improved performance in conventional SRAM cells by assist circuits can be dominated by the performance of the proposed BSRWA 10T SRAM cell.

3.1. Write Performance Analysis Using WM Parameter. Write margin (WM) is a parameter to measure the ability and performance of the write operation. Write operation of previous SRAM cells and proposed SRAM cell is observed in previous sections. In this section, the performance of the write operation and comparison results with previous SRAM cells is observed.

Write-ability performance analysis of memory cell through the "WM" parameter and occurrence of WM for proposed BSRWA SRAM cell with reference to previous SRAM cell (SSDF SRAM cell) is observed in Figure 8. The histogram plot of MC simulation for SSDF SRAM cell, SSDF SRAM cell with UDVS assist circuit [20, 21], SSDF SRAM cell with NBL assist circuit [15], and the proposed BSRWA SRAM cell is observed in Figure 8. The improvement of WM for SSDF SRAM cell [14] is 15.7% (WM = 0.38 V to 0.44 V) by UDVS assist circuit [20, 21] and 26.1% (WM = 0.38 V to 0.484 V) by the NBL assist circuit [15]. But the proposed BSRWA SRAM cell has an improvement of WM performance is 34.2% (WM = 0.38 V to 0.510 V) due to built-in self-write assist configuration. The write performance of the proposed SRAM cell is dominating the previous SRAM cells with the assist circuit's performance also.

3.2. Write Performance Analysis Using Write Trip Current (WTI) and Branch Current Analysis to Measure WTI through $\mathbf{I_{NC}}$. In this section, write trip voltage (WTV) and write trip current (WTI) are the parameters used to measure the ability and performance of the write operation [7]. To explore the individual transistor's effect on trip current, all the branch currents around the internal node-D can be measured in response to the voltage sweep. The pull-up branch, forced

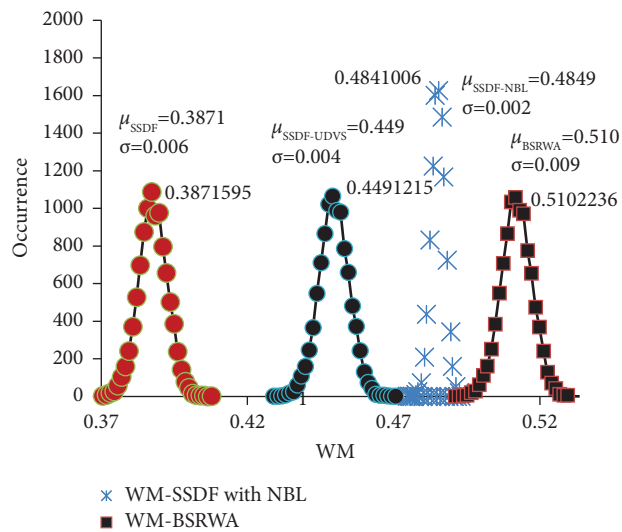

Figure 8: Write-ability performance analysis of memory cell through "WM" parameter and histogram graph of WM.

voltage source, and accessing transistor branch supply the current towards node-D; simultaneously, the pull-down branch draws the current from node-D to the ground. The direction of these branch currents changes based on the data stored in the SRAM cell. WTV and WTV are measured using *N*-curves [22], which are nothing but I–V characteristics of forced voltage source at memory node (Db = 0) for conventional, FD 10-ST, SSDF 9T-ST, and proposed BSRWA 10T SRAM cells are shown in Figures 9(a)–9(d), respectively. The strength of the N-curve current ($\mathbf{I_{NC}}$) suggests the behavior of memory cell. *N*-curve dropped during trip the memory cell. The minimum level of $\mathbf{I_{NC}}$ is notated as WTI.

$$\mathbf{I_{NC}} = \mathbf{I_{PU}} + \mathbf{I_{PD}} + \mathbf{I_{AX}}. \quad (4)$$

Write performance is improved by reducing the level of WTV. "WTV" is nothing but the minimum voltage required to flip the cell with write data.

The response of forced node current *(I_{NC})* for multiple voltage sweep parameters and multiple cell structures is shown in Figure 9. The primary sweep parameter is forced node voltage, and the secondary sweep parameter is V_{BLB}. The trip current level is calculated for different sweep voltage levels of V_{BLB}. When WTI is observed, "0" is the indication of data write. So write behavior of SRAM cells is observed based on WTI occurrence plots as shown in Figure 10. WTI depends on V_{BLB}. WTI occurrence plots are shifted right and reach to level-0 at WTV [23].

Figure 11 illustrates that the WTI occurrence plots of conventional, FD 10-ST, SSDF 9T-ST, and proposed BSRWA 10T SRAM cells at V_{BLB} is $V_{DD.}$ WTI is measured from the above occurrence plots and observed as the level of WTI is near "0" in the proposed BSRWA 10T SRAM when compared to previous SRAM cells as shown in Table 1. Write-ability of a bit cell indicates how easy or difficult it is to write to the cell. Write-trip-point defines the maximum bit-line voltage V_{BIT} – MAX needed to flip the cell content. The higher the bit-line voltage, the lower the write-trip-point, and the easier it is to write to the cell.

$$\text{Normalized Write} - \text{Trip} - \text{Point} = V_{DD} - V_{BIT-MAX}. \quad (5)$$

3.3. Thermal-Stability Analysis Using HSNM and Data Retention Voltage (DRV) during Hold Mode of Operation. In this section, thermal stability analysis is performed using the HSNM parameter. The justification of thermal stability for the proposed SRAM cell is as follows. Node-Db is connected to the ground through M_{NR1} in the pull-down path. During the read and hold mode of operation, the deviation of electrical voltage strength at node-DB due to M_{NR1} gets compensated by the change of electrical voltage strength at node-D due to a similar transistor M_{NR2}. The electrical properties of M_{NR1} and M_{NR2} are the same, so both transistors respond similarly to temperature change. So thermal stability of the proposed BSRWA 10T SRAM cell compared to previous SRAM cells is high, due to the compensation structure. The effect of temperature change from 15°C to 55°C on stability is observed with SNM occurrence histogram plots using Monte Carlo simulation as shown in Figure 12 [25]. The improvement of hold stability by the proposed BSRWA 10T SRAM compared with previous SRAM cells is observed in Table 2.

During the hold mode of operation, cell stability depends on the supply voltage. Cell stability is reduced by scaling the supply voltage. Data retention voltage is defined as the minimum operating voltage required by the cell for holding data. The proposed BSRWA 10T SRAM cell is simulated under different operating voltages and corresponding VTC, and HSNM occurrence plots are captured in Figure 13.

3.4. Write Delay Analysis. In this section, the performance of the proposed SRAM cell during the write operation and comparison results with previous SRAM cells are observed. Write-ability performance analysis of memory cells is through the "write delay" parameter [10].

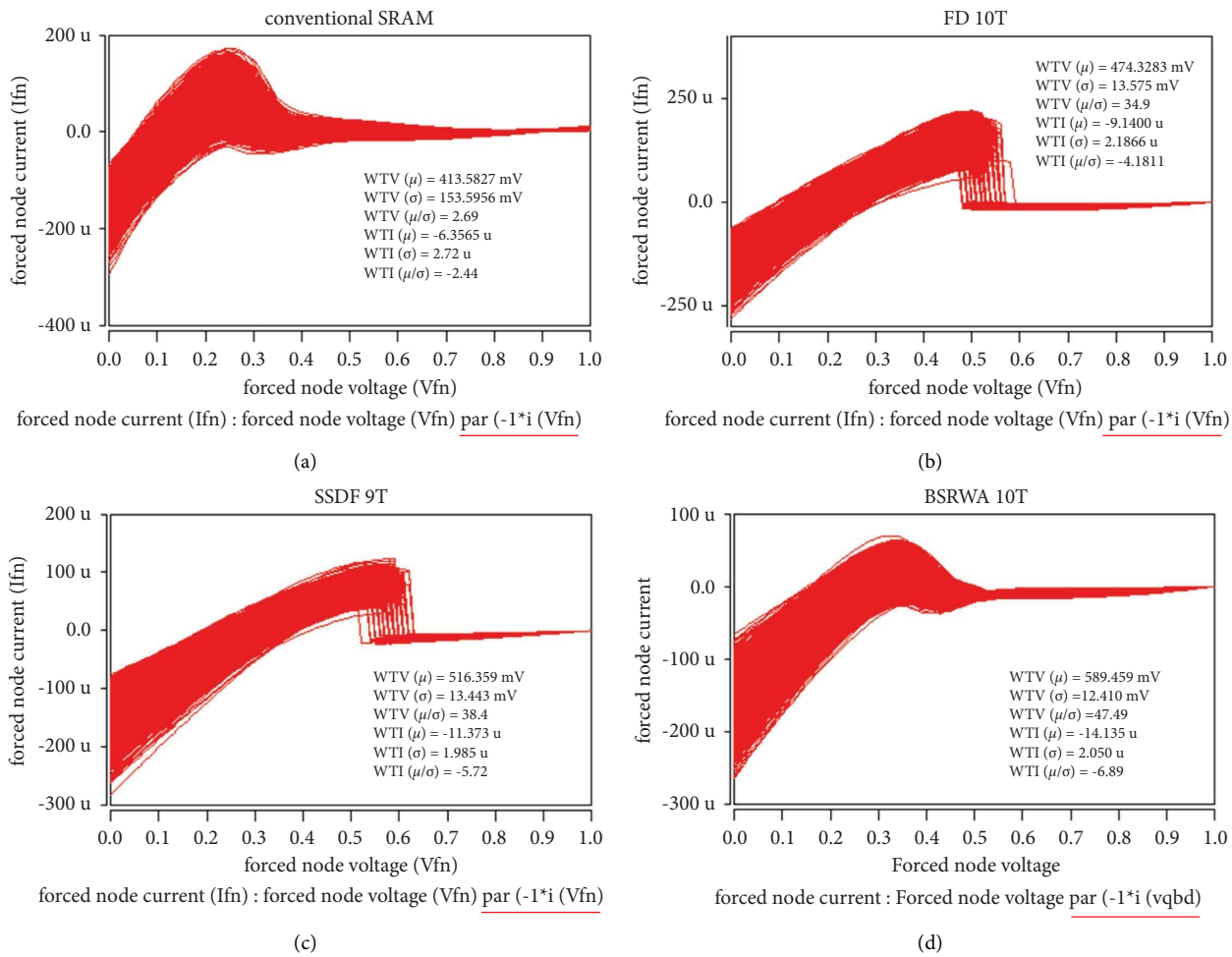

Figure 9: *N*-curve plots for (a) conventional memory cell, (b) FD 10-ST memory cell, (c) SSDF 9T-ST memory cell, and (d) proposed BSRWA 10T memory cell.

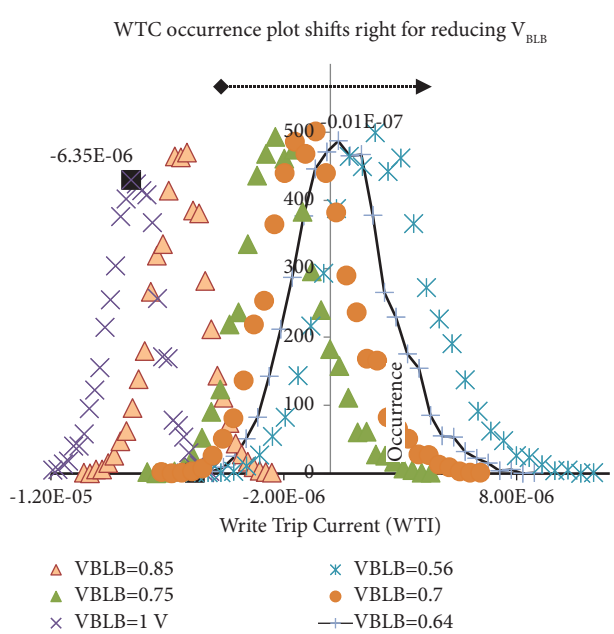

Figure 10: Write trip voltage (WTV) calculation using write trip current occurrence plots.

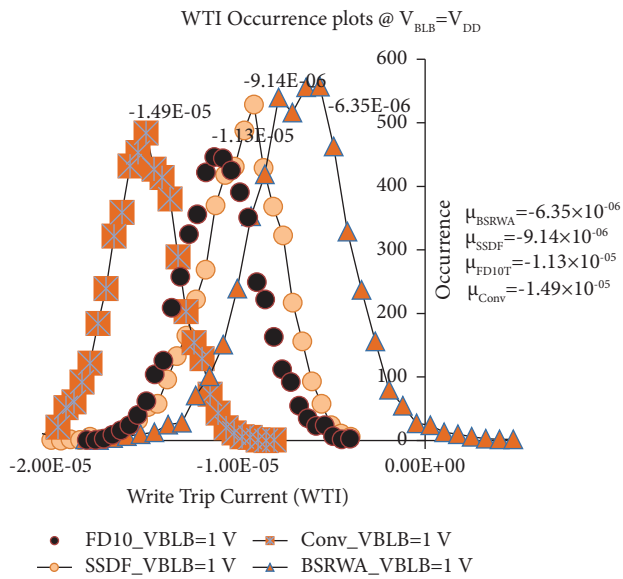

Figure 11: Write trip current occurrence plots extraction for all SRAM cells using Monte Carlo simulation at $V_{BLB} = V_{DD}$.

Table 1: Write-ability analysis through WTI, WTV, and WTP.

	$WTI_{@BLB = VDD}$ (amp)	$WTV_{@WTI = 0}$ (V)	WTP (V)
Conv-6T	-1.49×10^{-05}	0.49	0.51
FD-10T	-1.13×10^{-05}	0.54	0.46
SSDF	-9.14×10^{-06}	0.59	0.41
HSLE-10T [24]	-7.85×10^{-06}	0.61	0.39
SPG-11T [3]	-8.73×10^{-06}	0.58	0.42
Prop BSRWA	-6.35×10^{-06}	0.64	0.36

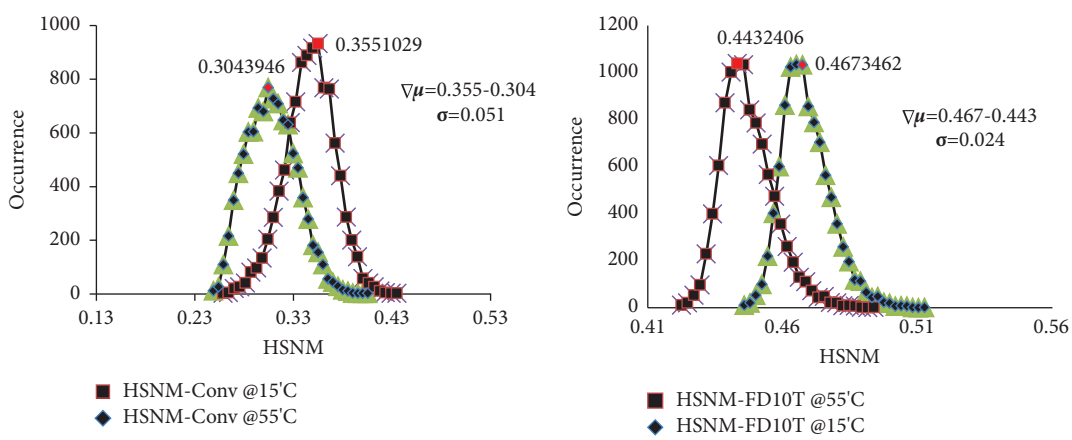

Figure 12: Continued.

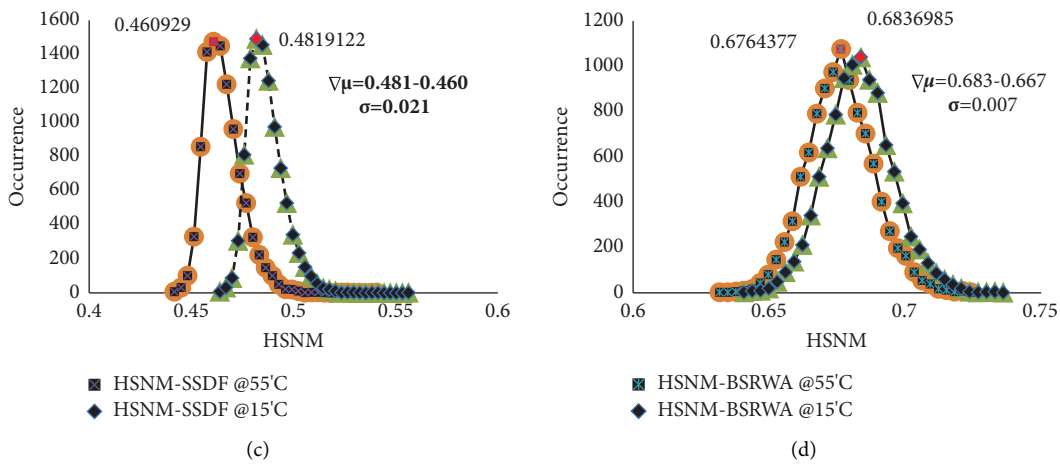

Figure 12: Hold thermal stability analysis of memory cell through "HSNM" parameter and histogram graph of (a) conventional memory cell, (b) FD 10-ST memory cell, (c) SSDF 9T-ST memory cell, and (d) proposed BSRWA 10T memory cell.

The write delay of the SRAM cell refers to the time taken to write new data into the cell after the write enable signal has been applied. The write delay depends on the size of the cell; i.e., area capacitance decides the delay. The write operation of BSRWA 10T SRAM cell through transient response (transient waveform) is shown in Figure 14. The occurrence of the delay parameter for the proposed BSRWA SRAM cell with reference to the previous SRAM cell (SSDF SRAM cell) is shown in Figure 15, and measured values are observed in Table 2.

3.5. Write Half-Selected Cell Stability. The paragraph describes a proposed SRAM cell, called BSRWA 10T, that eliminates the problem of write-half-select disturb in a bit-interleaving structure. The paragraph explains how the proposed SRAM cell works in four different situations during a write operation, including selected, hold, column half-selected, and row half-selected cells as shown in Figure 16.

For the column half-selected cell, the storage nodes are decoupled from BL, so memory node-D, SD gets not disturbed. For the row half-selected cell, corresponding WL, WBLB, and BL are tied to VDD. If the row half-selected cell stores "1," both D and SD remain at "1," and the stored data can be latched safely with any disturbance because node-D and BL are at the same level. If the row half-selected cell stores "0," SD gets charged to "1" through M_{AXR} by BL. But node-D pulled down to ground level through M_{NR2}, so node-D holds "0," which holds the M_{PRS} in off state through an inverter (M_{PL1} and M_{NL1}). So node-SD is isolated from the core memory node (D). Therefore, the stored data in the row half-select cell can also be latched safely. The proposed BSRWA SRAM cell operates with a bit-interleaving structure free of write-half-select disturb. Half-selected cell stability is also improved by SPG11T SRAM cell [3]. But the cell is controlled with extra control inputs such as RWL and VSS and also connected with extra transistors to generate SLB. So extra circuitry requires to generate extra control signals, which leads to more dynamic power dissipation. The proposed BSRWA SRAM cell operates with a bit-interleaving structure free of write-half-select disturb. Half-selected cell stability is also improved by SPG11T SRAM cell [3]. But the cell is controlled with extra control inputs such as RWL and VSS and also connected with extra transistors to generate SLB. So extra circuitry requires to generate extra control signals, which leads to more dynamic power dissipation.

3.6. Cell Area. Figure 17(b) shows the layout of the proposed BSRWA 10T SRAM cell which is compared with previous SRAM cells. Table 3 shows the sizing details of all SRAM cells, where width proportion ($w1$) is the Gaussian parameter for MC simulation. The observation from Figures 17(a) and 17(b) proposed BSRWA 10T SRAM cell area ($0.625 * 0.925\,\mu\text{m} = 0.57\,\mu\text{m}^2$) is 1.26 times (1.1X) of SSDF ($0.600\,\mu\text{m} * 0.750\,\mu\text{m} = 0.45\,\mu\text{m}^2$). The proposed cell needs 1.26 times more chip area, but it is having an advantage in saving the area overhead by assist circuits design because BSRWA 10T SRAM cell has better performance with the built-in self-assist circuit in the cell design itself.

Table 2: SRAM cell design parameters comparison among different SRAM cells.

	Write-0 $T_{d(P\ sec)}$	Write-1 $T_{d\ (P\ sec)}$	MC simulation (P sec)			HSNM@15°C			HSNM@55°C			ΔHSNM	DRV	RSNM
			(μ_{Td})	(σ_{Td})	$(\mu/\sigma)_{Td}$	(μ_{HSNM})	(σ_{HSNM})	$(\sigma/\mu)_{HSNM}$ (%)	(μ_{HSNM})	(σ_{HSNM})	$(\sigma/\mu)_{HSNM}$ (%)	(mV)	(mV)	(mV)
Conv-6T	531	491	382.72	91.54	4.18	0.355	0.037	10.63	0.304	0.033	11	50.7	618	181
FD-10T	481	424	364.93	88.90	4.08	0.467	0.019	4.23	0.443	0.020	4.6	24	480	342
SSDF-9T [11]	391	329	331.2	84.76	3.90	0.481	0.0197	4.10	0.460	0.021	4.5	21	492	421
HSLE-10T [24]	321	278	331.2	81.31	3.81	0.471	0.020	4.23	0.443	0.02	4.2	27	481	442
SPG-11T [3]	312	237	273.2	79.76	3.71	0.483	0.016	3.39	0.47	0.019	4.05	13	429	463
SSDF with UDVS + NBL	302	291	281.2	74.77	3.76	0.481	0.0197	4.10	0.460	0.021	4.5	21	492	421
Prop BSRWA	291	187	271.77	73.6	3.59	0.683	0.014	2.09	0.676	0.015	2.25	7	412	530

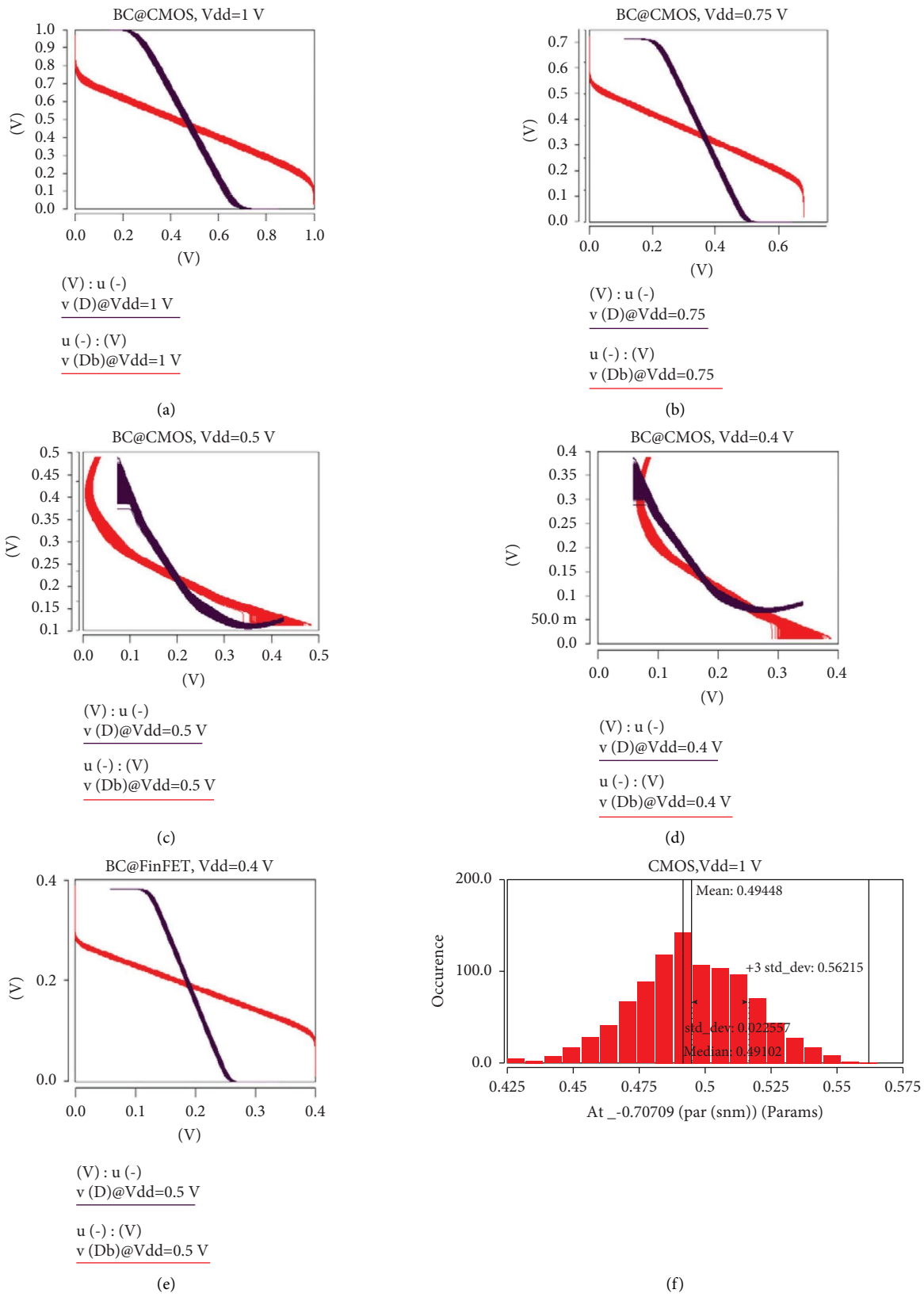

Figure 13: Continued.

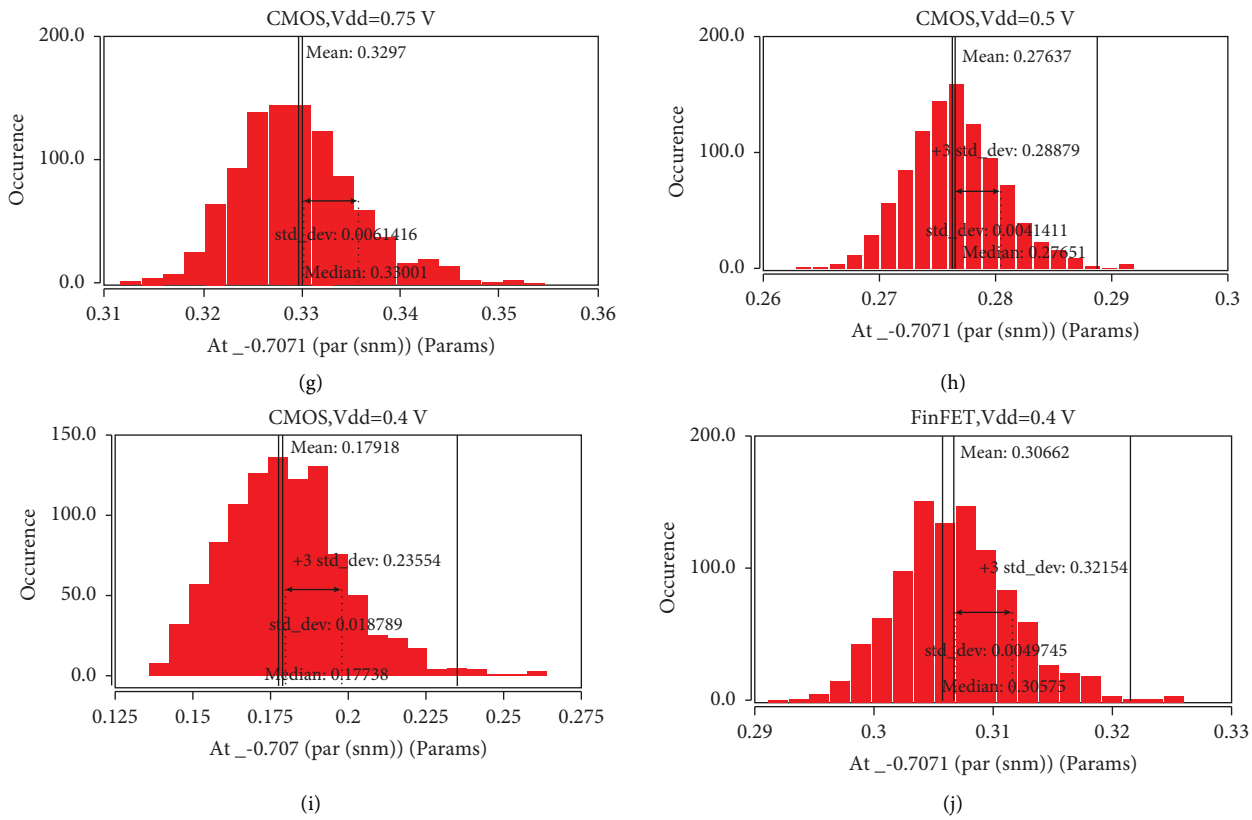

Figure 13: DRV calculation through HSNM and butterfly curves of proposed BSRWA 10T SRAM cell.

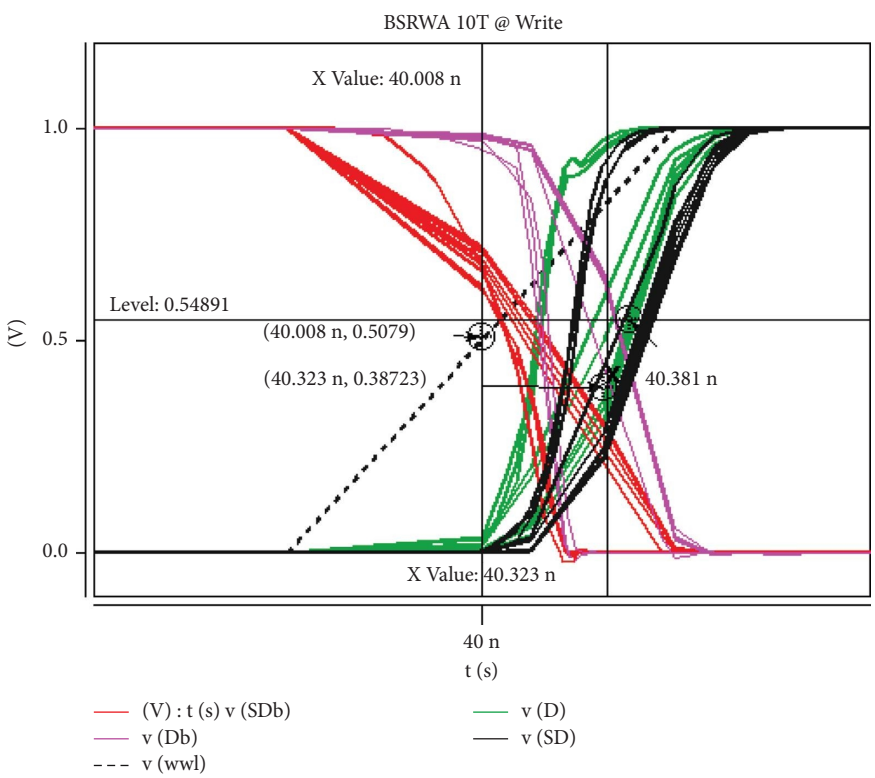

Figure 14: Write access delay for BSRWA 10T SRAM cell.

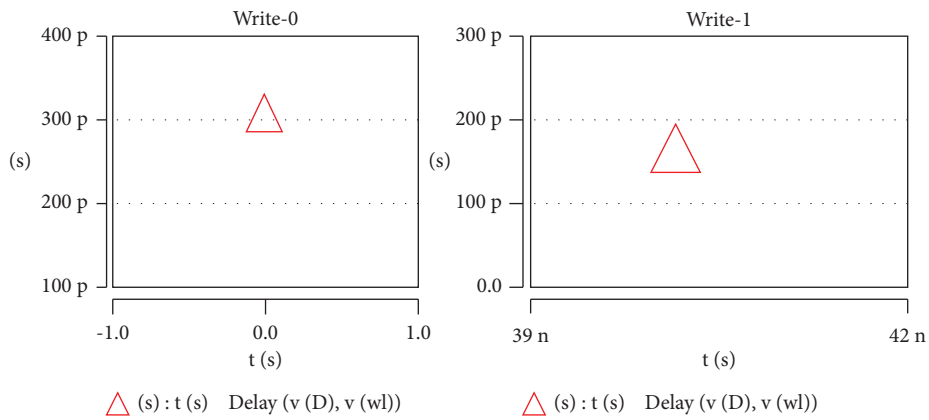

Figure 15: Write access delay for write-"0" and write-"1" operations by BSRWA 10T SRAM cell.

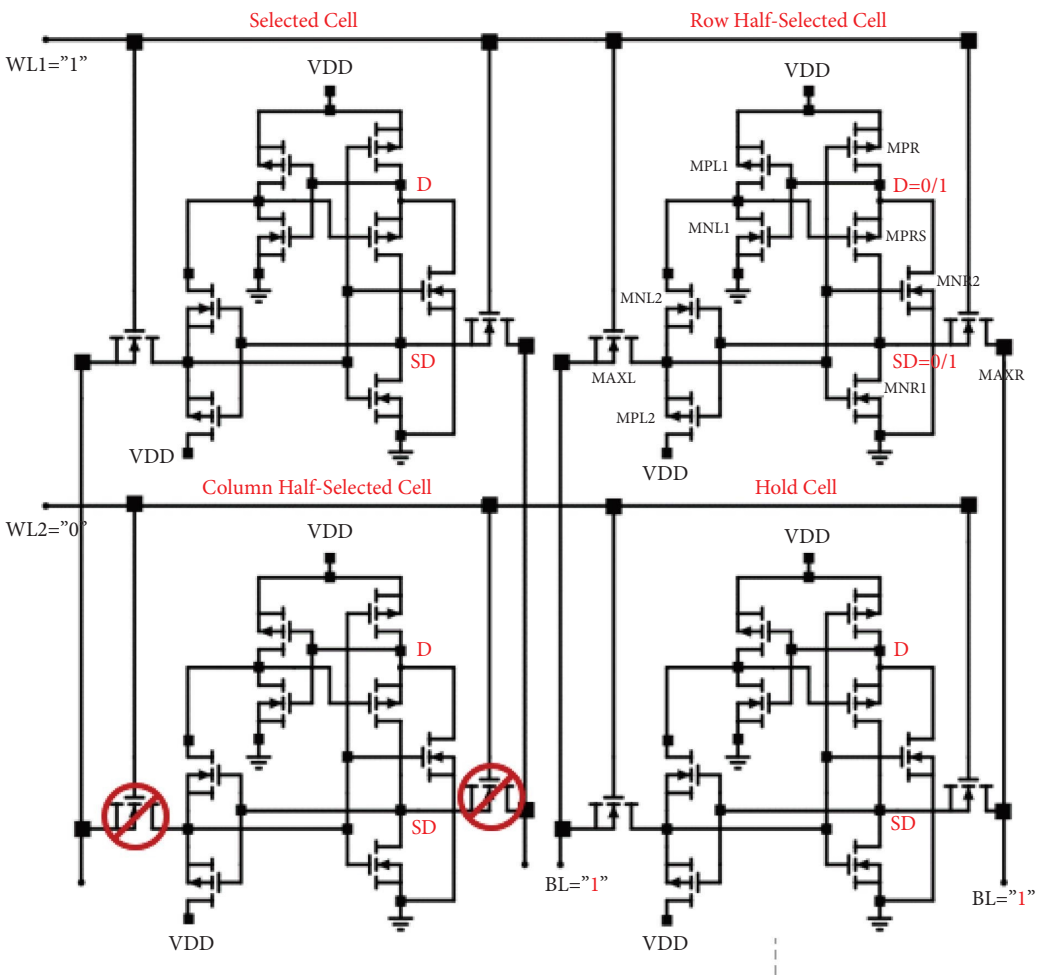

Figure 16: Half select cell structure in memory array.

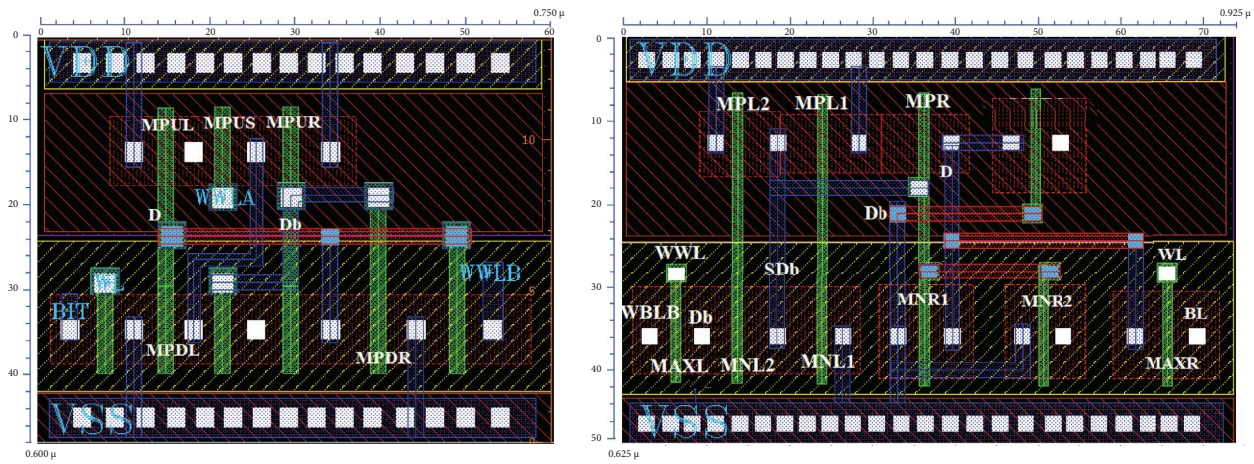

Figure 17: Layout in 22-nm industrial CMOS technology for (a) SSDF 9T SRAM cell and (b) proposed BSRWA 10T SRAM cell.

Table 3: Cell sizing using width proportion ($w1$) as Gaussian parameter for MC simulation and technology parameters.

Conv-6T	FD-10T	SSDF [11]	Prop BSRWA
**Conv-6T cell-R	*FD-10T cell-R	**SSDF-9T cell-R	**BISRWA cell-R
MPUR W = "$w1$"	MPDR W = "3 $*$ $w1$"	MPUR W = "1.5 $*$ $w1$"	MPR W = '$w1$"
MPDR W = "3 $*$ $w1$"	MPDSR W = "3 $*$ $w1$"	MPDSR W = "1.5 $*$ $w1$"	MPRS W = '$w1$"
MAXR W = "1.5 $*$ $w1$"	MFBR W = "3 $*$ $w1$"	MPDR W = "1.5 $*$ $w1$"	MNR1 W = "3 $*$ $w1$"
**Conv-6T cell-L	MPUR W = "1 $*$ $w1$"	M9,D W = "1.5 $*$ $w1$"	MNR2 W = "3 $*$ $w1$"
MPUL W = "$w1$"	MAXR W = "1.5 $*$ $w1$"	**SSDF-9T cell-L	MAXRW = "1.5 $*$ $w1$"
MPDL W = "3 $*$ $w1$"	**FD-10T cell-L	MPUSL W = "1.2 $*$ $w1$"	**BISRWA cell-L
	MPDSL W = "3 $*$ $w1$"	MPDL W = "1.5 $*$ $w1$"	MPL1 W = "$w1$"
	MFBL W = "1.5 $*$ $w1$"	MAXL W = "1.5 $*$ $w1$"	MPL2 W = "$w1$"
MAXL W = "1.5 $*$ $w1$"	MAXL W = "1.5 $*$ $w1$"	MPUL W = "1.2 $*$ $w1$"	MNL1 W = "3 $*$ $w1$"
	MPDL W = "3 $*$ $w1$"	MPDSL W = "1.5 $*$ $w1$"	MNL2 W = "3 $*$ $w1$"
	MPUL W = "1 $*$ $w1$"		MAXL W = "1.5 $*$ $w1$"

V_{THN} = 240 mv (sat), 248 mv (Lin); V_{THP} = 244 mv (sat), 253 mv (Lin). * $W1$ = MC sizing Gaussian parameter.

4. Conclusion

This proposed work concludes that the performance of the proposed SRAM cell dominates the previous SRAM cells, i.e., conventional, fully differential 10T-ST (FD 10T-ST), single stacked disturbance-free 9T-ST (SSDF 9T-ST). The proposed SRAM cell dominates SSDF 9T-ST SRAM cell in terms of write ability, even SSDF 9T-ST SRAM cell is assisted with assist circuits such as NBL [15], UDVS [20, 21], write assist combining negative BL and V_{DD} collapse. The read stability improvement of the proposed BSRWA 10T SRAM cell is 212%, 67%, and 33% from conventional SRAM cell, FD 10T SRAM cell, and SSDF 9T SRAM cells, respectively. The impact of temperature variation on the performance of memory cells is observed using Monte Carlo simulation for HSNM parameter. The deviation of HSNM for 15°C to 55°C is 14%, 5%, 4%, and 1% in conventional SRAM cell, FD 10T SRAM cell, SSDF 9T SRAM cell, and proposed BSRWA 10T SRAM cell, respectively. The impact of assist circuits on the write performance of memory cells is observed using Monte Carlo simulation for the write margin (WM) parameter. WM of SSDF 9T-ST SRAM is improved by 15% and 25% by adding UDVS assist circuit [20, 21] and write assist combining negative BL and V_{DD} collapse circuit. But BSRWA SRAM cell itself can improve WM by 32% without any assist circuit. Write delay of SSDF 9T-ST SRAM is reduced by 7.3%, 12.4%, and 18.3% by adding NBL [15], UDVS [20, 21], and write assist combining negative BL and V_{DD} collapse. But delay is minimized by 19.7% using the proposed BSRWA SRAM cell without any assist circuit. The proposed SRAM cell is designed at a 22 nm CMOS technology node and verified in the Synopsys Custom compiler. MC simulation results are monitored on Synopsys Cosmoscope wave viewer.

Data Availability

The data supporting the current study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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