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Review Article

Successive Approximation Register Analog-to-Digital Converter (SAR ADC) for Biomedical Applications

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This study presents a survey of the most promising reported SAR ADC designs for biomedical applications, stressing advantages, disadvantages, and limitations, and concludes with a quantitative comparison. Recent progress in the development of a single SAR ADC architecture is reviewed. In wearable and biosensor systems, a very small amount of total power must be devoured by portable batteries or energy-harvesting circuits in order to function correctly. During the past decade, implementation of the high energy efficiency of SAR ADC has become the most necessary. So, several different implementation schemes for the main components of the SAR ADC have been proposed. In this review study, the various circuit architectures have been explained, beginning with the sample and hold (S/H) switching circuits, the dynamic comparator, the internal digital-to-analog converter (DAC), and the SAR control logic. In order to achieve low power consumption, numerous different configurations of dynamic comparator circuits are revealed. At the end of this overview, the evolutions of DAC architecture in distinct biomedical applications today can make a tradeoff between resolution, speed, and linearity, which represent the challenges of a single SAR ADC. For high resolution, the dual split capacitive DAC (CDAC) array technique and hybrid capacitor technique can be used. Also, for ultralow power consumption, various voltage switching schemes are achieved to reduce the number of switches. These schemes can save switching energy and reduce capacitor array area with high linearity. Additionally, to increase the speed of the conversion process, a prediction-based ADC design is employed. Therefore, SAR ADC is considered the ideal solution for biomedical applications.

1. Introduction

The demand for finding solutions for diagnosing and treating diseases has increased with the rapid increase in requirements in medicine and healthcare systems. Biomedical applications such as medical implants and wireless sensors are becoming the most serious applications, helping monitor patients for long periods without imposing any restrictions on them [1–4]. The architecture of a wireless body sensor network (WBSN) [5] is shown in Figure 1. WBSN consists of several wireless sensor nodes attached inside, on, or around a human body to monitor vital body parameters and movements. Then, the WBS nodes have to send this biomedical data to a base station wirelessly. Thus, one of the most important building blocks is the analog-to-digital converter (ADC). It is required to convert the analog biomedical signals to digital format for storing and processing. Considering these nodes are portable battery-operated electronic devices, energy-efficient integrated circuit designs are required. It can be claimed that low power consumption is one of the most important bottlenecks for wireless biomedical applications because of limited battery lifetime [6]. The analog-to-digital converter (ADC) is a key building block as it can be considered the interface between the real analog domain and the digital processing domain.

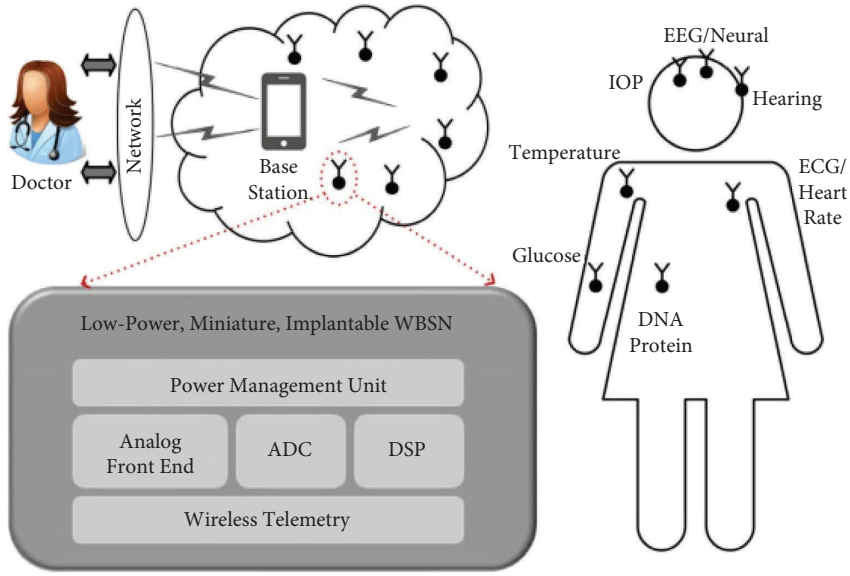

Figure 1: Wireless body sensor nodes forming [5].

ADC for wireless biomedical applications [2] must have low power consumption for a long battery lifetime. Also, the applications of biomedical impose extra requirements on ADC to have a smaller chip area, medium resolution, and sampling speed ranging from a few KS/s to a few MS/s [7, 8].

Generally, ADC has several important performance parameters, such as sampling frequency (F_S), resolution, effective number of bits (ENOB), signal-to-noise-and-distortion ratio (SNDR), power consumption, and figure of merit (FOM). Higher resolution and speed are simultaneously required, which make the ADC a critical design component.

The architecture of the ADC has a great impact on the performance of the overall system [9]. Although several works of ADC design and implementation have been achieved, there is a challenge to high speed ADC and high resolution with low power consumption for biomedical applications. An energy-efficient architecture of analog-to-digital converter (ADC) with reduced hardware complexity for biomedical applications is required [10–12]. Therefore, concerning low power considerations, a successive approximation register analog-to-digital converter (SAR ADC) is an appropriate choice for conversion from an analog signal to digital data.

The successive approximation register ADC has obtained significant attention in the latest years [13]. The objective of this study is to survey the different proposed techniques of low-power SAR ADC for biomedical applications in the past five years. Furthermore, this review helps researchers interested in the design of energy-efficient SAR ADC for a clear and rapid understanding of the essential components of SAR ADC with a demonstration of the different implementations schemes of each component.

The contributions of this survey are as follows:

(i) A comprehensive study demonstrating different single SAR ADC implementations and listing the pros, cons, and challenges of each block

(ii) Studying different optimizations that have been achieved to reduce the power consumption of SAR ADC in almost all manuscripts published in the 2017–2021 year span

(iii) Clear comparisons of different single SAR ADC techniques have been achieved on various CMOS technologies

(iv) The attained results have been analyzed based on power consumption, resolution, speed, and linearity. These results are discussed clearly in a detailed manner using tables and figures.

Therefore, the remainder of this study is organized as follows: the next Section 2 provides an overview of the architecture of SAR ADC. The different implementations of sample and hold switching are demonstrated in Section 3. In Section 4, various configurations of the dynamic comparator are presented. The CDAC architectures are discussed in Section 5. Section 6 describes the SAR register and its control logic. A summary of the recently published SAR ADC performance parameters is discussed in Section 7. Finally, conclusions are provided in Section 8.

2. SAR ADC Architecture

In this section, a brief architecture of the SAR ADC is reviewed, explaining the benefits of the SAR ADC among several ADC types. The block diagram of the basic implementation of SAR ADC is illustrated in Figure 2. The SAR ADC comprises an S/H switch, an internal DAC, a comparator, and successive approximation logic. The input signal is sampled by the S/H switch, and the internal DAC converts the digital code stored in the register to an analog value. Therefore, the comparator compares the S/H voltage and DAC output voltage, producing a digital output instructing the digital logic to update the register containing the code. Initially, the most significant bit (MSB) is displayed

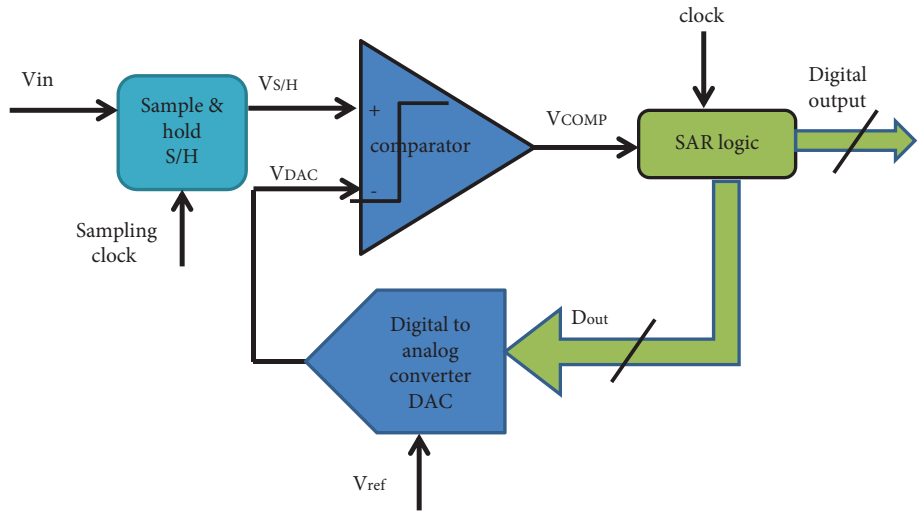

Figure 2: Block diagram of the SAR ADC.

in a digital format, and then the internal DAC sends the equivalent analog value (Vref/2) into the comparator for comparison with the sampled signal. If the resulting comparator output is one, meaning Vin is greater than $V_{ref}/2$, the MSB remains stored in the SAR register, and one is loaded to the second most significant bit. Else, if $V_{ref}/2 < V_{in}$, the comparator output will be zero, where the control circuit writes zero to the most significant bit and one to the second-most significant bit. Then a new cycle begins to verify the second-most significant bit. In every new clock cycle, the DAC decides on the next significant bit until all the required number N of bits are found. The clock and timing profile of SAR is indicated in Figure 3. Note that the two operations during the switching procedure are the sampling process and the conversion process. In the conversion process, all bits from the MSB to the least significant bit (LSB) are determined.

In general, the main advantage of SAR ADC is its inherently low power consumption compared to other types of ADC. To reduce the power consumption, there are many different methods, as will be demonstrated in this paper. Various configurations for the comparator [14–24] can be used to reduce power consumption, time delay, and noise effects. In addition, the modified binary-weighted CDAC structure [25–68] can save area and energy. Furthermore, the CDAC reference voltage switching schemes can decrease the power supply voltage and increase the speed of the conversion process [69–89]. Moreover, the different algorithm schemes can diminish the number of iterations for the conversion process [90–100]. In addition, the SAR ADC architecture is suitable for fine CMOS processes [101].

Unfortunately, there are several challenges facing the low-power SAR ADC for biomedical applications. The design of a high-resolution, low-power SAR ADC is very difficult because the area of a binary-weighted CDAC array increases exponentially with increasing resolution. In this case, high power and a large chip area will be produced. Furthermore, at low sampling frequencies, the leakage current of the sampling switch is one of the key design considerations where the nonlinearity system has resulted due to the long conversion period. Another challenge is the bit decision error due to the noise from the comparator, power supply, or the complete settling time of the CDAC. In the coming sections, we will explain in detail the components of the ADC.

3. SAR Sample and Hold Circuit

The first block in the SAR ADC is the sample and hold (S/H) circuit. The main challenges that face the sample switch are dynamic linearity, power consumption, and noise immunity. In the S/H operation, a continuous time signal is converted into a sampled or time-discrete signal with a regular sampling period. The sampling frequency follows the Nyquist theorem to avoid an aliasing effect.

A straightforward sample switch of an NMOS transistor [102] can be used that consumes a low power at a lower cost. However, it suffers from nonideal switching effects, nonlinearity, harmonic distortion, and noise.

The major bottleneck in S/H switching is the variation of conductivity between the gate and source terminals ($\mathbf{g_{gs}}$) of the sample transistor in the triode region. As the input signal changes ($\mathbf{V_{in}}$), the conductivity ($\mathbf{g_{gs}}$) varies equation (1).

$$\mathbf{g_{gs}} = \mu \mathbf{c_{ox}} \frac{\mathbf{w}}{\mathbf{l}} (\mathbf{V_{dd}} - \mathbf{V_{in}} - \mathbf{V_{Tn}}), \quad (1)$$

where μ is the surface mobility, $\mathbf{c_{ox}}$ is the capacitance per unit gate area, and $\mathbf{V_{Tn}}$ the threshold voltage of MOSFET.

Also, the charge injection and clock feed through distortion occur in the sampled signal. Where the charge injection is defined as the charge that exists between the source and drain terminals when the sample switch is turned off, and the clock feed through is defined as the charge injected due to the overlapping coupling capacitor between the gate and drain terminals. Consequently, it is preferable to implement the sample switch by using CMOS transmission gates [8, 64, 103] or the bootstrap switch in Figure 4 [2, 5, 6, 11, 17, 22, 24, 31, 34, 45, 53, 58, 63, 65–$ $67, 86, 90, 94, 104].$ $

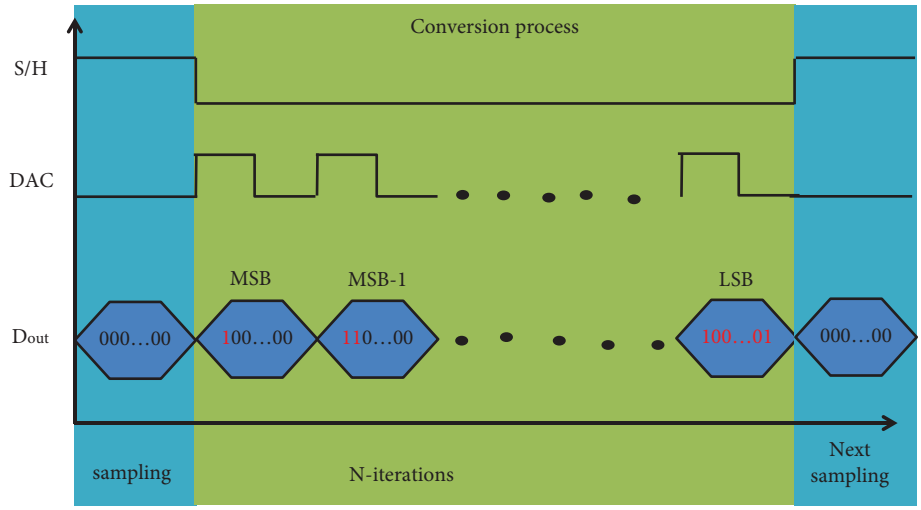

Figure 3: Clock and timing profile of the SAR ADC.

The variations in conductivity are reduced by utilizing the CMOS transmission gates, but the problem of input dependence still exists. Additionally, a large parasitic capacitor that limits the resolution of SAR appears.

A good solution to improve the linearity and decrease the power consumption is to employ the bootstrap switch. As shown in Figure 4, when "$\overline{\mathbf{clk}}$" is high, transistors M1 and M2 are turned on, and the capacitor C is charged by the supply voltage. The transistors M3, M5, and M6 are utilized to separate the capacitor C from the gate of the transistor M7. While "$\overline{\mathbf{clk}}$" is low, the transistors M3 and M4 are turned on and permit the capacitor C to discharge the stored charge through the M7 gate. This makes the conductivity constant and dependent only on the supply voltage. This switching scheme reduces nonlinearity error and voltage error, which are produced by the charge injection.

As well, a double bootstrap switch [12, 23] is employed to achieve higher linearity and enhance the common mode noise immunity. This scheme supports the fully differential architecture of the SAR comparator. In the double bootstrap switch, the gate-source voltage is raised to twice the supply voltage. Also, the bootstrap switch followed by a dummy switch is used [3, 4] for the clock feed through compensation. The charge injected during conversion is compared with the charge induced by a dummy switch.

In the SAR ADC for biomedical applications, the target design is to obtain power consumption of less than microwatts. So, the regular structure of the SAR sample and hold switch is the bootstrap circuit [63]. The different circuit schemes are summarized in Table 1. From this comparison, the tradeoff between power consumption, linearity, and noise is listed. We have noted that ultralow power consumption can be achieved by employing CMOS transmission gates [64]. However, the dynamic linearity and noise results become very bad. The required specifications can be obtained by using the bootstrap switch. To enhance the linearity and noise, the double bootstrap switch scheme [23] and the bootstrap switch followed by a dummy switch scheme [4] can be used, but the power consumption is increased. Also, to improve linearity, some researchers have used different techniques for bandwidth enhancement, such as the dual-path linearization technique [104], but at the expense of power.

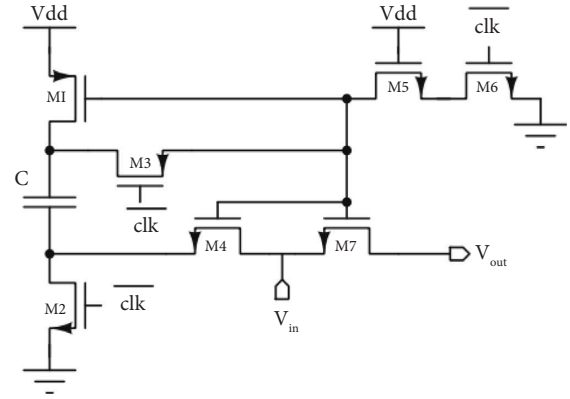

Figure 4: The conventional bootstrapped sample and hold circuit [63].

4. Different Configuration of Dynamic Comparator

Comparator is an essential building block in SAR ADC. The sampled input is compared with the voltage on the capacitor arrays of the DAC by the SAR comparator and produces the equivalent digital output that feeds to the SAR logic. In this section, the different designs of SAR comparator are presented. The methodology for implementing the SAR comparator targets the lowering of power consumption to be convenient for biomedical applications.

Likewise, several performance factors are considered besides the consumed power, such as accuracy, speed, resolution, propagation time delay, input-referred offset voltage, supply sensitivity, and meta-stability [14].

A dynamic latch comparator is the most utilized in prior works [15]. The four implementation techniques employed in the state-of-the-art SAR ADC are the simple structure of

Table 1: Comparison between different SAH structures.

Structure	CMOS transmission gates	Bootstrap switch	Double bootstrap switch	Bootstrap switch followed by a dummy switch
Dynamic linearity	Poor	Good	Very high	High
Power consumption	Very low	Low	High	Average
Common mode noise immunity	Low	Average	High	High
Charge injection and clock feed through distortion	High	Average	Low	Very low

the single-stage dynamic latch, the two-stage dynamic latch, the three-stage dynamic latch, and the multistage preamplifier dynamic latch.

4.1. Single-Stage Dynamic Latch Comparator. The single-stage dynamic latch comparators are the principle of one of the main strategies. Due to their lowest number of transistors, this scheme saves both power and area. The basic structure of the single-stage dynamic latch comparator [3, 4, 6, 16, 63, 86, 94] is presented in Figure 5. It consists of three sections, including the differential amplification section (M1 and M2), the cross-coupled inverter section (M3:M6), and the reswitched section (S1:S4).

The operation of the single-stage dynamic comparator is completed after two phases: the reset phase and the generation phase. In the reset phase, "**clk**" is low, the preceding analog input is removed, the switches are turned on, and the output is charged to the supply voltage **Vdd** through the MOSFET loading capacitor. No static power is consumed in this phase. While in the generation phase, "**clk**" is high, and the amplification output is generated through the positive feedback formed by the cross-coupled inverter section. The produced output depends on the differential input. A small difference in the input is directly converted to full-scale digital levels.

As shown in Figure 5, if $\mathbf{V_{in}^{+}}$ is greater than $\mathbf{V_{in}^{-}}$, the P node is discharged faster than the Q node, and M3 and M4 are turned off until the **Vgs** of M3 and M4 reach to $\mathbf{V_{dd}} - \mathbf{V_{thn}}$, then the M3 and M4 are turned on. Consequently, the $\mathbf{V_{out}^{+}}$ and $\mathbf{V_{out}^{-}}$ nodes are discharged. The $\mathbf{V_{out}^{+}}$ node is discharged faster than the $\mathbf{V_{out}^{-}}$ node. This is continued until the **Vgs** of M5 and M6 reach to $\mathbf{V_{dd}} - \mathbf{V_{thp}}$ and, therefore, the M5 and M6 are turned on. Accordingly, the $\mathbf{V_{out}^{+}}$ is turned into **gnd** and $\mathbf{V_{out}^{-}}$ is turned to ground ($\mathbf{V_{dd}}$) and vice versa. When $\mathbf{V_{in}^{-}}$ is greater than $\mathbf{V_{in}^{+}}$, the output $\mathbf{V_{out}^{+}}$ is turned into $\mathbf{V_{dd}}$ and $\mathbf{V_{out}^{-}}$ is turned into **gnd**.

A fully differential comparator can convert the change in input voltage signal to a full-scale signal in a short time and benefit from common mode noise rejection [6]. On the other hand, the main challenges in the design of the comparator are the comparator noise at small $\mathbf{V_{dd}}$, and the nonlinear distortion at large $\mathbf{V_{dd}}$. Therefore, adaptive supply in [16] is utilized such that the $\mathbf{V_{dd}}$ is used in sampling and in MSB conversion while $\mathbf{V_{dd}}/2$ is used in the next conversion in order to reduce power consumption.

4.2. Two-Stage Dynamic Latch. In the two-stage comparator design, a preamplifier stage with a single-stage dynamic latch is connected in a cascaded scheme as shown in Figure 6 [2, 5, 7, 11, 12, 15, 18–20, 27, 33, 35, 44, 53, 65, 90, 102].

Besides the amplification of the input signal, this comparator scheme prevents the kick-back noise, reduces the input-referred offset voltage, and improves the comparison speed [14].

Different implementations of the two-stage dynamic latch SAR comparator are utilized to enhance the performance of SAR ADC [15]. Employing the inverter-based amplifier in [17] improves the regulation of common mode. In order to reduce the delay, a forward body bias with lower threshold voltages is used [18]. Also, the noise sensitivity, the root mean square (RMS) input-referred noise, and the offset voltage have been improved.

The folded cascade preamplifier comparator is utilized in [19] to reduce the delay and power consumption and to enhance the standard deviation of the offset voltage. Furthermore, optimizing the transistor sizing [20] improves the input-referred offset and kick-back noise. As well, the complement differential pair of the dynamic latch is employed to decrease the input-referred offset voltage [7].

4.3. Three-Stage Dynamic Latch Comparator. The preamplifier stage, single-stage dynamic latch, and buffer stage are integrated in the SAR comparator [1, 31, 103] to decrease the delay, power consumption, kick-back noise, and the input-referred offset voltage. Also, two inverter stages may be used with the single-stage dynamic latch [29, 52, 58] to avoid the static current at the reset phase and to enhance the driving capability and achieve rail-to-rail digital output. Based on the dual sampling technique as mentioned in Section 5, a four-input dynamic comparator is utilized in [58].

4.4. Multistage Preamplifier Dynamic Latch Comparator. In this comparator scheme, multistages of the preamplifier stage and single-stage dynamic latch are employed taking the advantages of both. In addition, rejection of the common mode voltage and external noise is achieved [21].

Clearly, the sensitivity, offset voltage and speed are traded-off in [22]. By using one preamplifier stage and a bistable multivibrator of latch stage, the process and temperature (PT) variation is taken into consideration. Less than 0.58 LSB is achieved in the PT variation [22].

Different from the above-mentioned, a time-domain comparator [23, 24] is utilized to decrease the power consumption, improve the SNDR, and accelerate the conversion process. In this comparator, the input voltage is converted to pulses with different durations, and then a logic circuit such as a D-flip flop is utilized.

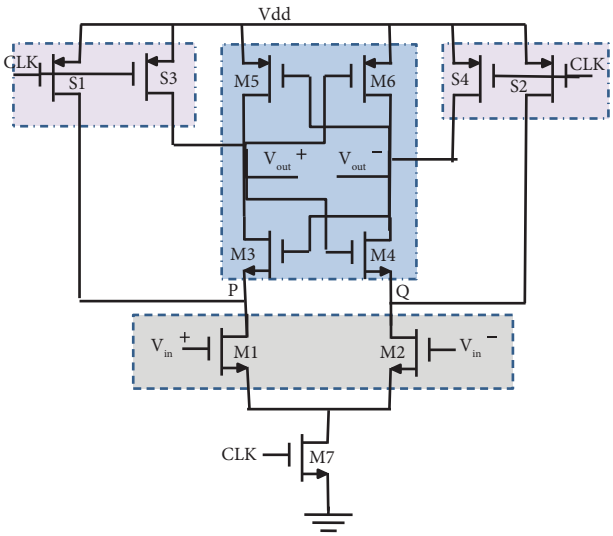

Figure 5: The basic structure of the single-stage dynamic latch comparator.

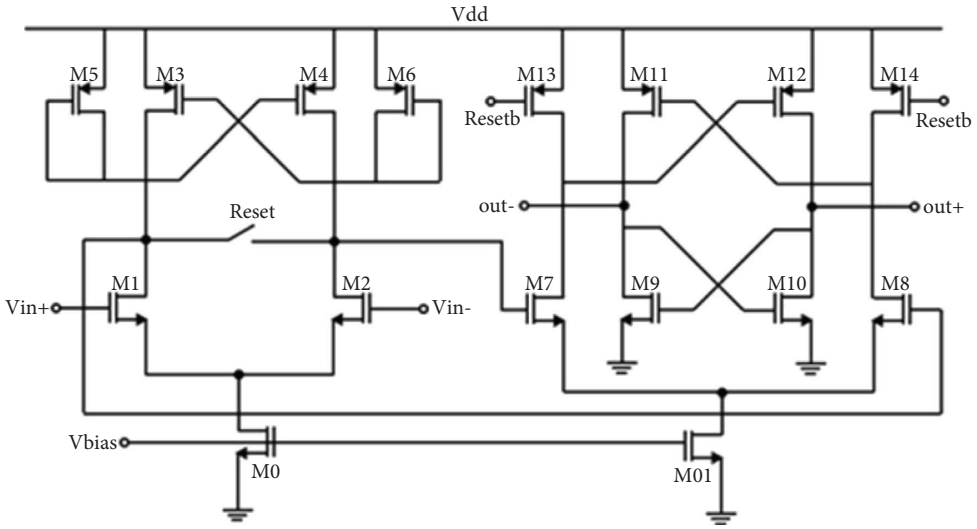

Figure 6: The two-stage preamplifier and dynamic latch [27].

All the previous comparator circuit schemes are listed in Table 2. A comparison has been accomplished between the different architectures of dynamic latch comparators in terms of power consumption, speed, kick-back noise, input-referred offset voltage, and resolution. Since the priority is the power consumption, the single-stage dynamic latch comparator has the lowest power consumption relative to the other configurations due to the lowest number of transistors employed in the circuit. However, it suffers from some disadvantages. The single-stage dynamic latch comparators run at a relatively low speed with large offset voltage and LSB. This mainly affects the resolution of ADC. However, the sampling rate and the resolution needed for biomedical applications lie in the low-to-medium range, which makes it possible to employ single-stage dynamic latch comparators. Also, one popular strategy is to utilize an amplifier stage with the dynamic comparator to obtain better offset performance. For example, the two-stage dynamic latch comparator, the tail transistor latch comparator, and the PMOS latch comparator have been utilized to improve the offset voltage while sacrificing power.

This comparison in Table 2 will help designers select the comparator circuit configuration that meets their power budget and throughput requirements. For biomedical applications, the main targets are lowering the consumed power with a low sample rate and moderate accuracy. Thus, the single-stage dynamic latch comparator, with some modifications [16], can be a good choice. Also, the two-stage dynamic latch comparator may be the familiar solution that trades off between power, speed, and noise [27]. Some researchers have used the tail transistor [2, 4, 7] or the PMOS latch comparator [2, 4, 12, 102] to decrease the power consumption.

Table 2: Comparison between different configurations of the comparators.

Configurations	Single-stage dynamic latch comparator	Two-stage dynamic latch comparator	Three-stage dynamic latch comparator	Multistage dynamic latch comparator
No. of transistor	Least	Moderate	High	Highest
Area	Small	Moderate	Large	Largest
Power consumption	Very low	Moderate	High	Highest
Speed	Very low	Low	High	Moderate
Kick-back noise	High	Low	Moderate	Very low
Offset voltage	Highest	Moderate	Low	Very low

5. SAR CDAC Architecture

The widespread adoption of DAC in distinct biomedical applications today has elevated the need for power consumption reduction [31]. The purpose of the DAC is straightforward. A reference voltage is utilized along with an array of capacitors to convert the applied digital bits to analog output voltage using switches controlled by the digital input bits as indicated in Figure 2. The resultant voltage varies with the reference voltage according to the input bits weight. Thus, the construction of the capacitor array and the reference voltage allocation affect significantly the performance of the DAC. Actually, a resistor-based DAC is utilized in prior work [103]. The R-2R ladder DAC is illustrated in Figure 7. This implementation of DAC is distinguished by simplicity and higher speed conversion. However, the great power consumption, large area, less stability, nonlinearity and matching requirements are the negative sides. Some works have adopted this DAC technique [25–89]. Replacing the resistance string by a capacitor array has led to large power and area saving. The CDAC exhibits lower energy dissipation, a higher linearity, and reasonably less processing time. Unfortunately, leakage affects the accuracy of the CDAC. Since the conversion time is less than a few us, the leakage effect may be ignored [101].

As shown in Figure 3, the transformation from digital input to analog output can be attained by applying sampling and conversion phases. The applied input voltage is stored on the CDAC array in the sampling phase, and then the switches are varied until reaching the equivalent digital code in the conversion phase. One of the major power-consuming sources in SAR ADC is the DAC's switching. In the next subsection, different techniques for CDAC are presented.

5.1. Capacitive DAC Array (CDAC). Evidently, the distribution of the capacitor array makes a great impact on the consumption of energy. In this section, different capacitor array techniques for CDAC are introduced in detail. Various capacitor techniques are proposed to further enhance the power efficiency of the CDAC arrays [25–68]. Prior works have achieved power reduction and area diminished by managing the CDAC arrays.

The standard structure of the capacitor array is composed of binary-weighted capacitors in addition to a dummy capacitor for full scale. To implement N-bit DAC, N capacitors are utilized. Unfortunately, a great-sized capacitor is required for a high resolution DAC as shown in Figure 8. For the conventional voltage switching scheme, the MSB capacitor is first connected to the reference voltage (**Vref**), and the remaining capacitors are connected to **gnd**. The voltage on the MSB capacitor represents half the **Vref**. If the input voltage is less than **Vref**/2, the MSB capacitor is reconnected to **gnd** and the next capacitor is attached to the **Vref**. Else, the MSB capacitor is kept connected to **Vref** and the following capacitor switched to **Vref**. The conventional structure and voltage switching scheme is achieved in [1, 25]. Various capacitive based DAC techniques are proposed to further enhance the power efficiency of the DAC capacitor arrays (CDAC) [25–68].

Almost all implementation techniques tend to downsize the CDAC through different structure techniques in order to reduce the energy and area of the CDAC [25–68]. Four main techniques have been proposed to distribute the CDAC array including, the CDAC array structure technique, one capacitor splitting technique, hybrid redistribution technique, and special capacitor array arrangement technique. In addition, utilizing more than one reference voltage contributes to power saving.

In the CDAC array structure technique, all capacitors in the conventional CDAC array are modified. As illustrated in Figure 9, the fully differential CDAC architecture can prevent static power consumption and enhance the dynamic range while still providing good common mode noise rejection [12, 87]. In this technique, two symmetric CDAC arrays on the upper and lower sides with differential input comparator have been utilized to diminish the MSB capacitor. The reduced capacitor has a size of 2^{n-2} as a replacement of 2^{n-1} capacitor size. However, a varying common level problem will appear.

In the two-stage subarray capacitor technique [2–6, 19, 27–30, 90, 95] the CDAC is split into two subarrays, the MSB (m-bit) and the LSB (L-bit) as shown in Figure 10. This technique achieves higher energy saving and less area as compared with the conventional technique. In addition, the linearity is enhanced and the parasitic capacitor effect is eliminated [27–30].

Meanwhile, to decrease the die size, cost, and the threshold voltage, the MIM (metal-isolated-metal) capacitor DAC array is replaced by a MOS capacitor [29]. Also, a modified two-stage dual split CDAC array technique is used to avoid the mismatch offset and reduce the capacitor array size [31–34]. This structure may be divided into three stages: subarray capacitor, the MSB, MLSB and LSB as shown in Figure 11. High resolution and optimization of CDAC area

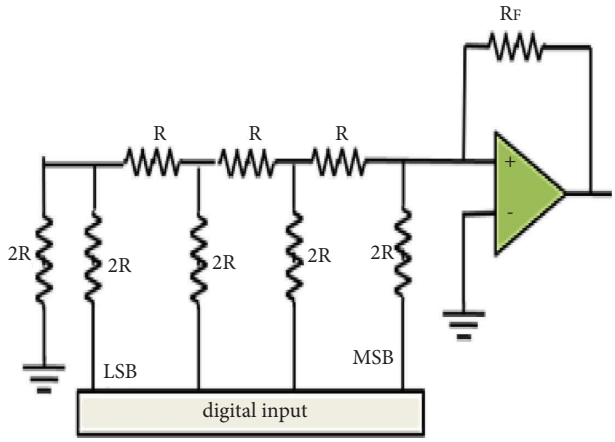

Figure 7: The R-2R DAC structure.

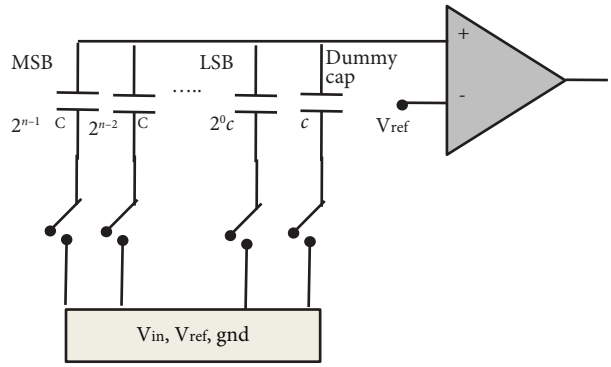

Figure 8: The conventional capacitive DAC.

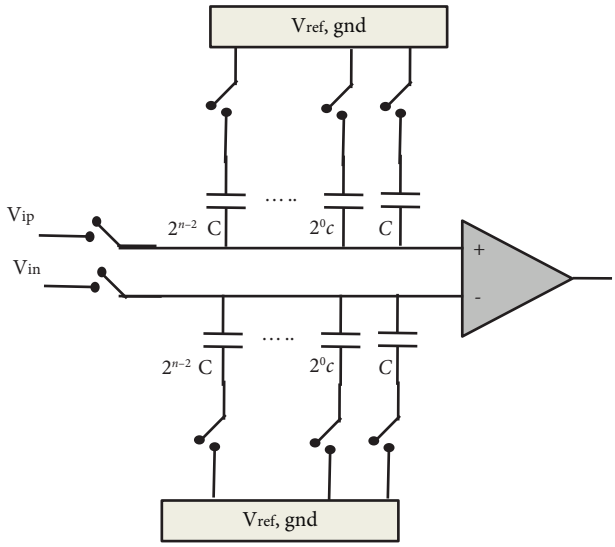

Figure 9: Fully differential structure of CDAC.

are achieved but with higher mismatch than the two-stage subarray capacitor technique. Consequently, the linearity of the two-stage subarray capacitor technique is better than the three-stage subarray capacitor technique.

Unlike in the merge-split technique as indicated in Figure 12, all capacitors on each side have been split into two similar capacitors except the dummy and unit capacitors [35–37].

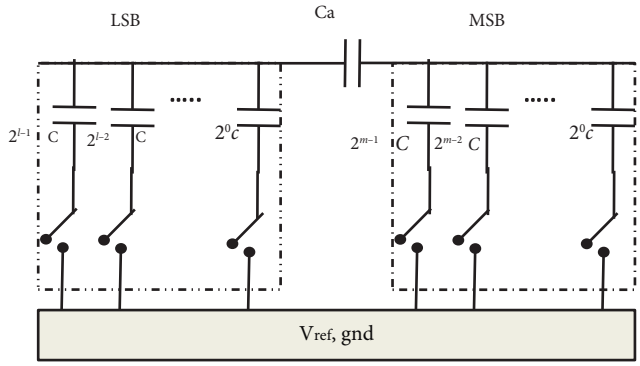

Figure 10: The two-stage subarray capacitor technique.

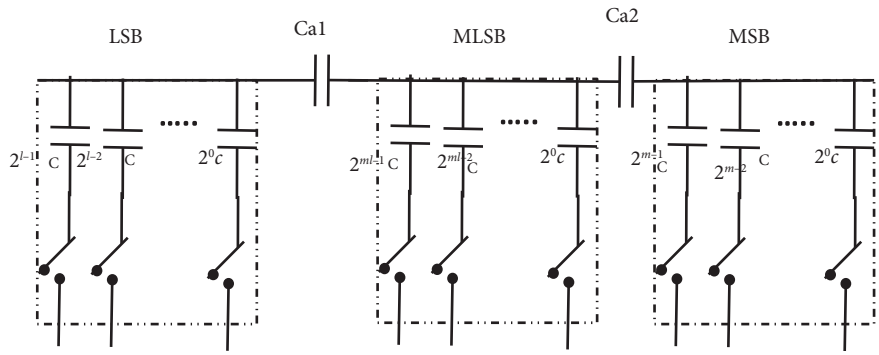

Figure 11: The dual split three-stage subarray CDAC.

Instead of handling the CDAC array, distribution of one capacitor splitting technique may be sufficient. The MSB splitting technique, the MSB capacitor is divided into binary-weighted capacitors as shown in Figure 13, is the most popular technique [11, 12, 22, 25, 38–46]. The power is saved by up to 37% as reported in [25]. The reswitching technique [45] can reuse the previously switched capacitors between nearby codes with as little hardware as to improve linearity. Unlike, the LSB capacitor technique is split into two serial capacitors [47, 48], as illustrated in Figure 14. This technique leads to a reduction in the overall capacitance by one over eight. Similarly, the split of the dummy capacitor into two capacitors C-2C has been employed in [28, 49–51], as shown in Figure 15. This technique reduces the average energy by up to 99.6% and the area of the capacitor by up to 87.21% [51].

The hybrid capacitor techniques [28, 30, 49–51] combine different techniques. Such as the binary-weighted and unary capacitor, that has been achieved in [30]. As demonstrated in Figure 16, the CDAC is split into two subarrays, the main array and the auxiliary array. The binary-weighted technique is used for the main array while the auxiliary array is based on a unary capacitor array. The dummy capacitor charge-sharing technique is named in this paper. It determines the least four bits between the dummy capacitor and the unary capacitor in the auxiliary array. The charge-sharing voltage switching scheme will be explained in the next subsection. The energy and area of the CDAC are saved by at least 99.5% and 93.5%, respectively, as compared with the conventional structure.

Utilizing the C-2C dummy capacitor technique, a two-stage subarray capacitor technique and the charge-sharing voltage switching scheme [28] has led to boosting the linearity and capacitors matching. As well, work [49] has employed the C-2C dummy capacitor technique, and the charge-sharing scheme to enhance the linearity. Another work [50, 51] has utilized the C-2C dummy capacitor technique with floating capacitor scheme. Moreover, work [50] has exploited beside the split MSB and MSB-1 capacitors into equivalent binary-weighted capacitors. In the floating capacitor scheme, MSB is connected only during the MSB bit generation. This technique has achieved a good performance of linearity with a reduction in power consumption and increase the matching of capacitors. The floating capacitor scheme reduces the average energy by up to 99.6% with less capacitor area by up to 87.21% [51].

In order to achieve higher conversion speed and resolution with less switching energy, the hybrid RC technique [10, 52, 53] is employed. In [52], the binary-weighted CDAC is utilized in the MSB array while the R-2R technique is utilized in the LSB array. Likewise, the binary-weighted capacitor technique and the string resistor technique have been integrated in [10]. A different work [53] has added a first-order and a second-order cascaded low-pass filter (LPF) before CDAC to enhance the dynamic range.

To achieve the tradeoff between linearity, area, and power, a segmented CDAC array [24] is utilized. In this technique, the capacitor array is split into three different techniques. The MSB capacitor is arranged as the

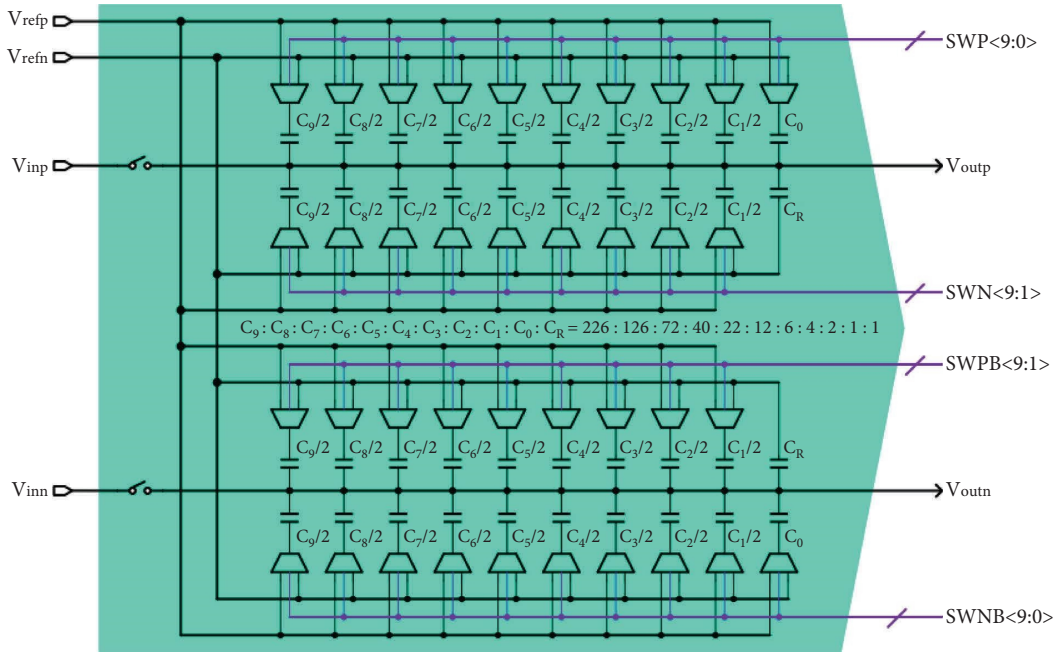

Figure 12: The merge-split CDAC technique [35].

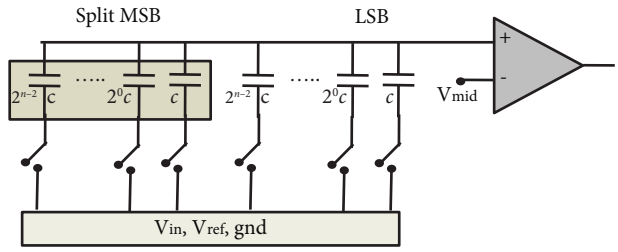

Figure 13: MSB split CDAC.

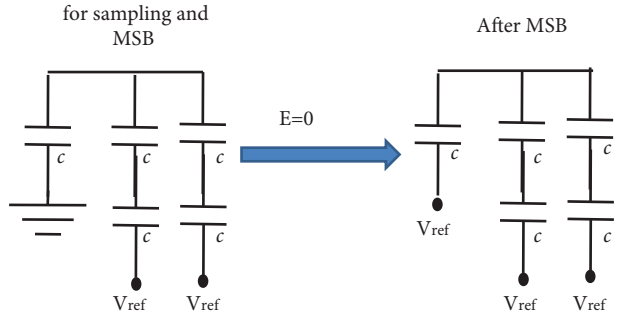

Figure 14: LSB split CDAC.

conventional binary-weighted technique, while the next 9 bits are divided into two-stage subarray capacitors that replace the big-weight capacitors with 7 equal capacitors.

Several works have adopted special arrangements for capacitor array technique [54–61]. The asymmetric capacitors technique [54] is shown in Figure 17, where MSB on the higher side of the capacitor array is removed. A different implementation technique in [55, 56] is achieved by utilizing a capacitance multiplexing technique as presented in Figures 18 and 19, respectively. The DAC capacitor array is divided into two subarrays, MSB and LSB. To decrease the consumed energy, two reference voltages are used during the comparison phase.

In [57], the reduction of energy and area has been accomplished by employing goblet architecture for the capacitor array without the need for extra reference voltage. All capacitors can be pulled up and down levels as shown in Figure 20.

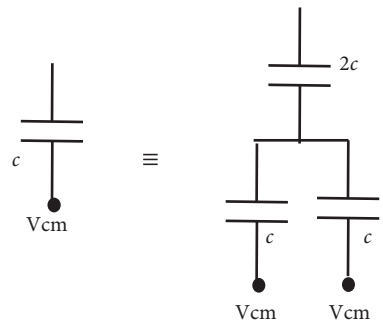

Figure 15: The C-2C dummy capacitor.

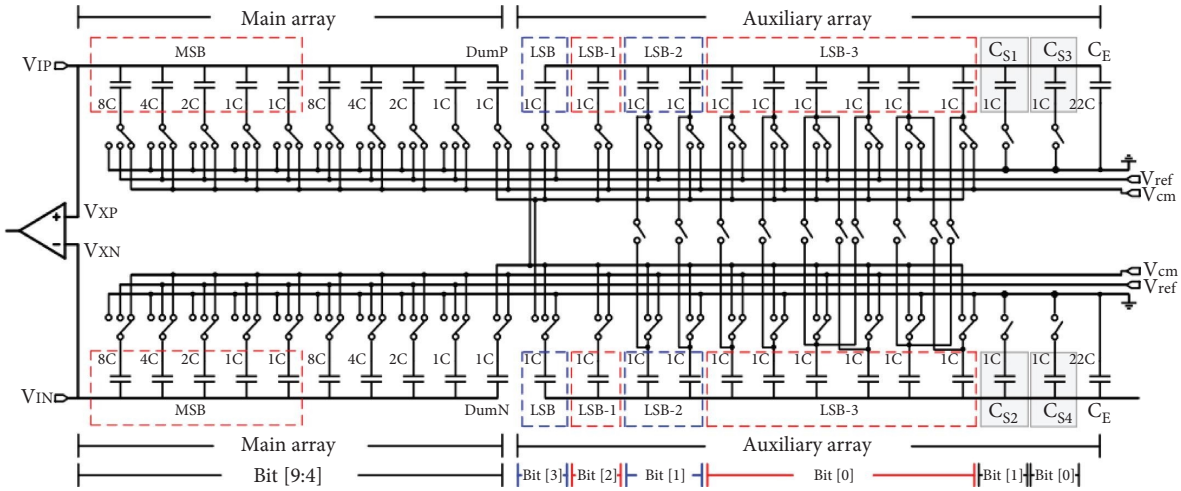

Figure 16: The charge-sharing switching technique [30].

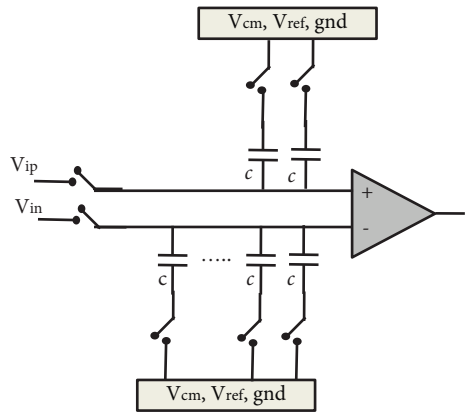

Figure 17: The asymmetric CDAC.

A dual sampling technique with four-input dynamic comparator is used in [58]. In this technique, one more bit has been added as indicated in Figure 21. The work [59] employs the subrange single-side technique to resolve the first few bits. This helps the proposed single-side technique to detect and skip switching in the main stage. The junction splitting technique is utilized in [60, 61]. The capacitor's array is split into sections of subcapacitors, which are connected in series by switches as illustrated in Figure 22. In this technique, the number of capacitors has been increased significantly in each stage during the conversion.

Several works have employed different and unusual implementation techniques for SAR DAC. In order to get rid of the parasitic capacitance effect, work [62–64] employs the charge-sharing scheme and a switched capacitor (SC) integrator, as shown in Figure 23. The execution of the operation takes place

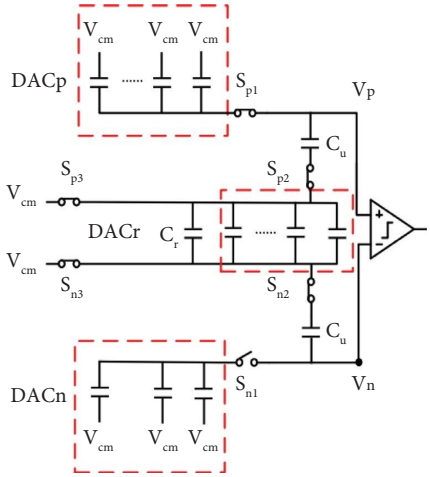

Figure 18: The capacitance multiplexing technique [56].

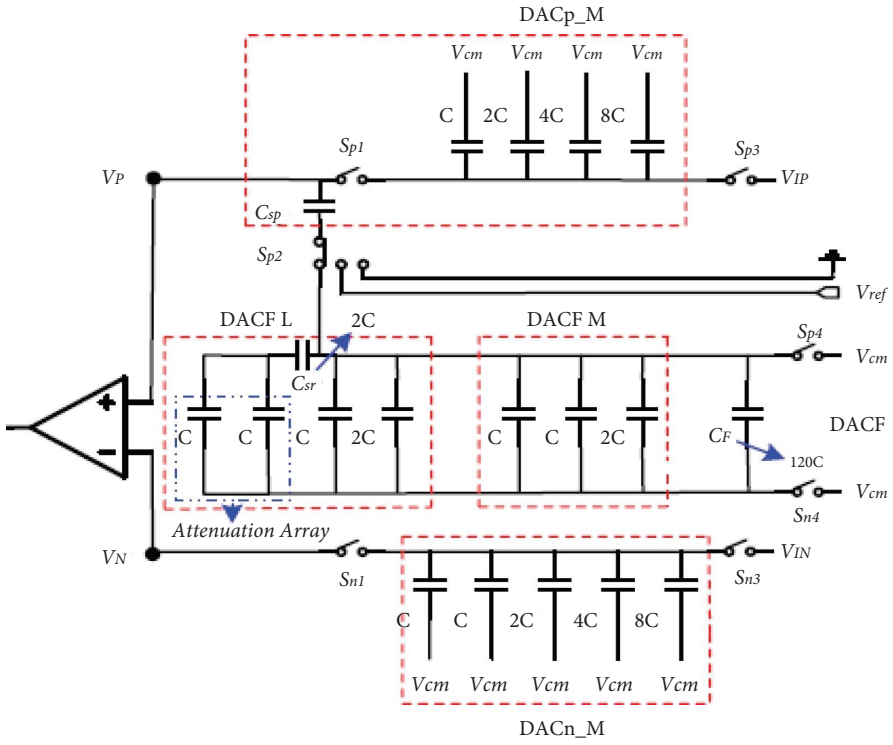

Figure 19: The asymmetric switching with the segment CDAC [55].

in the first three phases. In the sampling phase, the input is stored in the variable capacitor then the charge is transferred into the integrator during the next two phases. Also, a thermometer decoder is used in [2, 65] to reduce the static errors and glitches from MSB switching. One more is based on pseudo-two-stage SAR [66]. In the first stage, the MSB of a CDAC array is split into two capacitors with the same value except for the unit capacitor. Then, in the second stage, an active charge-transferring technique is used for the LSB, as shown in Figure 24. This technique reduces the capacitive loading and cost with less design effort.

Unlike, the difference current between the input sampling and the first four MSB of the previous samples [67] is quantized in order to reduce energy as illustrated in Figure 25. A promising technique in [68] utilizes the memristor in the SAR DAC. Memristor is a dynamic memory resistor where the resistor is changed with the applied voltage. If the power is off, a constant resistor is attained. Memristor DAC [68] is based on two memristors connected in opposite directions as shown in Figure 26.

5.2. CDAC Voltage Switching Schemes. To enhance the energy efficiency and diminish the chip area, various voltage switching schemes are used. Three main voltage switching schemes have been proposed based on using reference voltage. These schemes include the two-level, three-level and four-level voltage switching schemes.

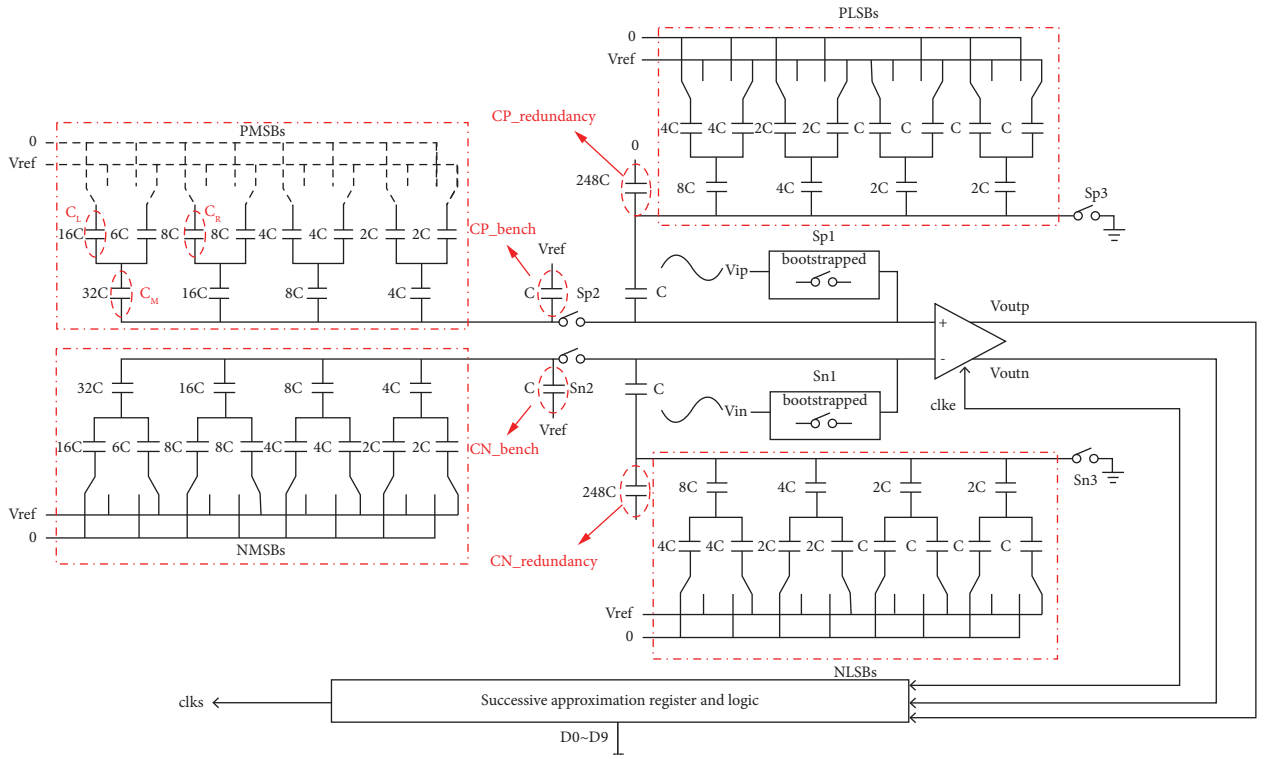

Figure 20: Extra reference voltage by using goblet architecture [57].

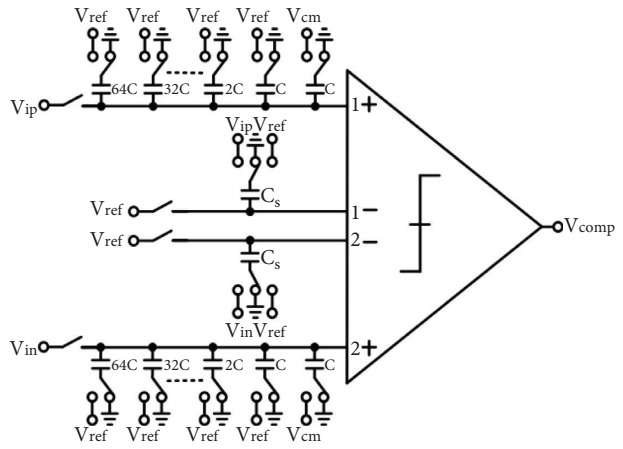

Figure 21: The dual sampling technique [57].

Two-level voltage switching schemes have been used in [41, 44, 57, 69–73] to improve the power consumption and enhance the stability and accuracy of CDAC. Higher precision and linearity can be obtained with lower average switching energy by employing two-level voltages.

As indicated in Figure 27, the monotonic voltage switching scheme is different from the conventional scheme [26]. In the sampling phase, the upper plate is charged to the input voltage, and the lower plate is connected to Vref.

After that, the comparator directly determines the MSB generation without changing any switch. So no energy is consumed in the first comparison. The MSB capacitor is switched to **Vref** or **gnd** according to the result of the comparator. Then, this process is repeated until LSB generation. Another voltage switching scheme, the charge redistribution scheme [69], is shown in Figure 28. A common mode voltage **Vcm** (0.5 **Vref**) is employed in the first two conversion cycles. This scheme consumes no energy. Excellent energy saving can be obtained by using a unary weighted capacitor with no need for a third reference voltage [70].

In this work, a different charge arrangement of the capacitor array is attained, as demonstrated in Figure 29. During this transition, there will be no energy loss from **Vcm**.

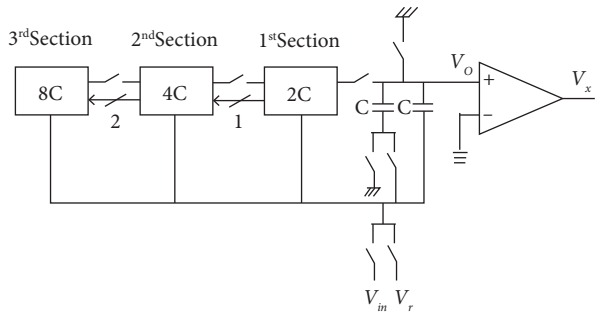

Figure 22: Hybrid and junction splitting [59].

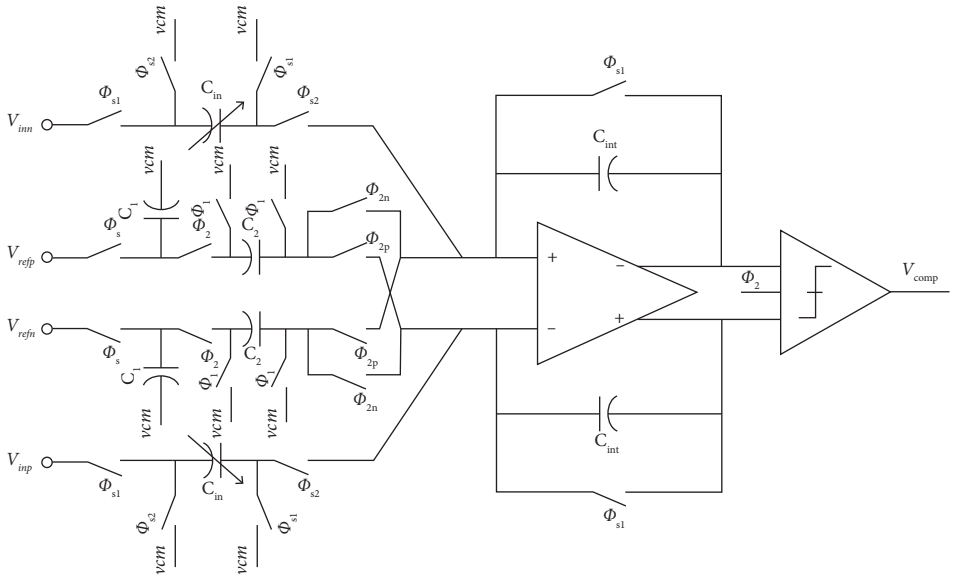

Figure 23: The schematic of the SC integrator [62].

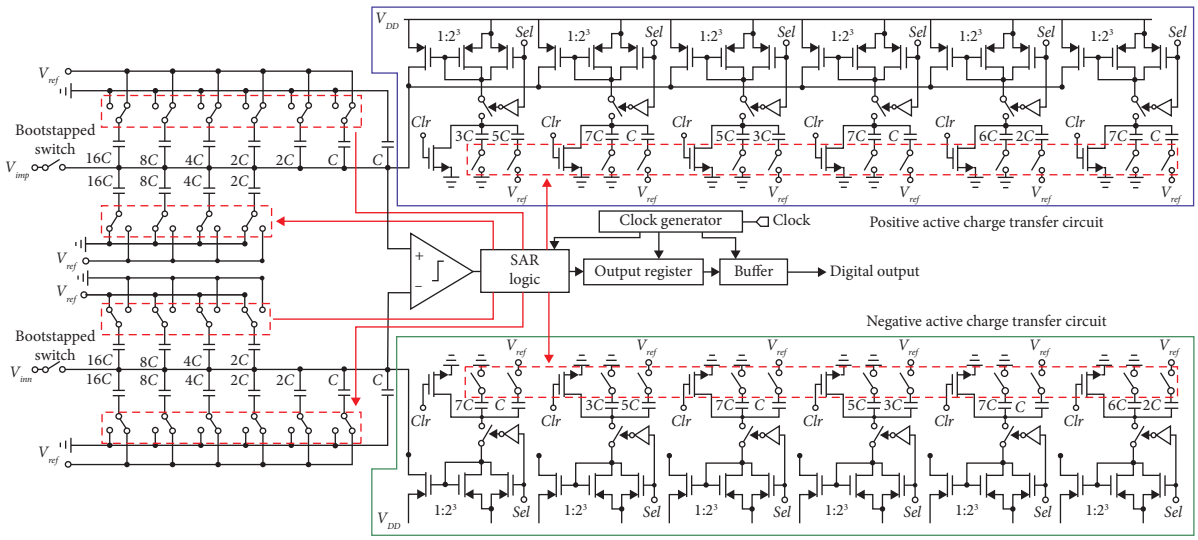

Figure 24: The pseudo-two-stage SAR with active charge-transferring technique [66].

Moreover, the threshold voltage is considered the average of the two prior threshold voltages in each conversion. The negative side of this scheme is the effect of capacitor mismatch on the linearity and also, the number of clock cycles will increase with the number of bits. The DC-DC converter is utilized in [72, 73]. The two steps down DC-DC

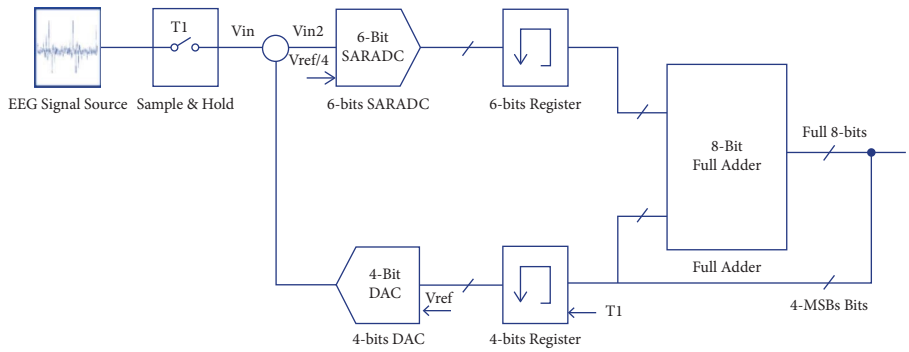

Figure 25: The block diagram of SAR ADC in [67].

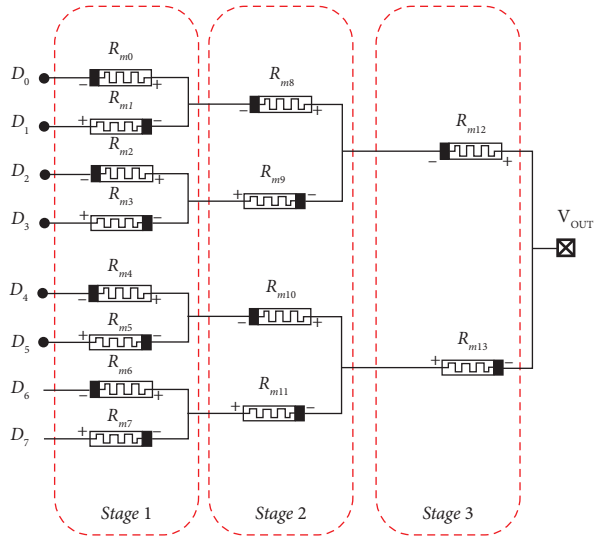

Figure 26: The DAC of two memristor connected in opposite direction [68].

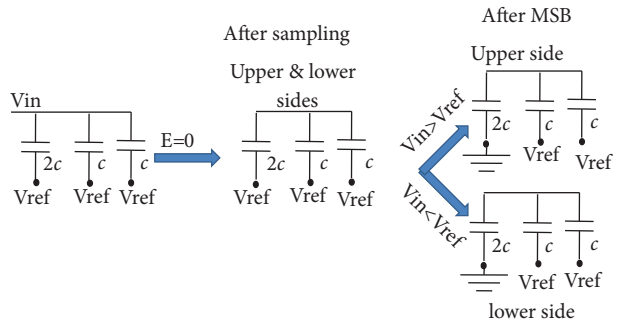

Figure 27: The monotonic voltage switching scheme.

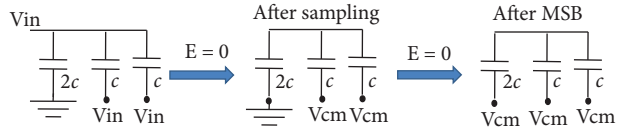

Figure 28: The charge redistribution scheme.

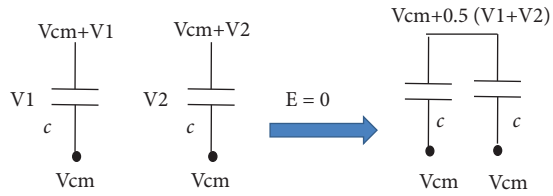

Figure 29: Zero energy drained from *Vcm*.

converter is used during the phase comparison, as shown in Figure 30. Regardless of the precision of **Vcm**, the linearity has been enhanced by using intermediate step in this scheme.

Additionally, to avoid using **Vcm**, the replacement dummy capacitor, an array of the capacitors is proposed in [44]. Several works [16, 26, 38, 43, 46, 51, 74–87] utilized the three level voltages (**gnd**, **Vref**, **Vcm**) to reduce the area of CDAC and relax the capacitor matching requirement without adding other switches. One bit has been added to these schemes. Another scheme, the charge-sharing voltage switching scheme [30], is shown in Figure 31. The principle of charge sharing: the top plate of the upper and lower sides are connected to **Vcm** and **Vref**, respectively. The bottom plate is switched to $\mathbf{V_{in}}$. To determine MSB, the upper and lower voltage sides of the MSB capacitor are changed to the same voltage 3/4 **Vref**. The charge-sharing voltage switching scheme reduces the overall power consumption compared to the monotonic voltage switching scheme. The trilevel scheme [74] and **VCM**-based scheme [75] have achieved zero energy consumption in the first two conversion cycles, as illustrated in Figure 32. A distinct scheme [12, 34–36, 38, 43, 45, 76–79, 84] has been proposed to reduce the switching steps, as shown in Figure 33. In this scheme, a hybrid-switch capacitor array, a trilevel, and $\mathbf{V_{CM}}$-based are utilized. There is no energy consumption in the first three comparison cycles because of the charge storing balance on the capacitors that diminishes any extra charge from the reference voltage. After the sampling phase, the first comparison can be executed directly with no switching energy consumption. In [46], instead of feeding the **Vcm** to all the DAC input bits, only LSB depends on the **Vcm**. Thus, this design has become insensitive to the variations of **Vcm** except for the LSB, where only one capacitor is switched. A different hybrid voltage switching scheme in [80] employs the second bit decision scheme with the negative energy reduction as shown in Figure 34, where the negative energy is considered the energy back to the voltage sources that does not consume any added energy. For the sake of energy saving, the reference voltage is scaled down to a quarter in [81]. This makes only the LSB depends on the variation of **Vcm**. In [41], scaling down the reference voltage (**Vref**/4) is utilized with the monotonic scheme and the MSB split to reduce the dynamic power. In [82], a higher side reset and set (HSRS) is used in the first two decisions with no energy loss. All capacitors are connected to **Vcm**. The determination of the MSB is achieved without any change in the switches, then all the upper side is reset to **gnd** for the MSB-1 determination. After that, the upper side is set to **Vcm** in the next decision.

In [85], the HSRS technique has also been utilized with a two-stage coarse-fine array architecture. The coarse array is based on the binary weight, while the fine array is based on the unary weight. Similarly, the spread second capacitor scheme is presented in [83], where all capacitors are connected to **Vcm** except the MSB after the second decision. Besides that, the capacitor array size is shrunk by using a two-step scaled reference level [87]. In the first stage, the MSB is determined by the reference voltage.

Vref (top, bottom). While in the second stage, the LSB is determined by using the same array capacitors and reference voltage **Vref** (top, bottom) + (**Vreftop** − **Vrefbottom**)/128.

A four-level voltage (**gnd**, **Vref**, **Vcm**, **Vaq**) have been utilized in [39, 88, 89], where the **Vaq** is the quarter of reference voltage **Vref**. This adds two bits more than the conventional scheme. In addition, the MSB splitting capacitor technique is employed with the four-level voltage scheme. Likewise, the last two capacitors are reused to determine LSB and LSB + 1 bits generation. Special works [28, 42, 46–50, 54, 56, 57, 78, 79, 89] have taken into consideration the effect of the parasitic capacitor array in order to shrink power consumption.

An important parameter that affects power consumption is the reset energy. It is the energy needed to reload all capacitors into the initial state sequence. It can be noted that the reset energy may sometimes be higher than the consumption energy in the conversion stage. While the reset energy is an important parameter in the next sampling period, in works [25, 39, 58, 60, 61, 71–73, 79–83, 88, 89], it has been ignored.

For minimizing the reset energy, two different methods have been exploited. The first one is the single-side switching method. In this switching method, the switching variation on one side is utilized after the first three compensations have been utilized [43, 54, 55, 59].

While the two-step reset method employs an intermediate stage between the final and the initial states to achieve zero reset energy consumption, this technique has been used in [28, 41, 42, 49, 50, 56].

6. SAR Register and Its Control Logic

The last block of SAR ADC is the SAR register and its control logic, which are placed after the comparator output to locate the SAR digital output.

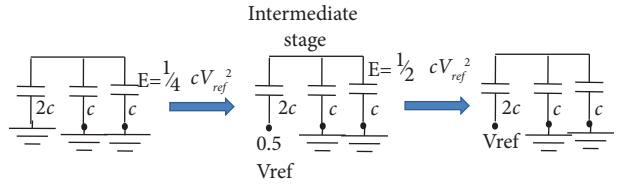

Figure 30: The two-step switching method.

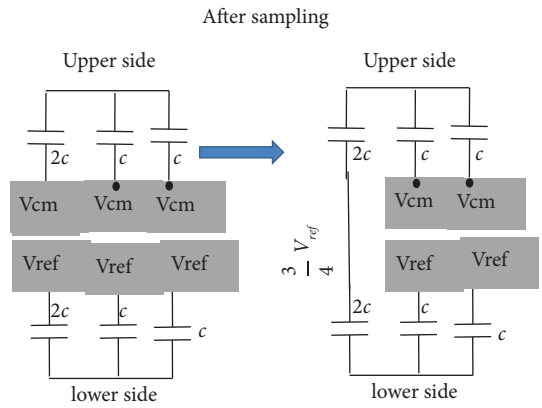

Figure 31: The charge-sharing voltage switching scheme.

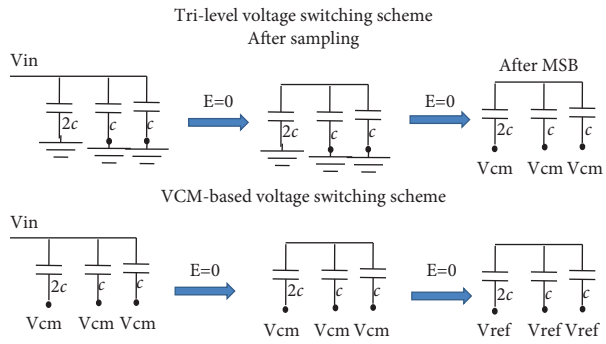

Figure 32: The trilevel and V_{CM}-based capacitor switch.

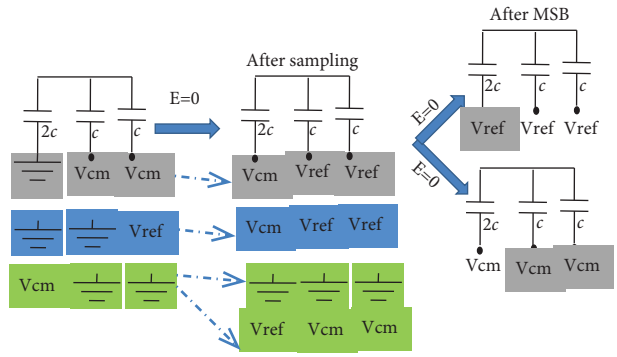

Figure 33: The hybrid switching scheme.

After the sampling phase, the sampled input is compared with the reference voltage, which is stored in CDAC. Then, the MSB is determined whether it is zero or one according to the comparator output in the conversion phase. Thereafter, the SAR logic is modulated and triggered in the next clock cycle to determine the following bit until the LSB and the corresponding output code are stored in the SAR register group.

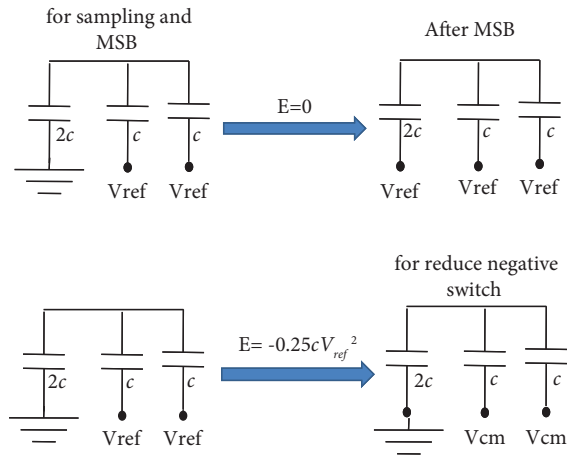

Figure 34: Two energy saving methods.

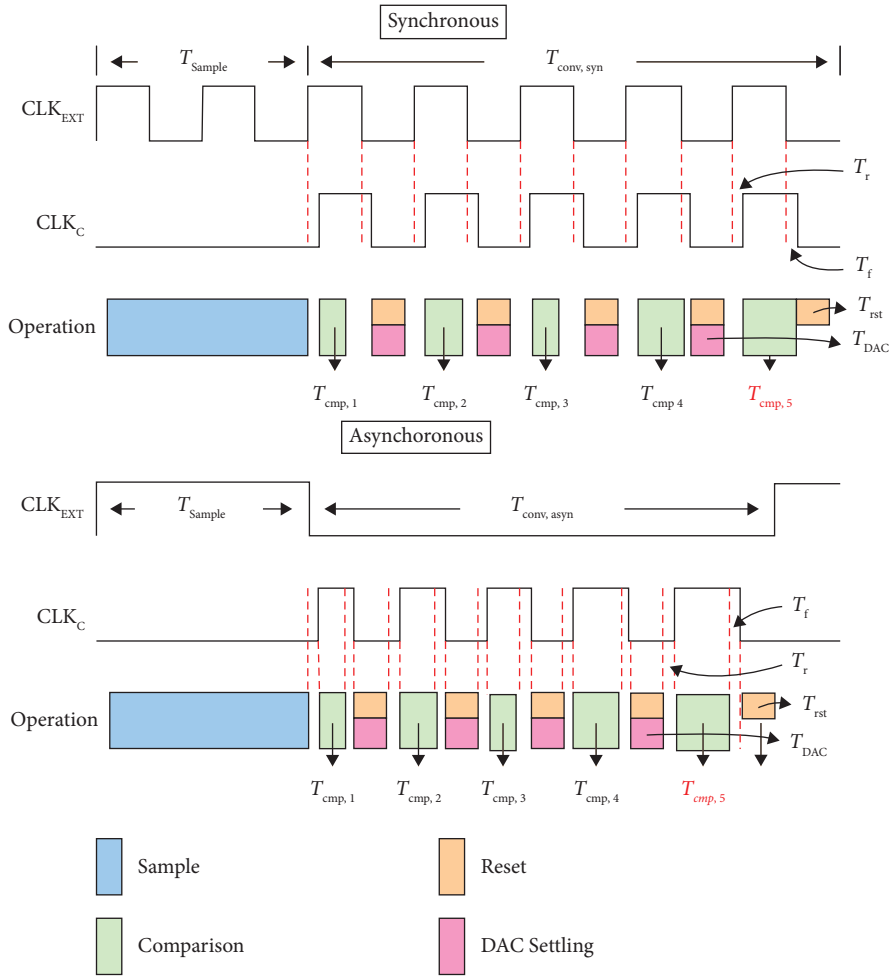

Figure 35: Timing diagram of (a) synchronous and (b) asynchronous control logic [91].

SAR logic control can be achieved using a synchronous or asynchronous scheme. In the conventional synchronous SAR logic [1–6, 8, 10, 12, 29, 31, 33, 34, 36, 40, 45, 52, 63, 65, 66, 68, 87, 90, 102, 103] an external regular clock is feed during the sampling and conversion phases as explained in Figure 35. Thus, the conversion clock is faster $(N+1)$ times that of the sampling

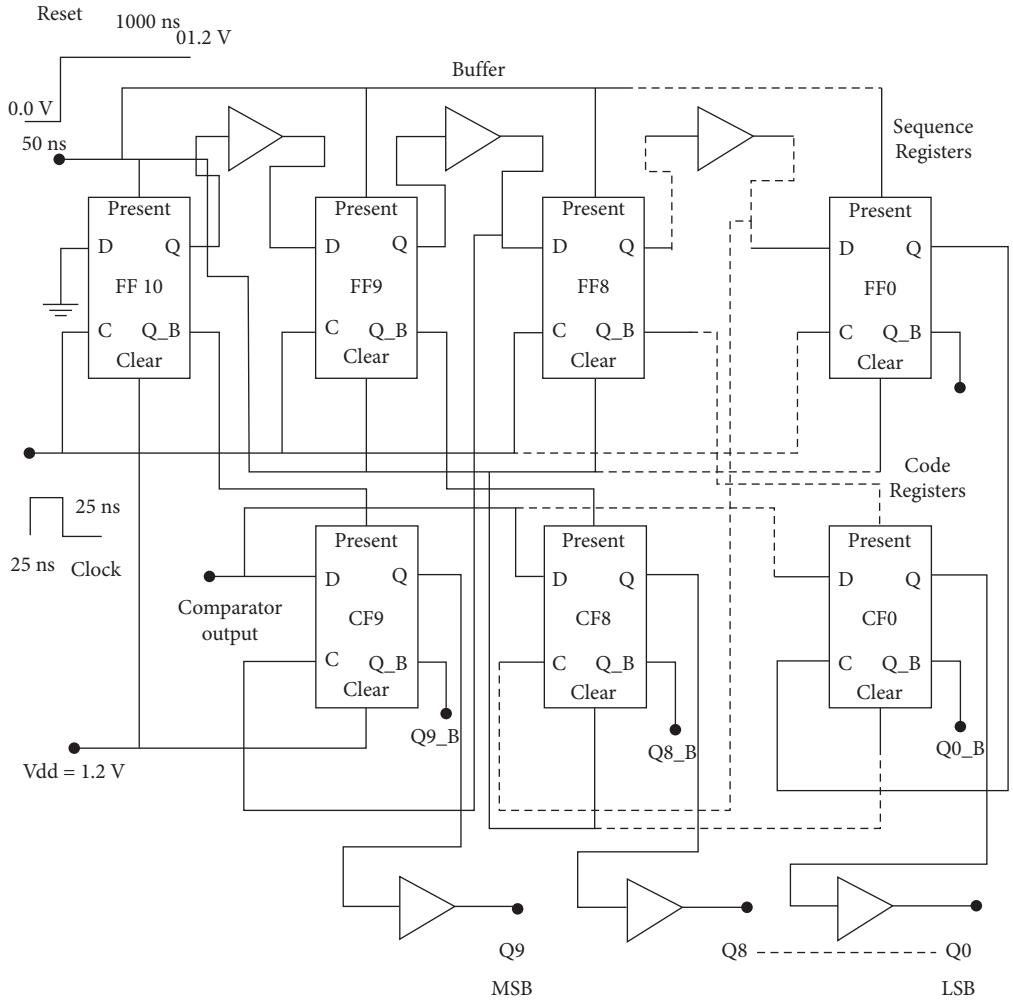

Figure 36: Schematic of the sequence/code register SAR logic [92].

clock. A modified synchronous timing strategy [90] is used for a fixed time in each cycle and variable time in DAC and comparator timing. The settling time of DAC is stretched, and the comparison time is diminished.

To improve the speed and power consumption of SAR ADC, an asynchronous scheme [7, 11, 16, 17, 24, 35, 44, 53, 58, 64, 86, 91] is employed, as shown in Figure 35. Also, the complexity and area of SAR control logic are minimized. Unlike the bit decision in the asynchronous scheme, it is generated without the need for an external clock cycle for every bit. In the end, the LSB is determined, and the reset clock and the end of conversion (EOC) are generated to hold the next sampled signal.

Two different implementations of SAR register and its logic control are used, including the sequence/code register and nonredundant SAR logic [92]. The sequence/code register [10, 11, 29, 33, 92, 102, 103] shown in Figure 36 is divided into two groups of registers. A set of sequence registers is arranged as a ring counter to determine the output bits. The second group of code registers is formed to save the bit decision.

While in the nonredundant SAR logic [4, 31, 64, 92], the number of registers has shrunk to less than half the sequence/code structure. This structure depends on the state of each bit and the previous bits' state, as indicated in Figure 37. Thus, the dynamic power consumption and area of the nonredundant design are diminished.

As mentioned above, the essential algorithm of SAR ADC is based on initially comparing the MSB during the quantization process. Then, the bit iteration starts from the MSB until the LSB, where the reference voltage changes in each iteration. Therefore, the number of bit cycles for conversion is determined by N cycle iteration by N resolution of SAR ADC. A different algorithm called the prediction algorithm [93–100] has been adopted to achieve power consumption savings and reduce the N cycle iterations. In the prediction algorithm, advanced information on the sampled value may be detected by a controlled SAR logic register [93]. The logarithmic methodology is utilized to scale down signal activity. This resulted in decreasing the dissipated energy during the conversion process.

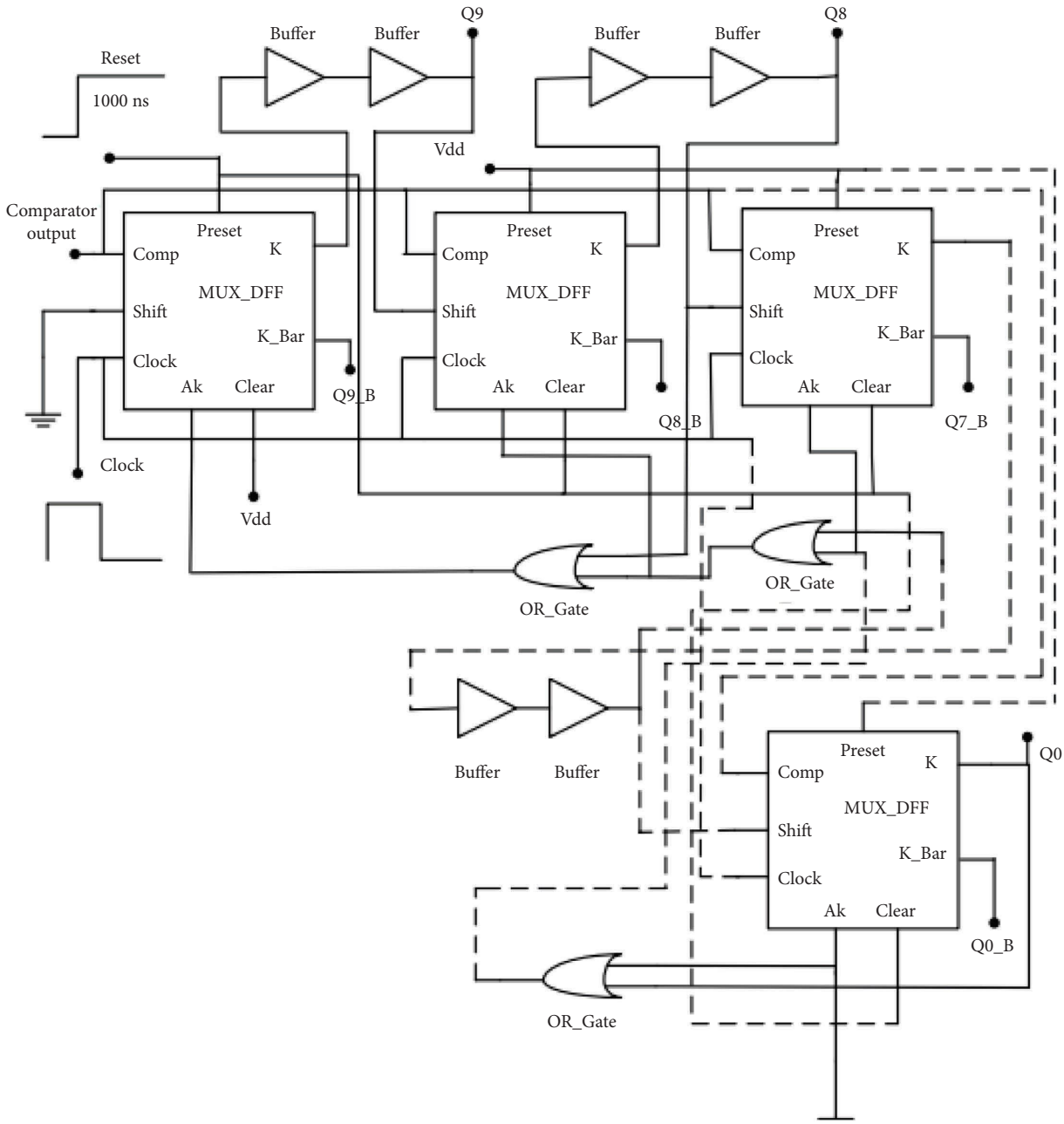

Figure 37: Schematic of the nonredundant register SAR logic [92].

Another work employs the modified LSB-first algorithm [94] to obtain the difference between adjacent samples. This scheme reduces the number of bit cycles through the conversion operation as well as the size of the capacitor array.

Also, work in [95, 96] applies the LSB-first algorithm with a self-adaptive window for higher energy savings. A quantization window [96] is defined as the space between two reference voltages where the input is located at a given time. Two categories are considered, including the constant-size window (static window) and the dynamic window of each cycle. The adaptive window has both the advantages of the two categories.

Similarly, a floating window tracking algorithm [98] is used to turn off the comparator during idle time. Consequently, a three-stage biasing comparator has been employed, including a folded cascade, a differential pair with a cross-coupled load, and a dynamic latch to track the changing input signal. In [99], the prediction of a subrange is completed by achieving two-step loading to diminish the charge variation of the CDAC.

A minimum possible amount of capacitor count is attained in [100]. This algorithm searches for fractions of charge in a charge-sharing DAC and produces a solution based on the smallest possible number of unit capacitors.

7. Summary of the Recently Published SAR ADC Performance Parameters

The SAR ADC achieves high energy efficiency compared with other ADC types. To evaluate the performance efficiency of SAR ADC, a Walden figure of merit (FOM_W) is employed [105]. The FOM_W is considered a very important parameter to indicate how much saving is achieved in power with a certain speed (F_s) and resolution represented by the effective number of bits (ENOB) equation (2). As well, spurious-free dynamic range (SFDR) can be defined as the ratio between the root mean square RMS signal amplitude and the root mean square RMS of the highest unwanted signal over the bandwidth of interest. To improve the linearity, SFDR must be increased, and the differential and integral nonlinearity (DNL/INL) in ADC must be as minimum as possible.

$$\mathbf{FOM_W} = \frac{\mathbf{P_{ADC}}}{2^{\mathbf{ENOB}}\mathbf{F_S}}, \quad (f J/\text{conv.} - \text{step}). \tag{2}$$

A comparison is made with the state-of-the-art techniques of SAR ADC, listed in Tables 3–8. The performance parameters of a single SAR ADC from 2017–2021 are categorized in these tables according to the technology process.

A summary of the recently published SAR ADCs implemented in the 500 nm process is presented in Table 3. According to the performance parameters listed in Table 3, in order to reduce the noise efficiency factor, the three-stage dynamic latch is utilized [1], achieving higher linearity. Also, by using different switching strategies [27], the resolution, speed, and linearity can be enhanced to 14 dB, 17 MS/s, and 95 dB, respectively. An asynchronous converter of [7] is able to reduce power consumption by 14.7 nW.

The performance parameter summary of the implementation of SAR ADC in 180 nm CMOS technology is demonstrated in Table 4. For reducing power consumption, the low sampling rate in [11, 12, 24, 39, 47, 63] is utilized. The different hybrid voltage switching schemes employed in [39, 47] reduce the power consumption and FOM_W. The minimum power consumption has been achieved in [47] by 4.1 nW. Likewise, the PMOS two-stage dynamic latch comparator in [12] diminishes the power consumption by 68 nW. The charge-sharing scheme with the switched capacitor (SC) integrator [63] has accomplished power consumption by 280 nW. Also, a voltage control delay line (VCDL)-based open-loop time-domain comparator has been utilized [24] to improve linearity by up to 85 dB. To minimize the FOM_W, the modified hybrid voltage switching scheme has been attained in [80] by 0.58 fJ/conv.-step. The highest resolution attained is 14 bits. This is achieved using a dual split CDAC array technique [33] or a two-step scaled reference level voltage [87]. Consequently, reducing the mismatch of the capacitor array has been established in [87].

In Table 5, fabrications of SAR ADC in 130 nm CMOS technology are listed. By using the dual split CDAC array technique [34] and a low sampling rate, the power consumption is reduced to 110 nW. Also, the low power consumption has been achieved by 960 nW and 850 nW and enhanced the linearity by 85.4 dB SFDR and 86.5 dB SFDR by using a dynamic tracking algorithm [97] and predictive with a two-step loading algorithm [99], respectively.

Table 6 reports the implemented SAR ADCs in 90 nm CMOS technology. Low power consumption of 74 nW and FOM_W of 1.25 fJ/conv.-step have been attained in [96] by using a timing control adaptive window. The MSB-splitting technique with a low sampling rate [40] has minimized the power consumption by 337.66 nW.

A novel LSB-first algorithm [94] has reduced the power consumption to 60.8 nW and enhanced the linearity (SFDR) to 70.6 dB, as presented in Table 7, in 65 nm CMOS technology. Likewise, the proposed modified algorithm [100] has diminished the power consumption of SAR ADC to 318.2 nW.

Table 8 reports the performance parameters summary of the SAR ADC less than 65 nm process. To save more power, the work [3] has employed the main structures of the building blocks of SAR ADC, including a bootstrap switch followed by a dummy switch, a single-stage dynamic latch comparator, a two-stage subarray capacitor technique, and a conventional synchronous SAR logic. Furthermore, the use of downsize technology of 45 nm support can decrease the power consumption by 422.3 nW with a FOM_W of 3.12 fJ/conv.-step. In addition, the power consumption has been reduced to 510 nW by using the reswitching technique [45]. As well, the linearity (SFDR) enhancement of this technique has reached 81.72 dB with a FOM_W of 1.1 fJ/conv.-step.

Concluding the following from the previous tables:

(i) For ultralow power consumption, the complement differential pair of the dynamic latch [7] reaches 14 nW. As well, the modified hybrid voltage switching scheme [39, 80] attains 42 nW and 43 nW, respectively. Also, the LSB capacitor technique [47], the dual split CDAC array technique [34], and the charge-sharing scheme with a switched capacitor (SC) integrator [63] achieve 4.1 nW, 110 nW, and 280 nW, respectively. Moreover, the timing control adaptive window [96], a novel LSB-first algorithm [94], and the modified algorithm with a minimum possible amount of capacitor count [100] accomplish 74 nW, 60.8 nW, and 318.2 nW, respectively. Furthermore, the main structures of the building blocks of SAR ADC, including a bootstrap switch, a two-stage dynamic latch comparator, and a two-stage subarray capacitor technique with fully differential [5] or single-ended [11], obtained 306 nW and 250 nW, respectively. These works have been implemented at a low sampling frequency suitable for biomedical applications.

(ii) The FOM_W makes a good tradeoff between power, sampling frequency, and resolution. The best results FOM_W are achieved with less than 1.25 (fJ/conv.-step) in the modified voltage switching scheme [45, 80] and the quantization window of the SAR control logic algorithm [96].

Table 3: Summary of the recently published SAR ADC performance parameters in 500 nm process.

Reference	Supply (v)	Power (w)	Area (mm^2)	F_s (S/s)	Resolution (dB)	ENOB (dB)	SNDR (dB)	SFDR (dB)	DNL (LSB)	INL (LSB)	FOM_W (fJ/conv.-step)
[1]**	3.3	21.9 μ	—	10 k	8	7.32	—	—	1.9/−1.9	0.17/ −0.28	31.4
[27]*	5	20.6 m	1.7	17 M	14	13.08	80	95	0.63/ −0.74	0.95/ −0.58	139.9
[7]**	—	14.75 n	—	2 k	10	—	—	—	—	—	—

*Simulated. **Measured.

Table 4: Summary of the recently published SAR ADC performance parameters in 180 nm process.

Reference	Supply (v)	Power (w)	Area (mm^2)	F_s (S/s)	Resolution (dB)	ENOB (dB)	SNDR (dB)	SFDR (dB)	DNL (LSB)	INL (LSB)	FOM_W (fJ/conv.-step)
[24]**	0.8	647 n	0.23	20 K	12	10.48	64	85	0.49/−0.41	0.47/−0.42	22
[87]**	3.3	477.2 μ	—	150 K	14	11.3	70.28	82.91	1.4/−0.25	1.1/−2.1	—
[98]**	1	12.2 μ	0.05	—	5	—	—	—	—	—	—
[2]**	1.5	2.7 μ	0.052	50 K	12	—	66.51	77	0.83/−0.26	0.88/−0.61	30.5
[6]*	1.8	1.9 μ	0.086	10 K	13	12.6	—	—	—	—	30.6
[63]*	1.8	0.28 μ	0.17	2 K	11	10.14	62.8	74.4	0.1/−0.6	0.35/−0.84	120
[39]*	0.6	42 n	—	20 K	10	9.4	58.2	73.7	0.572/−0.569	0.533/−0.422	3.11
[19]*	0.5	13.99 μ	—	1 M	10	7.69	61.96	68.54	0.9/−0.82	1.06/−1.31	—
[33]*	1.5	90.15 μ	—	1 M	14	11	67.9	—	0.4/−0.2	1/−1	—
[8]*	1.2	310 n	—	13.56 M	12	11.8	—	76.4	0.5/−0.68	0.62/−0.56	—
[29]*	1.2	76.88 μ	0.19	20 M	5	4.74	30.3	40	max −1	Less than 1.1	144
[67]*	1.8	0.26 μ	—	25 K	8	7.1	—	50.1	0.45–0.7	−0.9	7.58
[80]*	0.6	43.7 n	0.1035	100 K	10	9.55	59.3	78.2	0.28/−0.24	0.67/−0.41	0.58
[47]*	1A/0.5D	4.1 n	0.0249	1 K	10	9.73	60.3	69.8	0.31/−0.3	0.32/−0.2	4.1
[53]**	1.8	490 μ	—	1 M	—	10.76	66.54	78.42	0.72/−0.55	0.92/−0.78	57.2
[16]*	1.8/0.9	6.98 μ	—	200 K	9	8.3	51.9	56.2	—	—	111
[11]**	0.75	250 n	0.12	10 K	11	9.76	60.5	72	0.6/−0.37	0.94/−0.89	28.8
[66]**	1.2	90 μ	0.16	3.125 M	10	7.41	46.37		5.64/−1	4.76/−4.24	169000
[5]**	1	306 n	0.05	40 K	10	9.02	56.1	67	0.56/−0.69	1.14/−0.7	14.3
[10]**	1.8	78.8 μ	—	50 M	10	—	—	—	—	—	—
[12]**	0.5	68 n	0.144	10 K	10	9.3	57.8	61.6	0.41/−0.45	0.57/−0.48	10.8
[65]*	1.8A/ 0.9D	9.7 μ	0.35	50 K	12	—	68.6	—	—	—	88.4
[52]*	1.8	5.18 m	—	100 M	13	12.15	76.1	—	0.37/−0.44	0.56/−0.45	9.65
[83]**	1.8	3.8 m	0.23	10 M	10	8.5	53.1	60.9	2.8/−1	3.7/−3.6	—

Table 5: Summary of the recently published SAR ADC performance parameters in 130 nm process.

Reference	Supply (v)	Power (w)	Area (mm^2)	F_s (S/s)	Resolution (dB)	ENOB (dB)	SNDR (dB)	SFDR (dB)	DNL (LSB)	INL (LSB)	FOM_W (fJ/conv.-step)
[89]*	1.2	11.56 μ	—	1 M	8	7.51	47.12	57.36	0.26/−0.24	0.26/−0.28	62.11
[23]**	0.4	2.66 μ	—	250 k	9	6.66	41.91		0.49/−0.44	3.24/−1.31	105.4
[99]*	0.6	0.85 μ	0.12	10 k	12	11.76	—	86.5	—	—	—
[34]**	1	110 n	0.16	1 k	12	10.47	64.8	78.5	0.35/−0.41	0.6/−0.74	76
[97]*	0.6	0.96 μ	0.126	10 k	12	11.77	72.6	85.4	—	—	28

Table 6: Summary of the recently published SAR ADC performance parameters in 90 nm process.

Reference	Supply (v)	Power (w)	Area (mm^2)	F_s (S/s)	Resolution (dB)	ENOB (dB)	SNDR (dB)	SFDR (dB)	DNL (LSB)	INL (LSB)	FOM_W (fJ/conv.-step)
[31]*	1	42.82 m	—	125 M	14	13.16	—	—	±0.16	±0.16	37.43
[58]**	1.2	0.664 m	0.024	50 M	10	9.26	57.6	65.8	0.36/−0.32	0.45/−0.38	21.68
[103]*	1	77.26 μ	—	1 M	6	5.91	—	—	—	—	—
[40]*	0.5	337.66 n	—	10 k	10	—	55.93	77.17	—	—	65.1875
[64]*	0.7	931 n	0.00145	0.78 M	8	6.71	44.45	61	0.87/−0.54	1.37/−1.59	11.39
[96]**	0.35	74 n	—	100 k	10	9.21	57.3	—	0.37/−0.45	0.37/−0.42	1.25
[102]*	1.2	10 μ	—	100 k	8	—	—	—	—	—	—
[70]*	1	500 n	—	100 k	10	8.5	52.84	55.92	—	—	9.76

Table 7: Summary of the recently published SAR ADC performance parameters in 65 nm process.

Reference	Supply (v)	Power (w)	Area (mm^2)	F_s (S/s)	Resolution (dB)	ENOB (dB)	SNDR (dB)	SFDR (dB)	DNL (LSB)	INL (LSB)	FOM_W (fJ/conv.-step)
[68]*	1.2	21 μ	—	1 M	8	7.9	49.3	61	—	—	87.9
[94]**	1.2	60.8 n	0.09	10 k	10	9.4	58.4	70.6	0.4/−0.24	0.39/−0.36	9
[100]*	0.5A/1.1D	318.2 n	—	100 k	10	8.55	53.23	61.87	—	—	—
[73]*	1.2	—	—	100 k	10	—	—	—	—	—	—

Table 8: Summary of the recently published SAR ADC performance parameters in less than 65 nm process.

Reference	Process (nm)	Supply (v)	Power (w)	Area (mm^2)	F_s (S/s)	Resolution (dB)	ENOB (dB)	SNDR (dB)	SFDR (dB)	DNL (LSB)	INL (LSB)	FOM_W (fJ/conv.-step)
[90]**	40	1.1	1.3 m	0.04	160 M	12	9.21	57.18	75.29	—	—	13.71
[86]**	55	1	14.8 μ		1 M	10	9.74	60.39	—	0.7/−0.5	0.6/−0.7	17.3
[36]**	55	0.9	40.2 μ	0.029	10 M	12	10.03	62.13	73.52	0.45/−0.46	1.15/−1.68	3.85
[3]*	45	1.1	422.3 n	—	200 k	10	9.41	—	—	0.2	0.4	3.12
[35]**	40	1.1	1.32 m	0.037	100 M	10	9.3	58.03	72.6	0.62/−0.4	0.67/−0.54	130
[45]**	40	0.7	0.51 μ	0.014	200 k	12	11.19	69.1	81.72	0.45	0.79	1.1
[17]**	14	0.85	7 m	0.006	300 M	12	—	60.5	78.5	—	—	—

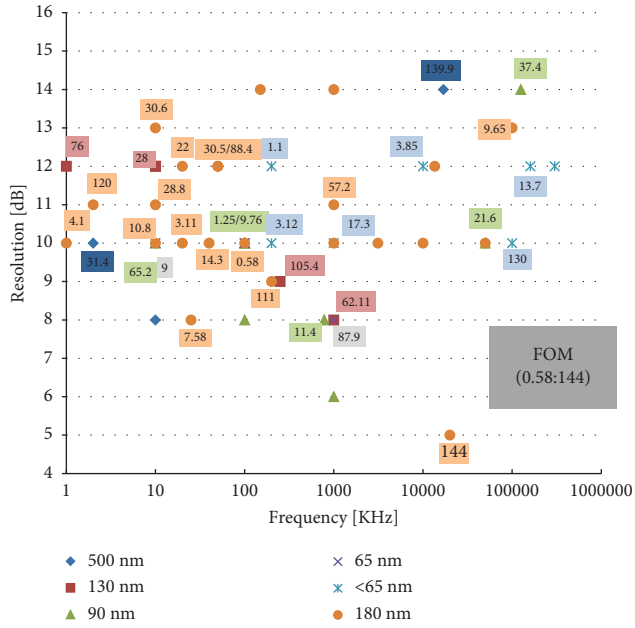

Figure 38: Single SAR ADC performance survey (2017–2021).

(iii) In order to achieve a higher resolution above 12 dB with maximum linearity up to 85 dB, the two-stage subarray capacitor technique with a new strategy of voltage switching array [27] has been proposed. Also, a segmented CDAC array [24] has attained high resolution with higher linearity. Furthermore, the predictive algorithm [99] and the dynamic tracking algorithm [97] have obtained good results.

(iv) As the resolution increases, the mismatch of the capacitor array increases. Therefore, the linearity of SAR ADC decreases. The downsizing of CMOS technologies supports the increase in sampling frequency.

In Figure 38, the resolution of SAR ADC is plotted versus the sampling frequency and FOM with different implementation technologies. The numbers in squares show FOM_W of each technique with different technology. It can be noted that more than half the total power is consumed by the DAC, which is dedicated to the capacitor array and switching mechanism.

The key issue to reducing energy consumption is the downsizing of the array capacitors and the use of different level voltages instead of one level voltage. Table 9 summarizes the energy performance of prior published DACs. The main issue is to maximize power savings. Mainly, two parameters have been utilized to achieve power consumption reduction: decreasing the size of the capacitor array and using different level voltages. The

Table 9: Performance summary of energy-efficient in DAC with MATLAB.

Reference	Average switching energy (CV^2_{REF})	Energy savings (%)	Number of required unit capacitors	Capacitor area reduction (%)	Reset energy (CV^2_{REF})	Dependency on the accuracy of V_{CM}	Max. common mode variation
[25]	1363.3	Ref	2048	Ref	—	No	No
[70]	0	100	266	87	—	No	No
[46]	26.7	98.4	512	75	—	Only LSB	1 LSB
[37]	21.3	98.4	512	75	—	Only LSB	0.5 LSB
[79]	21.3	98.7	512	75	—	From second bit	$V_{REF}/2$
[43]	10.54	99.23	512	75	0	From second bit	—
[72]	170.4	87.5	256	87.5	—	No	No
[81]	63.56	95.34	512	75	—	Only LSB	$V_{REF}/4$
[82]	106.2	92.2	1024	50	—	—	$V_{REF}/4$
[48]	10.8	99.2	256	87.5	48.12	From third bit	$V_{REF}/4$
[83]	26.4	98.1	512	75	—	From second bit	—
[80]^{2018}	7.94	99.4	512	75	—	From third bit	$V_{REF}/4$
[54]	17.6	99.01	384	81.25	0	From second bit	$V_{REF}/4$
[84]	9.38	99.31	512	75	74.58	Only LSB	$V_{REF}/2$
[73]	170.4	87.5	256	87.5	—	No	No
[41]	5.3	99.61	1024	50	0	—	$V_{REF}/16$
[57]	6.573	99.52	1616	21.09	24.1	No	No
[88]	48.03	96.48	256	87.5	—	—	—
[47]	31.75	97.67	256	87.5	63.875	From third bit	$V_{REF}/4$
[30]	6.7472	99.51	132	93.55	0.554	—	No
[59]	27.4	98	563	72.5	0	—	—
[56]	8.6	99.37	288	86	0	From second bit	$V_{REF}/32/$
[40]	42.417	96.89	1024	50	—	No	No
[42]	26.54	98.05	512	75	0	From second bit	$V_{REF}/4$
[60]	6.955	99.49	1024	50	—	From third bit	$V_{REF}/2$
[28]	2.9	99.8	292	86	0	From second bit	$V_{REF}/4$
[50]	9.6	99.3	268	87	0	From second bit	$3V_{REF}/8$
[49]	21.6	98.9		87.2	0	From second bit	$V_{REF}/4$
[58]	63.5	95.34	256 + 2Cs	82.61	—	Only LSB	$V_{REF}/2$
[55]	4.3491	99.68	163	92	0	From third bit	$V_{REF}/4$
[39]	26.58	70	512	75	—	From second bit	1 LSB
[71]	52.7	92.3	1024	50	—	No	No
[89]	29.3	97.85	256	87.5	—	From second bit	$V_{REF}/4$
[38]	21.21	98.4	256	87.5	127.75	From second bit	0.5 LSB
[85]	11.8502	99.13	162	92.1	0.1367	From third bit	231 LSB (231 $V_{REF}/512$)
[44]	55.44	95.93	512	75	127.75	No	No

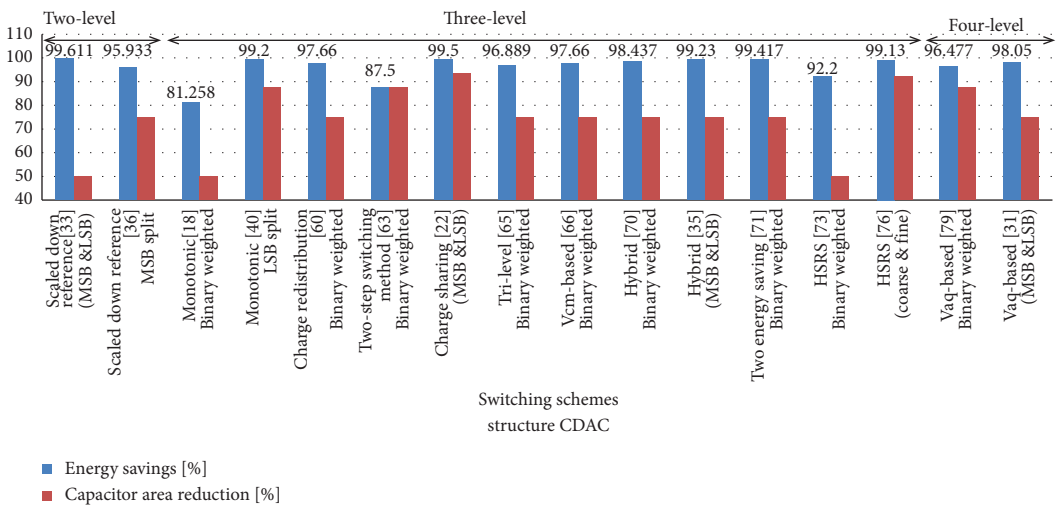

Figure 39: Some main CDAC structures and voltage switching schemes versus the energy-efficient.

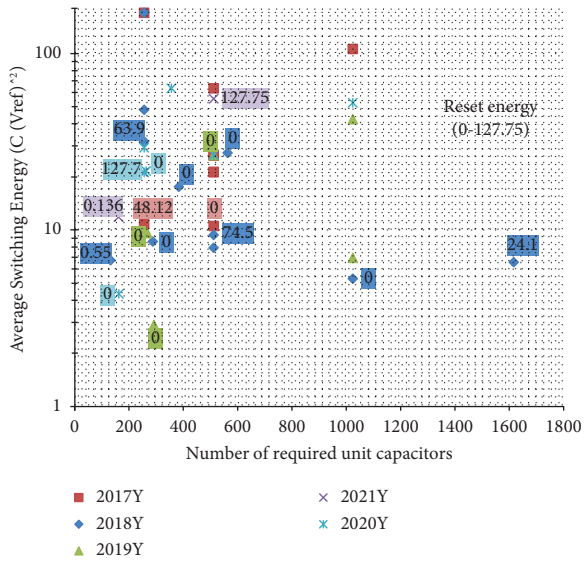

Figure 40: The energy-efficient of a single SAR ADC (2017–2021).

CDAC is suitable for the low-power SAR ADC. However, the different voltage switching schemes can improve the switching power consumption. Consequently, energy savings are enhanced. The various structures of CDAC can control the number of capacitors and capacitor area reduction. In Figure 39, the energy savings and capacitor area reduction are shown versus switching schemes and CDAC structure at different level voltages. It can be noted that the selection of CDAC structures and voltage switching schemes is necessary to achieve the required specifications. In the low-power SAR ADC for biomedical applications, the charge-sharing voltage switching scheme with two arrays (MSB and LSB) in the CDAC structure [30] has achieved a suitable specification. Also, the HSRS voltage switching scheme with two arrays (coarse and fine) in the CDAC structure [85] has arrived at the low-power DAC. For the zero reset energy, the scaled-down reference [41] and hybrid [43] voltage switching schemes with two arrays of the CDAC structure can be attained by using the two-step reset method and the single-side switching method, respectively. Figure 40 demonstrates the average switching energy versus the number of required unit capacitors ($\mathbf{C_u}$) with reset energy from 2017–2021. Several designs achieve at least 10 $\mathbf{CV^2_{ref}}$ average switching energies and capacitor areas lower than 200 $\mathbf{C_u}$ [30, 55]. But these designs have not been implemented in CMOS technology.

8. Conclusions

Recent progress on the single SAR ADC architecture design has been reviewed. Concerning low-power considerations, the SAR ADC architecture design is a suitable choice among other ADC architectures for biomedical applications. By using a dual-split CDAC array technique, a high resolution of 14 bits with a high speed of 125 MS/s has been implemented. Also, for ultralow power consumption, a power consumption of 4.1 nW with a FOM_W of 0.58 (fJ/conv.-step) has been achieved by the development of voltage switching schemes. High linearity with an SFDR of 95 dB has been realized by reducing the number of switches and mismatched capacitors. The tradeoff between energy saving of 99.51% and capacitor area reduction of 93.55% from the conventional CDAC technique has been attained by hybrid capacitor techniques. So, the development of a single SAR ADC architecture is mainly interested in DAC structure and voltage switching schemes.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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