Research Article

Exact Analysis and Physical Realization of the 6-Lobe Chua Corsage Memristor

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A novel generic memristor, dubbed the *6-lobe Chua corsage memristor*, is proposed with its nonlinear dynamical analysis and physical realization. The proposed corsage memristor contains *four* asymptotically stable equilibrium points on its complex and diversified dynamic routes which reveals a *4-state nonlinear memory device*. The higher degree of versatility of its dynamic routes reveal that the proposed memristor has a variety of dynamic paths in response to different initial conditions and exhibits a highly nonlinear *contiguous* DC *V-I* curve. The DC *V-I* curve of the proposed memristor is endowed with an explicit *analytical parametric representation*. Moreover, the derived *three formulas*, exponential trajectories of state $x_n(t)$, time period t_{fn} , and minimum pulse amplitude V_A , are required to analyze the movement of the state trajectories on the piecewise linear (PWL) dynamic route map (DRM) of the corsage memristor. These *formulas* are universal, that is, applicable to any PWL DRM curves for any DC or pulse input and with any number of segments. Nonlinear dynamics and circuit and system theoretic approach are employed to explain the *asymptotic quad-stable behavior* of the proposed corsage memristor and to *design a novel real memristor emulator* using *off-the-shelf* circuit components.

1. Introduction

Memristor, the acronym of memory resistor, is one of the most propitious elements in the emerging memory sector due to its exclusive attributes under DC or AC excitations, as well as its miniature nanoscale physical dimension. Extensive research is ongoing on memristors and the memristive system after the seminal paper published by *hp* in 2008 [1]. Memristor, the fourth basic circuit element, was postulated by Chua [2] and later generalized to a broader class of dynamical devices which exhibit interesting and valuable circuit-theoretic properties [3].

Recently, several researchers investigated the multistate phenomena in generic and extended memristors [4–7]. This important research direction could lead to another stage of technical innovation in the memristor area. The principle

of the multistate memristor can be explained using the nonlinear dynamics theory as well as circuit and system theoretic concepts [4–6]. For example, the locally active generic Chua corsage memristor exhibits an asymptotical stability via the supercritical Hopf bifurcation [8–9]. Once an initial state is set, the state alters following its nonlinear dynamic route. The state changing is repeated until the state reaches a particular state which is termed as an “attractor.” In this type of memristors, the state space contains various attractors and each attractor has its own basin of attraction [10]. When inputs or noises are applied at a stable equilibrium state of the generic corsage memristor, the equilibrium state is moved by the amount of time integral of the inputs. However, unless the state moves beyond the boundary of current basin of attraction, the state returns back to its original equilibrium state (attractor) [8, 9]. Therefore, it can

become a robust memory device. Since a part of the previous programming history of the corsage memristor is lost in this procedure, the phenomenon is known as “local fading memory” in bistable and multistate memory devices [4].

Another feature of this type of multistate corsage memristor is the alteration of the stable equilibrium states. In this case, a sufficiently large amplitude with short pulse width or a minimum pulse amplitude with lengthy pulse width is applied across the memristor to switch the state from one stable equilibrium state to another stable state by converging into the basin of a new stable attractor. In this way, the equilibrium state of a multistate corsage memristor is changed to a new stable state where the resistances or conductances of each stable equilibrium state are distinguishably different from each other [7]. The alteration of the stable equilibrium states of corsage memristors is determined by the function of its input and initial condition, and henceforth, the corsage memristors exhibit multistability and eventually can be used as multistate memory devices.

In this paper, we demonstrate a novel quad-stable generic memristor, dubbed the *6-lobe Chua corsage memristor*. The dynamic routes of the 6-lobe corsage memristor have *four* asymptotically stable equilibrium points and *three* unstable equilibrium points at the DC input voltage $V=0$ V. The *four* asymptotically stable equilibrium points of the proposed memristor define the corresponding four distinct resistance levels and can be used to develop a multibit-per-cell memory device similar to the unidirectional spin Hall magnetoresistance [11]. The multistable memory states are distinguishable by resistance levels in accordance to stable equilibrium points where the memory states can be defined with a pair of bits. To ease the demonstration of the switching kinetics of multistable memory states of the proposed memristor, we derived *three universal formulas* regarding the exponential state $x_n(t)$, the time period t_{fn} , and the minimum pulse amplitude V_A .

In addition to the theoretical insights, we have designed and built a real emulator circuit of the proposed corsage memristor. For the physical realization of the piecewise linear 6-lobe Chua corsage memristor, we use the Graetz bridge [12] circuit in parallel with an *active and locally active* resistor [5]. Concepts from circuit and system theory, and techniques from nonlinear dynamics theory, are employed in this paper to elucidate the key mechanisms underlying the emergence of switching strategies of quad-stable memory.

The rest of the paper is organized as follows: the 6-lobe corsage memristor is designed and introduced in Section 2. The parametric representation and DC V - I curve are analyzed in Section 3. The switching kinetics and the physical implementation of the proposed corsage memristor are described in Sections 4 and 5, respectively, followed by the concluding remarks in Section 6.

2. 6-Lobe Chua Corsage Memristor Model

The *6-lobe Chua corsage memristor* is an extension of the 1st-order locally active Chua corsage memristor [8]. It is a

piecewise linear (PWL) memristor whose state-dependent Ohm's law and state equation are as follows:

$$i = G(x)v, \quad (1)$$

where

$$G(x) = G_0 x^2, \quad (2)$$

and

$$\frac{dx}{dt} = f(x) + v, \quad (3)$$

where

$$f(x) = 33 - x + |x - 6| - |x - 12| + |x - 20| - |x - 30| + |x - 42| - |x - 56|, \quad (4)$$

and x , i , and v denote the memristor state, current, and voltage, respectively. In practice, G_0 is a scaling constant chosen to fit the intrinsic memductance scale of the memristor. In this paper, we choose $G_0 = 10^{-6}$ so that the current of the 6-lobe Chua corsage memristor can be measured in *milliamperes (mA)* [7].

2.1. Frequency-Dependent Pinched Hysteresis Loops. The frequency-dependent pinched hysteresis loops of a device, when driven by any periodic input current or voltage source with a zero DC component, are a signature of a memristor or memristive system [13]. The 6-lobe Chua corsage memristor defined in (1), (2), (3), and (4) exhibits frequency-dependent pinched hysteresis loops when it is driven by a sinusoidal input signal $v(t) = A \sin(\omega t)$ where $A = 5$ V, as shown in Figure 1. The input voltage $v(t)$ and the corresponding memristor current $i(t)$ are shown in the upper-right side of Figure 1(a), and the memristor state $x(t)$ and memductance $G(t)$ are shown in the lower-right side of Figure 1(a), whereas the left side of Figure 1(a) shows the memristive circuit diagram with AC excitation. The frequency-dependent pinched hysteresis loops are shown in Figure 1(b) for frequencies $\omega = 1$ rad/s, 10 rad/s, 20 rad/s, and 100 rad/s. The lobe area of the pinched hysteresis loops shrinks as the frequency increases and tends to a straight line for $\omega \geq 100$ rad/s as shown in Figure 1(b) [14]. It follows that the proposed corsage memristor is a generic memristor [15].

2.2. Dynamic Routes with Their Phase Portrait. The dynamic route of a nonlinear system prescribes the dynamics of nonlinear differential equations [14]. The dynamic route of the *short-circuited* ($v=0$ V), namely, the *power-off-plot (POP)*, 6-lobe Chua corsage memristor is shown in Figure 2 where (5) is used to plot the loci of $dx/dt|_{v=0}$ versus x .

$$\frac{dx}{dt} \Big|_{v=0} = \hat{f}(x) = 33 - x + |x - 6| - |x - 12| + |x - 20| - |x - 30| + |x - 42| - |x - 56|. \quad (5)$$

FIGURE 1: Frequency-dependent pinched hysteresis loop fingerprint of the 6-lobe Chua corsage memristor, calculated with initial state $x(0) = 5$: (a) the input voltage $v(t)$ (in red), corresponding memristor current $i(t)$ (in blue), memristor state $x(t)$ (in magenta), and memconductance $G(t)$ (in green) of the 6-lobe Chua corsage memristor; (b) frequency-dependent pinched hysteresis loops for zero-mean periodic input $v(t) = A \sin(\omega t)$ where $A = 5$ V and frequency $\omega = 1$ rad/s, 10 rad/s, 20 rad/s, and 100 rad/s.

The arrowheads in Figure 2 indicate the *direction of motion* of the state variable x from any initial state $x(0)$.

Figure 2 shows that for any initial state $x(0)$ on the *upper half* of the POP, where $dx/dt > 0$, the state variable $x(t)$ must move to the *right* as $x(t)$ increases with time, depicted by the purple arrowheads pointing to the right in Figure 2. On the contrary, for any initial state $x(0)$ on the *lower half* of the POP, where $dx/dt < 0$, the state variable $x(t)$ decreases with time and must move to the *left*, depicted by the black arrowheads pointing to the left in Figure 2. In the

theory of *nonlinear dynamics* [16], the stationary points where $dx/dt = 0$ or $\hat{f}(x)$ intersects the x -axis; are known as *equilibrium points*. Figure 2 shows that $\hat{f}(x)$ intersects the x -axis at seven points, namely, $x = X_{Q1} = 3$ (Q_1), $x = X_{Q2} = 9$ (Q_2), $x = X_{Q3} = 15$ (Q_3), $x = X_{Q4} = 25$ (Q_4), $x = X_{Q5} = 35$ (Q_5), $x = X_{Q6} = 49$ (Q_6), and $x = X_{Q7} = 63$ (Q_7). The equilibrium points Q_1 , Q_3 , Q_5 , and Q_7 are stable whereas Q_2 , Q_4 , and Q_6 are unstable equilibrium points because the state variable $x(t)$ diverges away from Q_2 , Q_4 , and

FIGURE 2: Dynamic route map of the 6-lobe Chua corsage memristor at $V=0$ V is called the *power-off-plot* (POP).

Q_6 . Moreover, the equilibrium points Q_1 , Q_3 , Q_5 , and Q_7 in Figure 2 are stable as the corresponding eigenvalues of those equilibrium points are negative real numbers whereas Q_2 , Q_4 , and Q_6 are unstable as the eigenvalues are positive [17].

Figure 2 shows that for any initial state $x(0) > X_Q + \delta x$, where $X_Q \in \{X_{Q2}, X_{Q4}, X_{Q6}\}$, the unstable equilibrium points Q_2 , Q_4 , and Q_6 converge to stable equilibrium points Q_3 , Q_5 , and Q_7 , respectively, to their right as shown with purple arrowheads. In contrast, for any initial state $x(0) < X_Q - \delta x$, Q_2 , Q_4 , and Q_6 converge to stable equilibrium points Q_1 , Q_3 , and Q_5 , respectively, to their left as shown with black arrowheads.

The phase portrait of stable equilibrium states Q_1 , Q_3 , Q_5 , and Q_7 is shown in Figure 3 where the dotted straight lines represent the separatrices between two stable equilibrium states and pass through the unstable equilibrium points Q_2 , Q_4 , and Q_6 , respectively. Similar to Figure 2, Figure 3 also shows that for any $x(0) > (X_{Q2} \text{ or } X_{Q4} \text{ or } X_{Q6})$, the trajectories of $x(t)$ converge to Q_3 , Q_5 , and Q_7 , respectively, as shown with purple arrowheads. Conversely, for $x(0) < (X_{Q2} \text{ or } X_{Q4} \text{ or } X_{Q6})$, $x(t)$ converges to Q_1 , Q_3 , and Q_5 , respectively, as shown with black arrowheads.

The dynamic routes in Figure 2 and the phase portrait in Figure 3 illustrate that the proposed memristor can be used as a 4-state or multibit-per-cell (2-bit) memory device at $v=0$ V.

The more stable equilibrium states of the 6-lobe corsage memristor increases the memory efficiency per device 50% and 25% compared to 2-lobe and 4-lobe corsage memristors, respectively, and eventually enhance the

capability to represent a desired function more closely than 2-lobe or 4-lobe corsage memristors.

3. Parametric Representation and the DC V-I Curve

In mathematics, parametric representation of an object is a collection of parametric equations which are used to express the coordinates of the points that make up a geometric object [18] where those parametric equations are defined by a group of quantities based on a function of one or more independent variables [19].

3.1. Parametric Representation. The parametric representation of the 6-lobe Chua corsage memristor can be derived by equating state (3) to zero ($dx/dt=0$) and solving for the following equilibrium points (6) for each DC input voltage $v=V$, at the DC equilibrium state $x=X(V)$:

$$\begin{aligned} \frac{dx}{dt} = & (33 - x + |x - 6| - |x - 12| + |x - 20| - |x - 30| \\ & + |x - 42| - |x - 56|) + v = 0. \end{aligned} \quad (6)$$

The DC voltage of the proposed corsage memristor is given explicitly by

$$\begin{aligned} V = & -(33 - x + |x - 6| - |x - 12| + |x - 20| - |x - 30| \\ & + |x - 42| - |x - 56|) \triangleq \hat{v}(X). \end{aligned} \quad (7)$$

FIGURE 3: Phase portrait of the stable equilibrium states Q_1 , Q_3 , Q_5 , and Q_7 . The horizontal dotted lines are the separatrices and pass through the unstable equilibrium states Q_2 , Q_4 , and Q_6 , respectively.

The parametric representation of the DC current of the 6-lobe cossage memristor can be derived by substituting V given by (7) for v in (1) with $G_0 = 10^{-6}$, namely,

$$I = -G_0 X^2 (33 - x + |x - 6| - |x - 12| + |x - 20| - |x - 30| + |x - 42| - |x - 56|) \triangleq \hat{i}(X). \quad (8)$$

The parametric representations of the proposed cossage memristor are shown in Figure 4 where Figures 4(a) and 4(b) show the loci of the parametric representation of $V = \hat{v}(x)$ versus X and $I = \hat{i}(x)$ versus X , respectively. The loci of the parametrically represented $V = \hat{v}(x)$ versus $I = \hat{i}(x)$ are shown in Figure 4(c).

For convenience of readers, several points of the parametric representation of $V = \hat{v}(x)$ and $I = \hat{i}(x)$ of the 6-lobe Chua cossage memristor over the range $\chi = \{X: -12 \leq X \leq 78\}$ are listed in Table 1.

3.2. DC V - I Plot. A circuit-theoretic approach is used to derive the DC V - I loci of the voltage-controlled 6-lobe Chua cossage memristor. Each DC value of voltage V and current I is computed using the following steps:

- (1) For each value of V listed in Table 1, we calculate all equilibria $x = X_k$, $1 \leq k \leq 7$, of the proposed memristor using state (3) where $dx/dt = 0$

$$V = -(33 - x + |x - 6| - |x - 12| + |x - 20| - |x - 30| + |x - 42| - |x - 56|) \triangleq \hat{v}(X). \quad (9)$$

- (2) Then we determine the DC current $i = I$ of the memristor corresponding to each equilibrium point $X = X_1, X_2, \dots, X_N$, $1 \leq N \leq 7$:

$$I = -G_0 X^2 (33 - x + |x - 6| - |x - 12| + |x - 20| - |x - 30| + |x - 42| - |x - 56|) \triangleq \hat{i}(X). \quad (10)$$

- (3) Finally, we draw the DC V - I curve by plotting the coordinates (V, I) on the V - I plane for each value of X .

The DC V - I loci of the 6-lobe cossage memristor is shown in Figure 5 over the input voltage range $-10 \text{ V} \leq V \leq 10 \text{ V}$ where the solid curves correspond to stable equilibrium states and the dash curves correspond to unstable equilibrium states. Since the DC V - I curve contains six contiguous lobes, henceforth call it the “six lobe cossage V - I curve.” The seven different colored DC V - I branches in Figure 5 represent the equilibrium points of the corresponding colors in Figure 3. At $v = 0 \text{ V}$, the state variables are $x = 3$ (red DC V - I curve Q_1), $x = 9$ (fluorescent green DC V - I curve Q_2), $x = 15$ (blue DC V - I curve Q_3), $x = 25$ (magenta DC V - I curve Q_4), $x = 35$ (cyan DC V - I curve Q_5), $x = 49$ (brown DC V - I curve Q_6), and $x = 63$ (green DC V - I curve Q_7). As the values of the state variable of each DC V - I branch at the origin are different, their slopes (i.e., conductances $G(x)$) at the origin are also different according to (2), as tabulated in the upper-left inset of Figure 5. The tabulated upper-left inset shows that the red DC V - I curve represents the lower conductance state (higher resistance state) whereas the green DC V - I curve represents the higher conductance state (lower resistance state). Moreover, the lower-right inset of Figure 5 shows a zoomed portion of the red DC V - I curve over

FIGURE 4: Parametric representations of the 6-lobe Chua corsage memristor (a) voltage $V = \hat{v}(X)$ versus state variable X and (b) current $I = \hat{i}(X)$ versus state variable X , for each value of $\chi = \{X: -12 \leq X \leq 78\}$. (c) DC V - I plot, where the coordinates (V, I) of each point are extracted from (a) and (b), for each value of $\chi = \{X: -7 \leq X \leq 73\}$ for better illustration.

the range $-5 \text{ V} \leq V \leq 2 \text{ V}$. The zoomed red DC V - I curve contains a *negative-slope region* over the voltage range $-3 \text{ V} < V < -1 \text{ V}$ which affirms that the proposed corsage memristor is locally active over the $-3 \text{ V} < V < -1 \text{ V}$ range as $\text{Re}Z(i\omega) < 0$ for DC input voltage ($\omega = 0$) [8]. The locally active negative slope region of the 6-lobe Chua corsage memristor is significant in circuit theory as it might give rise to complexity through which *complex phenomenon and information processing* might emerge [20, 21].

One of the most important features of the 6-lobe corsage memristor is the contiguousness of its DC V - I curve which is

different from many other published nonlinear DC V - I curves which exhibit several *disconnected* branches [14].

Another impressive feature is that the parametric representation and the DC V - I curve of the proposed corsage memristor has an explicit analytical equation, which rarely happens.

4. Switching Strategies of Memory States

The *power-off-plot* in Figure 2 shows that the 6-lobe Chua corsage memristor can be used as a *4-state* or *2-bit*

TABLE 1: Numerical values of the 6-lobe corsage memristor obtained from parametric representation over $-12 \leq X \leq 78$.

X	$V = \hat{v}(X)$ (V)	$I = \hat{i}(X)$ (mA)
-12	-15	-2.16
0	-3	0
3	0	0
6	3	0.11
9	0	0
10	-1	-0.1
12	-3	-0.43
15	0	0
20	5	2
25	0	0
30	-5	-4.5
35	0	0
40	5	8
42	7	12.35
49	0	0
50	-1	-2.5
56	-7	-21.95
60	-3	-10.8
63	0	0
70	7	34.3
78	15	91.26

memory device at $v = 0$ V. Conceptually, the simplest way to switch the memory states of the 6-lobe corsage memristor is to apply a square pulse with an appropriate pulse amplitude V_A and pulse width Δw . For a successful switching between the memory states of the proposed corsage memristor, the square pulse should have a minimum pulse width for an appropriate pulse amplitude, V_A . Any square pulse with less than the minimum pulse width results in switching failure.

The switching kinetics of the 6-lobe Chua corsage memristor can be represented through its *dynamic route map* (DRM). The solution of each straight-line segment of the dynamic route map of our corsage memristor is an exponential function where the complete solution $\mathbf{x}(t)$ is made of a sequence of the exponential waveforms, joined at the various breakpoints in the dynamic routes. In this paper, we derived the following universal exponential state variable $x_n(t)$ formula related to a straight-line segment around an equilibrium point Q_n of the piecewise linear DRM (detailed derivation of $x_n(t)$, t_{fn} , and V_A are provided in the supplementary document (available here).):

$$x_n(t) = Q_n - mv(t) \left(1 - e^{m(t-t_{0n})} \right) - (Q_n - x(t_{0n})) e^{m(t-t_{0n})}, \quad (11)$$

where m represents the sign value of the straight-line slope,

$$m = \text{sgn} \left(\frac{(dx/dt)|_{\text{start}} - (dx/dt)|_{\text{end}}}{x_{\text{start}} - x_{\text{end}}} \right), \quad (12)$$

and t_{0n} is the initial time of the segment whereas $x(t_{0n})$ represents the initial state at t_{0n} . The universal formula of the time, t_{fn} , required for the trajectory of $x_n(t)$ to move from any initial point $x(t_{0n})$ to the end of the straight-line segment is also derived as follows:

$$t_{fn} = t_{0n} + \underbrace{\frac{1}{m} \ln \left[\frac{(Q_n - mv(t) - x(t_{fn}))}{(Q_n - mv(t) - x(t_{0n}))} \right]}_{\Delta t_{fn}}. \quad (13)$$

The appropriate pulse amplitude V_A is computed by replacing $t = t_{fn}$ in (11) and substituting the value of t_{fn} from (13) to (11) where the resultant equation is shown as follows:

$$V_A > Q_{n-1} - x(t_{0(n-1)}), \quad (14)$$

where Q_{n-1} and $x(t_{0(n-1)})$ represent, respectively, the immediate before equilibrium point and the initial state of the resultant memory state Q_n .

The derived universal formulas in (11), (12), (13), and (14) are applicable for any piecewise linear DRM curve of any number of segments and any DC or pulse input $v(t)$. Such exponential analytical solutions can be derived from no nonlinear functions other than the PWL functions.

The dynamic route map (DRM) in Figure 6(a) shows an application of successful switching for an appropriate pulse amplitude V_A and pulse width Δw where the 6-lobe corsage memristor switches from high-resistance (low conductance) state Q_1 to low-resistance (high conductance) state Q_5 . To switch from Q_1 to Q_5 , we choose the pulse amplitude $V_A = 5.5$ V which satisfies the condition $V_A > [(Q_4 - x(t_{04})) = 5]$. To compute the appropriate pulse width Δw , we choose the final state (with input V_A) $x_{\Delta w}(t) = 26.5$ for a square pulse $v(t)$ by satisfying the condition $x_{\Delta w}(t) > Q_4$, as shown in Figure 6(a). For $x_{\Delta w}(t) \leq Q_4$, the proposed corsage memristor fails to switch from memory state Q_1 to Q_5 and converges to memory state Q_3 . However, pulse width Δw is equal to the time required for the trajectories to move from $x_1(t_{01})$ to $x_{\Delta w}(t)$ and can be computed by summing the time needed for each individual straight-line segment to reach the terminal points and express as

$$\Delta w = \Delta t_{f1} + \Delta t_{f2} + \Delta t_{f3} + \Delta t_{f4}. \quad (15)$$

The total time period t_f required to move from memory state Q_1 to Q_5 is expressed as

$$t_f = \Delta w + \Delta t_{f4wv} + \Delta t_{f5}, \quad (16)$$

as shown in Figure 6. The sequence of exponential $x(t)$ obtained from (11) is shown as follows:

$$x(t) = \begin{cases} x_1(t) = Q_1 + v(t) \left(1 - e^{-(t-t_{01})} \right) - (Q_1 - x_1(t_{01})) e^{-(t-t_{01})}, & t_{01} \leq t < t_{f1}, \\ x_2(t) = Q_2 - v(t) \left(1 - e^{-(t-t_{02})} \right) - (Q_2 - x_2(t_{02})) e^{-(t-t_{02})}, & t_{02} \leq t < t_{f2}, \\ x_3(t) = Q_3 + v(t) \left(1 - e^{-(t-t_{03})} \right) - (Q_3 - x_3(t_{03})) e^{-(t-t_{03})}, & t_{03} \leq t < t_{f3}, \\ x_4(t) = Q_4 - v(t) \left(1 - e^{-(t-t_{04})} \right) - (Q_4 - x_4(t_{04})) e^{-(t-t_{04})}, & t_{04} \leq t < t_{f4}, \\ x_{4wv}(t) = Q_4 - v(t) \left(1 - e^{-(t-t_{04wv})} \right) - (Q_4 - x_{4wv}(t_{04wv})) e^{-(t-t_{04wv})}, & t_{04wv} \leq t < t_{f4wv}, \\ x_5(t) = Q_5 + v(t) \left(1 - e^{-(t-t_{05})} \right) - (Q_5 - x_5(t_{05})) e^{-(t-t_{05})}, & t_{05} \leq t, \end{cases} \quad (17)$$

and by inserting the initial states, equilibrium points, and time period for the trajectories to move from

initial states to final states, the $x(t)$ can be expressed as follows:

$$x(t) = \begin{cases} x_1(t) = 3 + v(t) \left(1 - e^{-(t-t_{01})} \right), & (t_{01} = 0) \leq t < (t_{f1} = 0.778), \\ x_2(t) = 9 - v(t) \left(1 - e^{-(t-t_{02})} \right) - 3e^{-(t-t_{02})}, & (t_{02} = t_{f1} = 0.778) \leq t < (t_{f2} = 2.008), \\ x_3(t) = 15 + v(t) \left(1 - e^{-(t-t_{03})} \right) - 3e^{-(t-t_{03})}, & (t_{03} = t_{f2} = 2.008) \leq t < (t_{f3} = 4.841), \\ x_4(t) = 25 - v(t) \left(1 - e^{-(t-t_{04})} \right) - 5e^{-(t-t_{04})}, & (t_{04} = t_{f3} = 4.841) \leq t < (t_{f4} = 7.48), \\ x_{4wv}(t) = 25 - v(t) \left(1 - e^{-(t-t_{04wv})} \right) + 1.5e^{-(t-t_{04wv})}, & (t_{04wv} = t_{f4} = 7.48) \leq t < (t_{f4wv} = 8.684), \\ x_5(t) = 35 + v(t) \left(1 - e^{-(t-t_{05})} \right) - 5e^{-(t-t_{05})}, & (t_{05} = t_{f4wv} = 8.684) \leq t. \end{cases} \quad (18)$$

The memory state switching from Q_1 to Q_5 in Figure 6(a) shows that the applied square pulse with $V_A = 5.5$ V is equivalent to translating the red curve $f(x)$ upwards by 5.5 units, as shown by the blue curve. The dynamic route starting from Q_1 ($x = 3$), at $t = 0^-$, would jump abruptly from Q_1 on the red curve to a point directly above Q_1 on the blue curve (yellow circle) at $t = 0^+$ (shown with the upward green arrow) as the pulse input increases from 0 V to 5.5 V. Since the blue curve is located above the x -axis (where $dx/dt > 0$) over the range of interest, its motion can only move to the right, until time $t = \Delta w$. When the square pulse returns to zero at $t = \Delta w$, the point (shown with the green circle) on the blue curve reverts back abruptly to the point $x_{\Delta w}(t = \Delta w) = 26.5$ on the red curve (shown with the light cyan circle followed by the downward green arrowhead), whereupon the dynamics must continue to move along the dynamic route indicated by the black arrowheads, until it converges to the low-resistance memory state Q_5 ($x = 35$).

The exponential trajectories of the $x(t)$ related with the individual piecewise linear segments are shown in Figure 6(b). Observe from Figure 6(b) that the total time period (t_f) needed for the $x(t)$ trajectories to reach Q_5 from Q_1 is the summation of all the time periods needed for an individual trajectory to propagate through the piecewise linear segments which is $t_f = \Delta w + \Delta t_{f4wv} + \Delta t_{f5} = 17.2$ s.

To switch back from the low-resistance (high conductance) state Q_5 to the high-resistance (low conductance) state Q_1 of our corsage memristor, we simply applied a negative voltage pulse with amplitude $V_A = -5.5$ V and pulse width $\Delta w_b = 7.684$ s where Δw_b is computed using (15). The dynamic route and the state trajectories $x(t)$ of switching back kinetics from memory states Q_5 to Q_1 is shown in Figures 7(a) and 7(b), respectively. In Figure 7(a), at $t_b = \Delta w_b$, the state variable $x_{\Delta w_b}(t_b = \Delta w_b) = 8.9$ and the slope $dx/dt < 0$ at that linear segment for which the state variable $x(t)$ must move to the right and eventually converge

FIGURE 5: DC V - I plot of the 6-lobe corsage memristor over input voltage $-10 \text{ V} \leq V \leq 10 \text{ V}$. The left inset shows the conductance values at $V=0 \text{ V}$. The right inset shows the zoomed portion of the red DC V - I curve over the voltage range $-5 \text{ V} \leq V \leq 2 \text{ V}$.

to the equilibrium memory state Q_1 ($x=3$). The similar phenomenon with exponential trajectories of $x(t)$ is shown in Figure 7(b) where the $x(t)$ decreases as the time increases and converges to $x(t_{fb})=3$ where $x(t_{fb})=3$ is regarded as the Q_1 memory state. To switch back from Q_5 to Q_1 , the total time $t_{fb}=20.701 \text{ s}$ is needed as shown in Figure 7(b).

The pulse amplitude V_A and the pulse width Δw play a crucial role in the switching kinetics of the memory states of the 6-lobe Chua corsage memristor. An inappropriate pulse amplitude or pulse width may result in switching failures. To choose the appropriate pulse amplitude V_A , we already provided (14) whereas we illustrate the inappropriate pulse width scenario in Figure 8. In Figure 8, we provide the same pulse amplitude $V_A=5.5 \text{ V}$ to switch from memory state Q_1 to Q_5 with a different pulse width $\Delta w=7 \text{ s}$. Observe from Figure 8(b) that the exponential trajectories are converging to memory state Q_3 ($x=15$) rather than converging to memory state Q_5 ($x=35$). The reason behind such switching failure is the pulse width as at $t=\Delta w$ and the state variable $x_{\Delta w}(t=\Delta w)=23.812$ which lies in the left-hand side of Q_4 ($x=25$), as shown in Figure 8(a). According to Section 2.2, any point that lies in the left side of Q_4 ($x=25$) follows the dynamic route $dx/dt < 0$ (as shown with the black

arrowhead in Figure 2) and converges to equilibrium state Q_3 , and in this case, the state variable $x(t)$ follows the same route $dx/dt < 0$ and converges to Q_3 ($x=15$) as $x_{\Delta w}(t=\Delta w) < Q_4$.

For convenience of the readers, we plotted the hyperbolic relationship between the pulse amplitude V_A versus the pulse width Δw of the switching memory states between Q_1 and Q_5 of our 6-lobe corsage memristor as shown in Figure 9.

5. Physical Realization of the 6-Lobe Chua Corsage Memristor

For physical realization of the 6-lobe Chua corsage memristor, we modified the circuit in Figure 1(a) with the switching kinetics closer to the behavioral attributes of our 7-segment PWL hypothetical memristor which is shown in Figure 10. The novel circuit consists of the cascade between a passive nonlinear-resistive two-port and a dynamic first-order one-port [5]. The passive nonlinear-resistive two-port is composed of parallel connected Graetz bridges [12] with opposite diode directions whereas the dynamic first-order one-port is made up of a C - R parallel circuit.

FIGURE 6: Memory state switching kinetics of the 6-lobe Chua corsage memristor from memory state Q_1 to Q_5 for an input square pulse $V_A = 5.5$ V and $\Delta w = 7.48$ s. (a) Dynamic routes of the switching kinetics of the 6-lobe Chua corsage memristor. The two magenta-color vertical line segments indicate an instantaneous jump between the red and the blue piecewise-linear plots in the dynamic route map. (b) Movement of the exponential trajectories of $x(t)$ with respect to time t .

FIGURE 7: Switching kinetics from low-resistance state Q_5 to high-resistance state Q_1 for an input square pulse $V_A = -5.5$ V and $\Delta w_b = 7.684$ s. (a) Dynamic routes of the switching-back kinetics of the proposed cossage memristor. (b) Movement of the exponential trajectories of $x(t)$ with respect to time t .

FIGURE 8: Switching failures of the 6-lobe corsage memristor from Q_1 to Q_5 for a pulse amplitude $V_A = 5.5$ V and pulse width $\Delta w = 7$ s. (a) Dynamic routes of the switching kinetics and (b) movement of the exponential trajectories of $x(t)$ with respect to time t . The switching failure happens due to insufficient pulse width.

The *active and locally active* resistor R_0 in Figure 10 should exhibit the contiguous six breakpoints on its DC V - I curve similar to the 6-lobe Chua corsage memristor. To design the nonlinear resistor R_0 , we applied the circuit-theoretic analysis on an op-amp circuit [22] to obtain the desired DC V - I breakpoints at specific voltages. According to [22], the driving-point characteristic of a single positive and negative feedback op-amp circuit provides *two* breakpoints on its piecewise linear DC V - I curve. To obtain a *six*-breakpoint piecewise linear DC V - I curve, we combine three op-amp circuits in parallel as shown in Figure 11.

The current i coming out from the parallel op-amp circuit in Figure 11 provides a piecewise linear DC V - I curve with *six* breakpoints when plotted in the V - I plane.

The active and locally active two-port (marked with the black box) in Figure 11 consists of three op-amp circuits (marked with red, blue, and magenta boxes) in parallel. The circuit parameters and the components of the three op-amp circuit in Figure 11 are similar for each box except the negative feedback resistances (R_{41} , R_{42} , and R_{43}) which determine the effective saturation voltage E_{sat} of an individual op-amp circuit. The saturation voltage E_{sat} along with

FIGURE 9: Relationship between the pulse amplitude V_A and pulse width Δw for the switching kinetics of the 6-lobe cossage memristor.

the negative feedback resistance play a key role to achieve the V - I breakpoints at specified voltages such as $V = 3$ V, $V = 5$ V, and $V = 7$ V. The op-amp circuits in Figure 11 also contain a positive feedback path where the difficulty arises with the driving-point and transfer function. To resolve this problem, we replace the op-amp circuit in the red box (in Figure 11) by its three ideal models, such as the “Linear region,” “+Saturation region,” and “-Saturation region” as shown in Figures 12(a)–12(c), respectively.

The Linear region of the op-amp circuit in Figure 12(a) shows that the potential difference between the noninverting terminal (v_+) and the inverting terminal (v_-) is zero, so the differential voltage $v_d = (v_+ - v_-) = 0$ and eventually inverting terminal voltage,

$$v_- = v_+ = v_x = v. \quad (19)$$

The following relation between output voltage v_{03} and inverting terminal voltage v_- can be computed by the voltage divider rule

$$v_- = v_x = \left(\frac{R_{33}}{R_{33} + R_{43}} \right) v_{03} = \beta v_{03}, \quad (20)$$

where $\beta = R_{33}/(R_{33} + R_{43})$ and henceforth

$$v = \beta v_{03}. \quad (21)$$

Pedagogically, in the linear region, the relation between the saturation voltage ($\pm E_{\text{sat}}$) and output voltage v_{03} is as follows:

$$-E_{\text{sat}} < v_{03} < E_{\text{sat}}, \quad (22)$$

for which, in the Linear region, the relation between the input voltage v and saturation voltage ($\pm E_{\text{sat}}$) is

$$-\beta E_{\text{sat}} < v < \beta E_{\text{sat}}. \quad (23)$$

The loop

$$\textcircled{4} - \textcircled{3} - \textcircled{1} - \textcircled{4} \quad (24)$$

provides linear region current i_{lin} as

$$i_{\text{lin}} = \frac{1}{R_{73}} \left[v \left(1 + \frac{R_{73}}{R_{63}} \right) - v_{03} \right]. \quad (25)$$

For the +Saturation region shown in Figure 12(b), the relation between the output voltage v_{03} and the saturation voltage E_{sat} is as follows:

$$v_{03} = E_{\text{sat}}, \quad (26)$$

and the differential voltage $v_d > 0$, so that $(v_+ - v_-) > 0$, and eventually the relationship between input voltage and saturation voltage is

$$v \geq \beta E_{\text{sat}}. \quad (27)$$

The current for the +Saturation region $i_{+\text{sat}}$ is computed as follows:

$$i_{+\text{sat}} = \frac{1}{R_{73}} \left[v \left(1 + \frac{R_{73}}{R_{63}} \right) - E_{\text{sat}} \right]. \quad (28)$$

For the -Saturation region shown in Figure 12(c), the relation between the output voltage v_{03} and the saturation voltage E_{sat} is

$$v_{03} = -E_{\text{sat}}, \quad (29)$$

and $v_d < 0$, so that $(v_+ - v_-) < 0$, and henceforth, the relationship between the input voltage and saturation voltage is

$$v \leq -\beta E_{\text{sat}}, \quad (30)$$

and the -Saturation region current is computed as

$$i_{-\text{sat}} = \frac{1}{R_{73}} \left[v \left(1 + \frac{R_{73}}{R_{63}} \right) + E_{\text{sat}} \right]. \quad (31)$$

FIGURE 10: Circuit diagram of the real 6-lobe Chua corsage memristor emulator with quad-stable input dynamics.

The current i_3 flowing out of the op-amp circuit in Figure 11 is computed by adding all currents (i_{lin} , i_{+sat} , and i_{-sat}):

$$i_3 = \left\{ \underbrace{\left[\frac{1}{R_{73}} \left[v \left(1 + \frac{R_{73}}{R_{63}} \right) - v_{03} \right] \right]}_{\text{Linear region}} + \underbrace{\left[\frac{1}{R_{73}} \left[v \left(1 + \frac{R_{73}}{R_{63}} \right) - E_{sat} \right] \right]}_{\text{+Saturation region}} + \underbrace{\left[\frac{1}{R_{73}} \left[v \left(1 + \frac{R_{73}}{R_{63}} \right) + E_{sat} \right] \right]}_{\text{-Saturation region}} \right\} \quad (32)$$

Plotting the output voltage v_{03} and input current i_3 with respect to the input voltage v of the op-amp circuit with positive and negative feedback paths over the specified ranges of all the three regions provides a *piecewise linear* curve as shown in Figure 13(a). The op-amp circuit enclosed in the red box in Figure 11 exhibits *two* breakpoints at $V = \pm 7$ V with circuit parameters $R_{33} = 1$ K, $R_{43} = 1$ K, $R_{63} = 100$ K, $R_{73} = 1$ K, and $E_{sat} = 14$ V over the input voltage range -14 V $\leq V \leq 14$ V. The mathematical simulation results shown in Figure 13 shows that the linear region of the op-amp circuit lies in the range -7 V $\leq V \leq 7$ V (as $\beta E_{sat} = 7$ V) whereas the positive and negative saturation regions lie at $V > 7$ V and $V < -7$ V, respectively. Moreover, the output voltage v_{03} at the positive and negative saturation regions are $v_{03} = +E_{sat} = +14$ V and $v_{03} = -E_{sat} = -14$ V, respectively, and in the linear region, v_{03} increases proportionately to the input voltage v . However, the current i_3 of the op-amp circuit increases linearly in the saturation region and decreases in an inversely proportional manner to the input voltage v in the linear region.

Similarly, following the circuit-theoretic concepts mentioned above, the input currents i_2 and i_1 of the op-amp circuits in Figure 11 are computed as

$$i_2 = \left\{ \underbrace{\left[\frac{1}{R_{72}} \left[v \left(1 + \frac{R_{72}}{R_{62}} \right) - v_{02} \right] \right]}_{\text{Linear region}} + \underbrace{\left[\frac{1}{R_{72}} \left[v \left(1 + \frac{R_{72}}{R_{62}} \right) - E_{sat} \right] \right]}_{\text{+Saturation region}} + \underbrace{\left[\frac{1}{R_{72}} \left[v \left(1 + \frac{R_{72}}{R_{62}} \right) + E_{sat} \right] \right]}_{\text{-Saturation region}} \right\} \quad (33)$$

and

$$i_1 = \left\{ \underbrace{\left[\frac{1}{R_{71}} \left[v \left(1 + \frac{R_{71}}{R_{61}} \right) - v_{01} \right] \right]}_{\text{Linear region}} + \underbrace{\left[\frac{1}{R_{71}} \left[v \left(1 + \frac{R_{71}}{R_{61}} \right) - E_{sat} \right] \right]}_{\text{+Saturation region}} + \underbrace{\left[\frac{1}{R_{71}} \left[v \left(1 + \frac{R_{71}}{R_{61}} \right) + E_{sat} \right] \right]}_{\text{-Saturation region}} \right\} \quad (34)$$

The loci of v_{02} versus v and i_2 versus v and v_{01} versus v and i_1 versus v are shown in Figures 13(b) and 13(c), respectively.

The total current i flowing out of the 3 parallel connected op-amp circuits in Figure 11 is equal to the summation of the

FIGURE 11: Circuit diagram of nonlinear resistor R_0 of the real 6-lobe corsage memristor using off-the-shelf components.

three currents (i_1 , i_2 , and i_3) of the individual op-amp circuits and computed as

$$i = i_1 + i_2 + i_3. \quad (35)$$

The six-breakpoint V - I curve of nonlinear resistor R_0 is shown in Figure 14. Mathematical simulation results of

current i and the equivalent nonlinear resistance R_0 are shown in Figure 14(a) with the parameters (the measured resistor values of circuit implementation are used in mathematical and SPICE simulations) $R_{31} = R_{32} = R_{33} = 0.985\text{K}$, $R_{61} = R_{62} = R_{63} = 100.5\text{K}$, $R_{71} = R_{72} = R_{73} = 1.001\text{K}$, $R_{41} = 3.888\text{K}$, $R_{42} = 1.797\text{K}$, $R_{43} = 0.987\text{K}$, and $E_{\text{sat}} = 14\text{V}$. The plots of the current i and the active and locally active

FIGURE 12: Region-based ideal models of the op-amp circuit: (a) Linear region, (b) +Saturation region, and (c) -Saturation region.

resistance R_0 obtained by SPICE simulation and the actual circuit implementation are shown in Figures 14(b) and 14(c), respectively.

The mathematical simulation presented in Figure 14(a) shows that the V - I curve and the resistance value of the nonlinear resistor R_0 has *six* breakpoints at $V = \pm 6.99$ V, ± 4.95 V, and ± 2.82 V. The slope of R_0 is different between these breakpoints and hence defines different memory states. Similar to the mathematical model, the plots of the V - I curve and the nonlinear resistance R_0 obtained by SPICE simulation and the circuit implementation also have *six* breakpoints at $V = \pm 6.9$ V, ± 4.89 V, and ± 2.77 V and $V = \pm 5.74$ V, ± 4.05 V, and ± 2.15 V, respectively. The insets in Figures 14(a)–14(c) show the zoomed figure of R_0 near the origin and show that $R_0 = 0$ at input voltage $V = 0$ V.

The nonlinear resistance waveform obtained from the SPICE modelling in Figure 14(b) shows that the R_0 is

constant at resistance 147.47Ω for an input voltage range -2.77 V $< V < 2.77$ V, except for a tiny interval at the origin ($V = 0$ V). However, for 2.77 V $< V < 4.89$ V and 4.89 V $< V < 6.9$ V, the R_0 increases linearly from 147.47Ω to 216.07Ω and from 216.07Ω to 336.10Ω , respectively, whereas for $V > 6.9$ V, R_0 increases almost linearly. Due to the linear increment of R_0 with a constant slope over the above-mentioned voltage range, it can be acclaimed that the real 6-lobe corsage memristor emulator contains *four* different memory states, namely, R_{01} , R_{02} , R_{03} , and R_{04} where $R_{01} = (R_0 = 147.47 \Omega)$, $R_{02} = (147.47 \Omega < R_0 \leq 216.07 \Omega)$, $R_{03} = (216.07 \Omega < R_0 \leq 336.10 \Omega)$, and $R_{04} = (R_0 > 336.10 \Omega)$.

Similar to the SPICE model, the mathematical and the circuit implementation plots of R_0 also contains the *four* different memory states as shown in Figures 14(a) and 14(b), respectively. The fluctuation of R_0 at the -2.16 V $< V < 2.16$ V voltage range in Figure 14(c) is negligibly small and can be

FIGURE 13: Mathematical simulation of input currents (i_3 , i_2 , and i_1) and output voltages (v_{03} , v_{02} , v_{01}) with respect to input voltage v . Loci of (a) v_{03} versus v and i_3 versus v , (b) v_{02} versus v and i_2 versus v , and (c) v_{01} versus v and i_1 versus v of the individual op-amp circuits.

regarded as $R_0 = 137 \Omega$. The fluctuation was induced due to computational difficulties at $V = 0$ V in the oscilloscope. Although the resistance R_0 of the mathematical model of the 6-lobe cossage memristor and the real emulator are quantitatively different, they are also qualitatively identical.

The breakpoints of the V - I curve of the nonlinear resistor R_0 in mathematical simulation, shown in Figure 14(a) and the *SPICE* simulation shown in Figure 14(b), are slightly different. This deviation happens due to the nonideal circuit components of the *SPICE* module. Moreover, the V - I curve breakpoints of R_0 measured from the circuit implementation is further deviated from the mathematical and *SPICE* simulation. The reason behind such deviation is the nonideal characteristic of the op-amp circuit as well as the noise induced from the DC power supply and the oscilloscope probe. Another reason for such deviation is the used op-amp's rated saturation voltage ($E_{\text{sat}} = 13.7$ V) which is slightly less than the mathematical and *SPICE* saturation voltage $E_{\text{sat}} = 14$ V.

Although the breakpoints of the DC V - I curve in Figure 5 and the breakpoints of Figure 14 are quantitatively different, they are qualitatively similar. In this artifact, one of our

primary motives is to show that the basic method explained in [4, 5] and [14] can be used to convert the DC V - I curve of any real nonlinear resistor into a memristor. We prove this analogy by analyzing the parallel connected op-amp circuit in Figure 11 which has the capabilities to emulate the attributes of the 6-lobe Chua cossage memristor as it exhibits a 7-segment *PWL* DC V - I curve as shown in Figure 14.

The *SPICE* simulation of switching of memory states of the real 6-lobe Chua cossage memristor emulator (in Figure 10) is shown in Figure 15. Figure 15(a) shows the example of successful switching between the memory states R_{01} and R_{03} . To switch from R_{01} to R_{03} , a pulse input $V_A = 5.5$ V with a pulse width $\Delta w = 7.5$ s is applied across our real emulator circuit in Figure 10. Observe from Figure 15(a) that the resistance $R_0 = 147.47 \Omega$ at $t = 0^+$, and it gradually increases during the pulse period Δw and saturated at $R_0 = 216.5 \Omega$ and remained there although the input voltage become zero for $t \geq \Delta w$. The saturated resistance $R_0 = 216.5 \Omega$ lies over the memory state $R_{03} = (216.07 \Omega < R_0 \leq 336.10 \Omega)$ which confirms the successful switching from memory state R_{01} to R_{03} for an input pulse $V_A = 5.5$ V

FIGURE 14: DC current I versus DC voltage V and DC resistance $R_0 = (V/I)$ derived and measured from the 6-lobe corsage memristor emulator. (a) I versus V and R_0 versus V plot of mathematical model, (b) I versus V and R_0 versus V plot of spice circuit simulation, and (c) I versus V and R_0 versus V plot of the actual circuit implementation.

FIGURE 15: Switching kinetics of the memory states of real 6-lobe Chua corsage memristor emulator. (a) Successful switching: the corsage memristor emulator switches from memory state R_{01} to R_{03} with a resultant resistance $R_0 = 216.5 \Omega$ for an input pulse $V_A = 5.5 \text{ V}$ and pulse width $\Delta w = 7.5 \text{ s}$. (b) Switching failure: the proposed corsage memristor emulator fails to switch from R_{01} to R_{03} for an input pulse $V_A = 5.5 \text{ V}$ and pulse width $\Delta w = 7 \text{ s}$ as the resultant resistance $R_0 = 215.6 \Omega$ lies in the memory state range R_{02} .

and $\Delta w = 7.5 \text{ s}$. However, to fit the resistance scale, we truncated the $t \leq 0$ part of the R_0 in Figure 15(a) as that part is insignificant because at $t = 0^+$, R_0 immediately rises from $R_0 = 0 \Omega$ to $R_0 = 147.47 \Omega$.

In this paper, we also demonstrate the switching failure scenario of the real 6-lobe Chua corsage memristor as shown in Figure 15(b). In Figure 15(b), a pulse input $V_A = 5.5 \text{ V}$ with a pulse width $\Delta w = 7 \text{ s}$ is applied across our real emulator. The nonlinear resistance R_0 is saturated at $R_0 = 215.6 \Omega$ and remained there as the time increases although the voltage becomes $v(t) = 0$ for $t \geq \Delta w$. The resultant resistance $R_0 = 215.6 \Omega$ lies over the memory state $R_{02} = (147.47 \Omega < R_0 \leq 216.07 \Omega)$ which confirms the failure of switching as our intention is to switch from memory state R_{01} to R_{03} for an input pulse $V_A = 5.5 \text{ V}$ and $\Delta w = 7 \text{ s}$, but we converge on memory state R_{02} .

The switching failure scenario gives us the insights that the emulator circuit of our proposed corsage memristor is also dependent on the appropriate pulse amplitude and the pulse width like its mathematical model. To illustrate the relationship of pulse amplitude and the pulse width in our real emulator circuit, we plot the *pulse amplitude V_A versus pulse width $|\Delta w|$* curve as shown in Figure 16. The hyperbolic relationship in Figure 16 shows that the maximum pulse amplitude V_A requires less pulse width Δw to switch from one memory state to another state whereas the minimum pulse amplitude requires maximum pulse width.

6. Conclusion

The recent interest in inherently nonlinear memristor devices is bringing to a new life to the theory of nonlinear

circuits and systems. In this paper, we design and build a highly nonlinear novel device, namely, the 6-lobe Chua corsage memristor, and its real emulator circuit using the nonlinear circuit theory. The proposed generic memristor can be used as a multistate, specifically 4-state, memory device with an increased efficiency of 50% compared to the 2-lobe and bistable extended memristor whereas the efficiency of the proposed memristor increased by 25% compared to the 4-lobe corsage memristor. Moreover, due to the presence of more equilibrium points compared to the 2-lobe or 4-lobe corsage memristors, the proposed corsage memristor exhibits a higher variety of dynamic routes in response to different initial conditions $x(0)$ which enhance the capability to represent a desired function more closely than 2-lobe or 4-lobe corsage memristors. Due to the diversified dynamic routes and the enhancement in stable memory states, the proposed corsage memristor is more versatile and effective than its predecessor 2-lobe and 4-lobe corsage memristors. Moreover, the diversified dynamic routes reveal a contiguous highly nonlinear DC V - I curve with *six* distinct *contiguous* hysteresis lobes, unlike the most published highly nonlinear disconnected DC V - I curves. Furthermore, the *universal formulas*, derived in Section 4, ease the demonstration of the switching kinetics of the 6-lobe corsage memristor and assist to switch the memory states precisely with an appropriate pulse amplitude and pulse width in accordance to an initial condition $x(0)$. The universal formulas are applicable to any device which exhibits a PWL dynamic route map with any *number of segments* for any *DC or pulse input*. Following the introduction of a purely mathematical memristor model with quad stability (2-bit memory system) at DC and pulse input, this paper elucidates the mechanisms behind the

FIGURE 16: Relation between amplitude V_A versus pulse width Δw of the real 6-lobe Chua corsage memristor emulator.

emergence of the first real emulated 6-lobe Chua corsage memristor using *off-the-shelf* elements. Nonlinear system theoretic concepts were applied to the model of the two-port memristive element to gain a deep insight into the quad-stable characteristic of its dynamics where the quantitative attributes of the real emulator might not be similar to the mathematical model but they are qualitatively same.

Data Availability

The data used to support the findings of this study are available from the first author or corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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Supplementary Materials

Finding of universal formulas. Figure 1: dynamic routes of the switching kinetics of the 6-lobe Chua corsage memristor. The two magenta-color vertical line segments indicate an instantaneous jump between the red and the blue piecewise-linear plots in the dynamic route map. Figure 2: movement of the exponential trajectories of $x(t)$ with respect to time t . (*Supplementary Materials*)

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