

Research Article

A Novel Memductor-Based Chaotic System and Its Applications in Circuit Design and Experimental Validation

Li Xiong ^{1,2,3}, Yanjun Lu ¹, Yongfang Zhang ⁴, and Xinguo Zhang⁵

¹School of Mechanical and Precision Instrument Engineering, Xi'an University of Technology, Xi'an 710048, China

²School of Physics and Electromechanical Engineering, Hexi University, Zhangye 734000, China

³State Key Laboratory of ASIC & System, Fudan University, Shanghai 200433, China

⁴School of Printing, Packaging Engineering and Digital Media Technology, Xi'an University of Technology, Xi'an 710048, China

⁵School of Information Science and Engineering, Lanzhou University, Lanzhou 730000, China

Correspondence should be addressed to Yanjun Lu; yanjunlu@xaut.edu.cn

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This paper is expected to introduce a novel memductor-based chaotic system. The local dynamical entities, such as the basic dynamical behavior, the divergence, the stability of equilibrium set, and the Lyapunov exponent, are all investigated analytically and numerically to reveal the dynamic characteristics of the new memductor-based chaotic system as the system parameters and the initial state of memristor change. Subsequently, an active control method is derived to study the synchronous stability of the novel memductor-based chaotic system through making the synchronization error system asymptotically stable at the origin. Further to these, a memductor-based chaotic circuit is designed, realized, and applied to construct a new memductor-based secure communication circuit by employing the basic electronic components and memristor. Furthermore, the design principle of the memductor-based chaotic circuit is thoroughly analyzed and the concept of “the memductor-based chaotic circuit defect quantification index” is proposed for the first time to verify whether the chaotic output is consistent with the mathematical model. A good qualitative agreement is shown between the simulations and the experimental validation results.

1. Introduction

With the deep study of the chaotic systems and chaotic circuits, the concept of memristor was first put forwarded by Chua in 1971 [1]. Memristor is the fourth circuit component after capacitor, resistor, and inductor were coined, which is actually a nonlinear resistor with natural memory function. Nevertheless, we did not see significant progress on relevant research at that time on account of insufficient attention was paid to the memristor. The immature nanomanufacturing technology and difficult manufacturing of memristor with real materials all contributed to the slow progress on memristor [2]. It was not until 2008 that the HP Laboratories confirmed the existence of memristor and simultaneously a memristor-based real device was coined with its results published in *Nature* [3, 4]. Since then, memristor has become a hot research spot of chaos and it drew much more eyes from researchers engaged in various areas of

science and engineering [5–10]. It is well known that memristor has two models, namely, charge control and chain control. Among them, charge control exports memristor, while chain control exports memductor. If the memristor is a constant, it becomes the same concept as resistor. Correspondingly, the physical meaning of memductor is equivalent to conductance. Because the design of memductor is more convenient than the design of memristor in the design of chaotic circuits, the model of memductor is studied in this paper.

As a tunable nonlinear device with small size and low power consumption, memristor is quite suitable for the applications of high-frequency chaotic circuit, image encryption, and chaotic secure communication. It is no wonder that, in recent years, utilizing memristor to construct chaotic circuits has attracted close attention of quite a number of researchers [11–15]. Among them, Itoh and Chua adopted the memristor with a characteristic curve for the monotone

rise and piecewise linear to replace the diode in Chua's circuit and followed by the chaotic oscillation circuit based on memristor was derived [6]. Similarly, Muthuswamy and Kokate replaced the memristor with piecewise linear model instead of Chua's diode and analyzed the dynamic characteristics of the system after replacement. The results indicated that the chaotic characteristics of the system were more complex than that of the classical Chua's [7]. In 2010, Muthuswamy and Chua proposed the most simple third-order memristor chaotic circuit so far and in [8, 9] showed the experimental results of the corresponding hardware circuit, whose greatest feature was the simple structure. It was connected in series simply by a linear inductor, a linear capacitor, and a nonlinear memristor. In addition, Bao et al. carried on the research on the memristor chaotic circuit and realized a series of new Chua's memristor chaotic circuits by using the smooth model magnetic controlled memristor [10–12]. At present, the proposed memristor chaotic oscillation circuits of different structure and types [13–23] include the chaotic circuits with two memristors [16], integer-order memristor chaotic circuit [18], fractional-order memristor chaotic circuit [19], and memristor-based circuit for neural networks [23], whereas most of the researchers focus on theoretical analysis and numerical simulation for the memristive chaotic system and the experimental validation of the hardware circuit is rarely seen because those memristive chaotic circuits are theoretically established and their feasibility to be implemented by using hardware circuit is still not known. In particular, it is more difficult to design and implement a practical circuit for certain more complicated memductor chaotic systems. Therefore, we construct a novel memductor-based chaotic circuit and implement the experimental validation of the hardware circuit for above reason.

Moreover, in order to meet the security requirements of chaotic secure communication, researchers proposed a method to improve the predictability and complexity of the system by constructing hyperchaotic systems [24–26] and memristor-based chaotic systems, since memristor is a nonlinear component, whose memory ability [27–31] of the current by convection is not available in conventional chaotic circuit elements. In this way, it is especially suitable for the chaotic secure communication field [32–36]. Although the application research of memristor is just the beginning in the field of chaotic secure communication, it has great potentials and advantages in improving the confidentiality and security of chaotic secure communication system. So far, there is no literature to implement the memductor-based chaotic secure communication in chaotic modulation way. In this paper, chaotic modulation is adopted to implement the memductor-based secure communication based on the novel memductor-based chaotic circuit.

The contribution of this paper is that a new method for constructing ordinary chaotic system into memductor-based chaotic system is proposed by using memristor as nonlinear term. Then, we perform a detailed analysis, active control, synchronous stability analysis [37–40], and secure communication of the novel memductor-based chaotic system. The active control is implemented, and the synchronization stability results are determined by using Lyapunov

stability theory. The corresponding physical circuit implementation is also proposed to show the accuracy and efficiency of the memductor-based chaotic circuit. The analog circuit implementation results match with the Multisim and MATLAB simulation results. In addition, the concept of “the memductor-based chaotic circuit defect quantification index” is first proposed to verify whether the chaotic output is consistent with the mathematical model through deep analysis on the design principle of memductor-based chaotic circuit. Our research provides important theoretical and technical basis for the realization of the large-scale integrated circuit with memductor. This paper is expected to serve as a further step to apply memductor into real-world secure communication.

This paper falls into 6 parts. In Section 2, a novel 4D memductor-based chaotic system is constructed. In following Section 3, several qualitative issues about the novel memductor-based chaotic system, such as the basic dynamical behavior, divergence, stability of the equilibrium set, bifurcation, Poincaré map, and synchronous stability, are investigated analytically and numerically. In Section 4, the proposed memductor-based chaotic circuit is implemented in an analog electronic circuit. After that, a new memductor-based chaotic secure communication circuit is proposed based on the novel memductor-based chaotic circuit in Section 5. Finally, some conclusions and discussions are drawn in Section 6.

2. The Construction of a Novel Memductor-Based Chaotic System

2.1. A Specific Memductor Model. Apart from the three basic circuit components, including capacitor, resistor, and inductor, the fourth circuit component is memristor, which derives from the magnetic flux and charge in the circuit. And the resistance value of the memristor varies with the current flowing through the circuit. When the circuit is powered down, the resistance value of the memristor still remains valid before the power is broken. Therefore, memristor is actually a nonlinear resistor with natural memory function.

The memristor is defined as the relation between the magnetic flux and the charge quantity, that is,

$$d\phi = mdq. \quad (1)$$

Memristor can be divided into accumulation charge memristor and magnetic flux-controlled memristor. For a charge-controlled memristor, ϕ is easily obtained by

$$\phi = f(q). \quad (2)$$

For (2), differentiation can be easily obtained as follows:

$$\frac{d\phi}{dt} = \frac{df(q)}{dq} \frac{dq}{dt}. \quad (3)$$

Thus, $v(t)$ can be obtained as follows:

$$v(t) = \frac{df(q)}{dq} i(t). \quad (4)$$

According to Ohm's law, $v(t)$ is obtained as follows:

$$v(t) = m(q)i(t). \quad (5)$$

Thus, a memristance value is obtained as follows:

$$m(q) = \frac{df(q)}{dq}, \quad (6)$$

where $m(q)$ is the memristance, and its unit is Ohm (Ω). If the memristance value is a constant, then it becomes the same concept as resistance. It can also be obtained by a linear relationship between the current and the voltage.

For the magnetic flux-controlled memristor, q is easily obtained by

$$q = f(\phi). \quad (7)$$

From $i = dq/dt$, we can get

$$i(t) = w(\phi)v(t), \quad (8)$$

where $w(\phi)$ is the memductance. In the chaotic circuits, the use of memductor is more extensive. This is because the design of memductor in chaotic circuits is more convenient than memristor design.

Here, a magnetically controlled memristor is defined with a smooth cubic monotonic rise nonlinear characteristic curve. The model is a nonlinear memductor, and the nonlinearity is modeled by using a cubic curve model. The formula is described as follows:

$$q(\phi) = a\phi + b\phi^3. \quad (9)$$

Act on the equation ends of the sign with d/dt , that is,

$$\begin{aligned} \frac{dq(\phi)}{dt} &= \frac{d}{dt}(a\phi + b\phi^3) = \frac{d}{d\phi}(a\phi + b\phi^3) \frac{d\phi}{dt} \\ &= (a + 3b\phi^2) \frac{d\phi}{dt}. \end{aligned} \quad (10)$$

In consideration of $dq = idt$, $d\phi = udt$, and $\phi = \int udt$, we can obtain

$$i = (a + 3b\phi^2)u \quad (11)$$

and

$$i = au + 3bu \left(\int udt \right)^2. \quad (12)$$

Equation (11) is the VAR (volt ampere relation) expression of the memductor. It makes the physical concept of

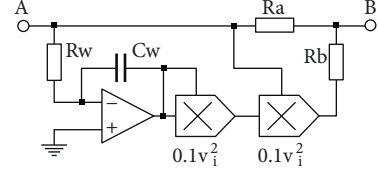


FIGURE 1: The alternative circuit of memristor.

memductor more distinct; thus, we can clearly see that the dimension of $(a + 3b\phi^2)$ is conductance. Equation (12) seems useless, but it is very important for engineering design. The specific circuit of memristor can be directly designed by (12). Even when the model represented by (10) changes, we can also design corresponding memductor-based or memristor-based circuits according to this method.

2.2. Realization Circuit of the Specific Memductor Element.

According to (12), the specific circuit of memristor can be designed directly. An equivalent memductor-based circuit consisting of operational amplifier, analog multiplier, resistor, and capacitor is shown in Figure 1.

Here, we assume that the B terminal is connected to the inverting input of the next-stage operational amplifier, so the B point has dummy ground and zero level. The A point is the voltage input, and it is set as u_A . The multiplier coefficient of analog multiplier is 0.1, and the relation between input and output voltage is described as $u_o = 0.1 u_i^2$. It is assumed that the normalized resistance is $10 \text{ k}\Omega$. Then, the output voltage of the operational amplifier is $-(300/R_w C_w) \int u_A dt$. And the output voltage of the operational amplifier after normalization is $-300 \int u_A dt$. After the first analog multiplication, the voltage is $30(\int u_A dt)^2$. After the second analog multiplication, the voltage is $3u_A (\int u_A dt)^2$. Therefore, the current flowing through R_b is easily obtained as follows:

$$i_{R_b} = \frac{3u_A (\int u_A dt)^2}{R_b}. \quad (13)$$

Thus, the current flowing through B point is obtained as follows:

$$i_B = \frac{u_A}{R_a} + \frac{3u_A (\int u_A dt)^2}{R_b}. \quad (14)$$

In the following, the circuit parameter design is carried out.

$$\begin{aligned} R_w &= 33.3 \Omega, \\ R_a &= \frac{10 \text{ k}\Omega}{a}, \\ R_b &= \frac{10 \text{ k}\Omega}{b}. \end{aligned} \quad (15)$$

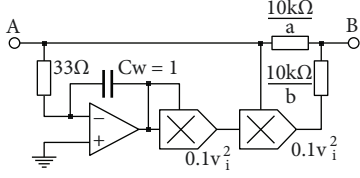


FIGURE 2: The alternative circuit of memductor based with specific parameters.

Then, the total current flowing through B is obtained as follows:

$$i_B = au_A + 3bu_A \left(\int u_A dt \right)^2. \quad (16)$$

In this way, the circuit structure and circuit parameter design of the memductance are realized. The equivalent memductor-based circuit with specific parameters is shown in Figure 2.

2.3. A Novel 4D Memductor-Based Chaotic System. The 3D chaotic system is described as follows:

$$\begin{cases} \dot{x} = \alpha(y - h(x)), \\ \dot{y} = x - y + z, \\ \dot{z} = -\beta y, \end{cases} \quad (17)$$

where

$$h(x) = m_1 x + m_2 f(x) = m_1 x + m_2 \left(\frac{1}{2} (|x+1| - |x-1|) \right), \quad (18)$$

and where x, y, z are the state variables and α, β, m_1, m_2 are the constant parameters of the 3D system. Here, replace $h(x)$ with the memductance $w(x)$; thus, a mathematical model of a chaotic circuit consisting of a memductor element is obtained as follows:

$$\begin{cases} \dot{x} = \alpha(y - w(x)), \\ \dot{y} = x - y + z, \\ \dot{z} = -\beta y, \end{cases} \quad (19)$$

where

$$w(x) = ax + 3bx \left(\int x dt \right)^2. \quad (20)$$

Therefore, according to the characteristics of the aforementioned specific memductor element and the specific realization circuit with memductor, a novel 4D memductor-based chaotic system is proposed based on the ordinary 3D

chaotic system (17). And the novel 4D memductor-based chaotic system is presented as follows:

$$\begin{cases} \dot{x} = \alpha(y + \xi x - cu - dxu^2), \\ \dot{y} = x - y + z, \\ \dot{z} = -\beta y - \gamma z, \\ \dot{u} = x, \end{cases} \quad (21)$$

where x, y, z, u are the state variables and $\alpha, \beta, \xi, \gamma, c, d$ are constant, positive parameters of the novel memductor-based chaotic system.

When choosing $\alpha = 16$, $\beta = 15$, $\xi = 0.25$, $c = 0.00625$, $d = 0.125$, and $\gamma = 0.5$, there exist typical chaotic attractors in system (21). That is, after adding 1D memristor to the ordinary 3D chaotic system, we need to find the appropriate parameters to satisfy the memductor-based system to produce new chaotic phenomena. For the constructed novel memductor-based chaotic system, four parameters ξ, γ, c, d are added. When the specific parameters are brought in, the equation becomes

$$\begin{cases} \dot{x} = 16(y + 0.25x - 0.00625u - 0.125xu^2), \\ \dot{y} = x - y + z, \\ \dot{z} = -15y - 0.5z, \\ \dot{u} = x. \end{cases} \quad (22)$$

However, the numerical solutions of the proposed 4D memductor-based chaotic system (22) are not able to be implemented by using general circuit components. Therefore, in practical applications, it often needs to be varied to make proper adjustments of these variables. Here, the method of scale transformation is to replace x, y, z , and u by $4x, 0.5y, 3z$, and u , respectively. After scale transformation, (22) becomes

$$\begin{cases} \dot{x} = 4x + 2y + 0.025u - 2xu^2, \\ \dot{y} = 8x - y + 6z, \\ \dot{z} = -2.5y - 0.5z, \\ \dot{u} = -4x. \end{cases} \quad (23)$$

Thus, the novel 4D memductor-based chaotic system after scale transformation is easily described as follows:

$$\begin{cases} \dot{x} = \xi x + \alpha y + cu - dxu^2, \\ \dot{y} = \eta x - y + \mu z, \\ \dot{z} = -\beta y - \gamma z, \\ \dot{u} = -\rho x, \end{cases} \quad (24)$$

where x, y, z, u are the state variables and $\alpha, \beta, \xi, \gamma, c, d, \eta, \mu, \rho$ are constant, positive parameters of the novel 4D memductor-based chaotic system. When choosing $\xi = 4$,

$\alpha = 2$, $c = 0.025$, $d = 2$, $\eta = 8$, $\mu = 6$, $\beta = 2.5$, $\gamma = 0.5$, and $\rho = 4$, there exist typical chaotic attractors in system (24).

3. Dynamical Analysis of the Novel Memductor-Based Chaotic System

3.1. Chaotic Attractors. The chaotic attractors with MATLAB simulation of the novel 4D memductor-based chaotic system (24) are shown in Figure 3. It can be seen from the numerical simulation results that the numerical range of each variable parameter is within -10 V to $+10\text{ V}$, and it fully conforms to the requirements of circuit design in practical applications. That is because the working voltage of electronic components generally ranges from -15 V to $+15\text{ V}$ in practical electronic circuits. As a result, it must be the equation of scaling if the memductor-based chaotic circuit is to be implemented.

3.2. Divergence and Stability of Equilibrium Set. The divergence of the novel 4D memductor-based chaotic system (24) is easily calculated as follows:

$$\nabla = \frac{\partial \dot{x}}{\partial x} + \frac{\partial \dot{y}}{\partial y} + \frac{\partial \dot{z}}{\partial z} + \frac{\partial \dot{u}}{\partial u} = \xi - du^2 - 1 - \gamma = 2.5 - 2u^2. \quad (25)$$

In this way, the system will be dissipative on the condition that the parameter becomes $|u| > \sqrt{5}/2$, because a necessary and sufficient condition for system (24) to be dissipative is that the divergence of the vector field is negative when the time tends to infinite. Furthermore, the corresponding dynamic characteristics will be presented.

Considering $\dot{x} = \dot{y} = \dot{z} = \dot{u} = 0$, then the equilibrium equation of system (24) is easily obtained as follows:

$$\begin{cases} \dot{x} = \xi x + \alpha y + cu - dxu^2 = 0, \\ \dot{y} = \eta x - y + \mu z = 0, \\ \dot{z} = -\beta y - \gamma z = 0, \\ \dot{u} = -\rho x = 0. \end{cases} \quad (26)$$

Clearly, the set of equilibrium points of the system (24) is obtained as follows:

$$E = \{(x, y, z, u) \mid x = y = z = 0, u = \sigma\}, \quad (27)$$

where σ is any real constant. That is, the set of points on the u coordinate is the equilibrium point and the system has an infinite set of equilibrium points. Through linearizing the system (24) near the equilibrium point, then the Jacobian matrix for system (24) at equilibrium point (27) is obtained as follows:

$$J_E = \begin{bmatrix} \xi - d\sigma^2 & \alpha & 0 & 0 \\ \eta & -1 & \mu & 0 \\ 0 & -\beta & -\gamma & 0 \\ -\rho & 0 & 0 & 0 \end{bmatrix}, \quad (28)$$

where $\xi = 4$, $\alpha = 2$, $d = 2$, $\eta = 8$, $\mu = 6$, $\beta = 2.5$, $\gamma = 0.5$, and $\rho = 4$. Then, the specific Jacobian matrix for system (24) at equilibrium point is easily obtained as follows:

$$J_E = \begin{bmatrix} 4 - 2\sigma^2 & 2 & 0 & 0 \\ 8 & -1 & 6 & 0 \\ 0 & -2.5 & -0.5 & 0 \\ -4 & 0 & 0 & 0 \end{bmatrix}. \quad (29)$$

The characteristic polynomial of the Jacobian matrix (29) is described as follows:

$$\text{Det}(J_E - \lambda I) = 0. \quad (30)$$

Therefore, the eigenvalues at the equilibrium point of the novel memductor-based chaotic system can be obtained as follows:

$$\begin{aligned} \lambda_1 &= 5.7332, \\ \lambda_{2,3} &= -1.6276 \pm 3.0918i, \\ \lambda_4 &= 0.0221, \\ |\sigma| &> 1.118. \end{aligned} \quad (31)$$

It can be concluded from (31) that the equilibrium point set of the system, which accords with the condition of chaos generation, is unstable.

3.3. Bifurcation, Lyapunov Exponents, and Poincaré Graph. The calculation of Lyapunov exponent is a method employed to quantitatively judge the chaos of system. When choosing $\xi = 4$, $\alpha = 2$, $c = 0.025$, $d = 2$, $\eta = 8$, $\mu = 6$, $\beta = 2.5$, $\gamma = 0.5$, and $\rho = 4$, the initial conditions are chosen as $x(0) = -0.17528$, $y(0) = -1.0872$, $z(0) = 1.6368$, and $u(0) = -3.2852$. The Lyapunov exponents of the novel memductor-based chaotic system are, respectively, calculated as follows: $L_1 = 0.0600$, $L_2 = 0.0065$, $L_3 = -0.0069$, and $L_4 = -10.4012$. Figure 4 shows the projection of a chaotic attractor generated by the novel memductor-based chaotic system on the $x - u$ plane. It represents the extreme sensitivity of the memristor-based chaotic system to the initial values [30]. When the initial value varies by 0.00001, there will be such a prominent difference in the result. It is obvious that the proposed memductor-based chaotic system is extremely sensitive to initial values. In Figure 5, the Lyapunov exponent spectrum of the novel memductor-based chaotic system is shown. Consequently, it is found that the novel memductor-based chaotic system is chaotic oscillation from the chaotic attractors and Lyapunov exponents.

In order to further verify the chaotic dynamical behavior of the novel memductor-based chaotic system (24), the bifurcation diagram and the Poincaré graph are strictly calculated. Through numerical analysis, the bifurcation diagram with parameter variation is shown in Figure 6, where α is a variable parameter. It is obvious that the system will undergo a huge change in topology when α is about 1.1. The Poincaré

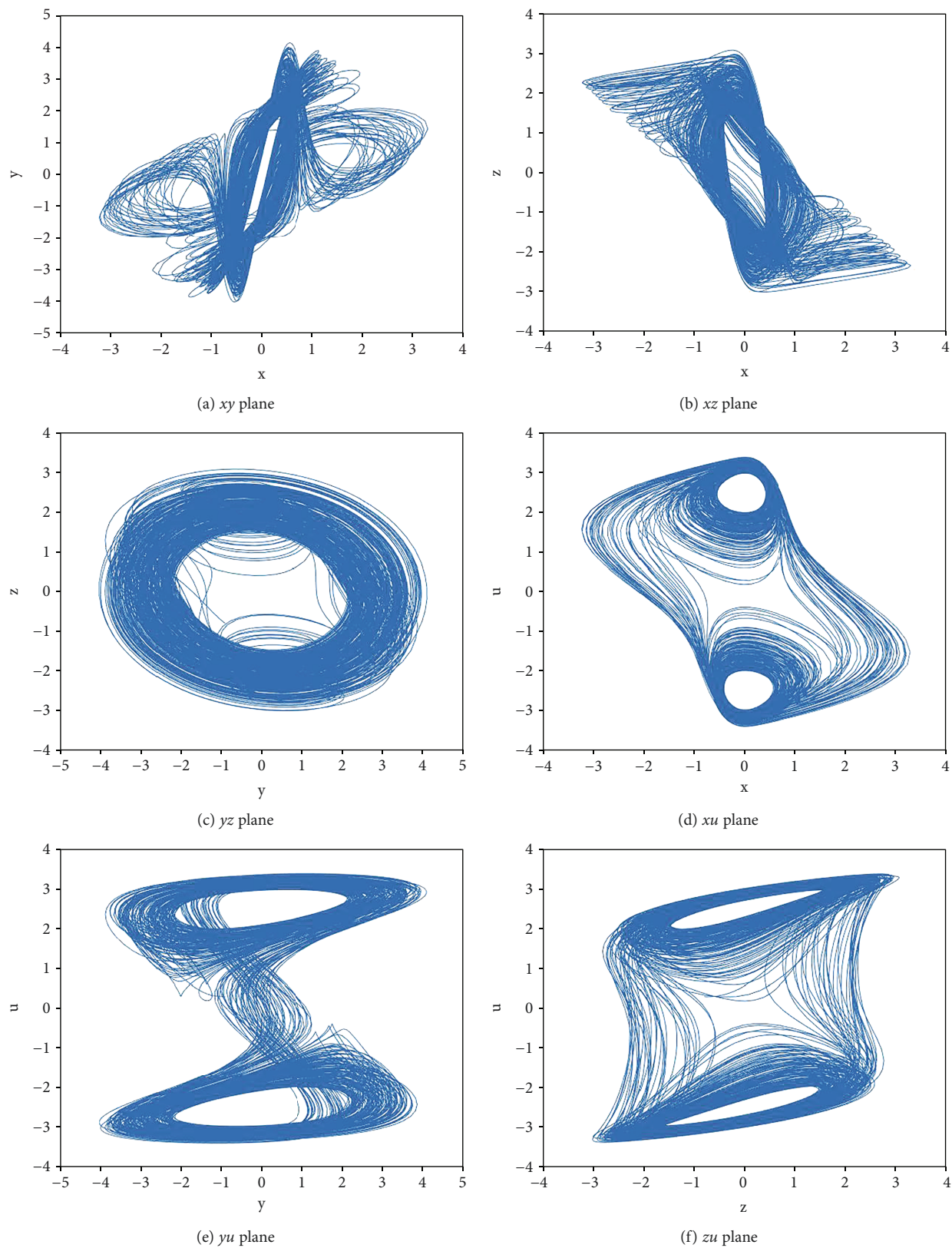


FIGURE 3: The chaotic attractors of system (24) with MATLAB.

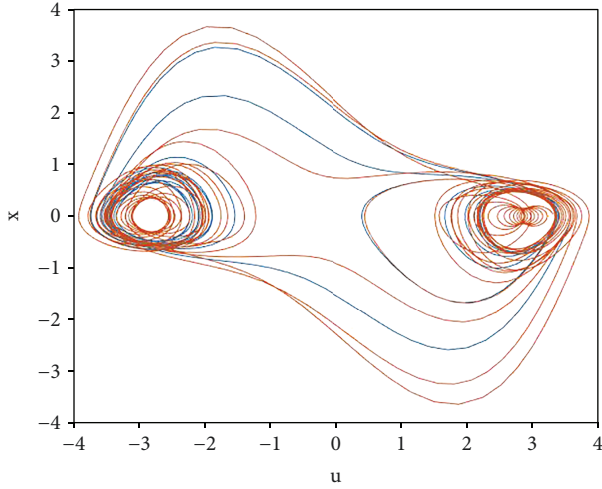
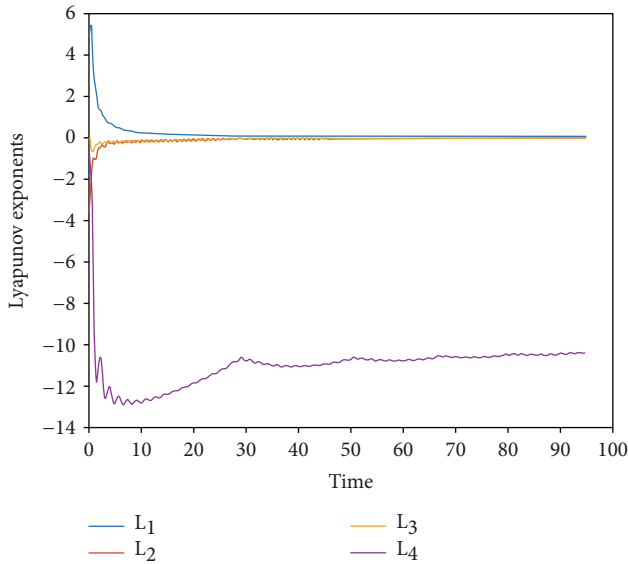
FIGURE 4: The chaotic attractor of ux plane.

FIGURE 5: The Lyapunov exponent spectrum.

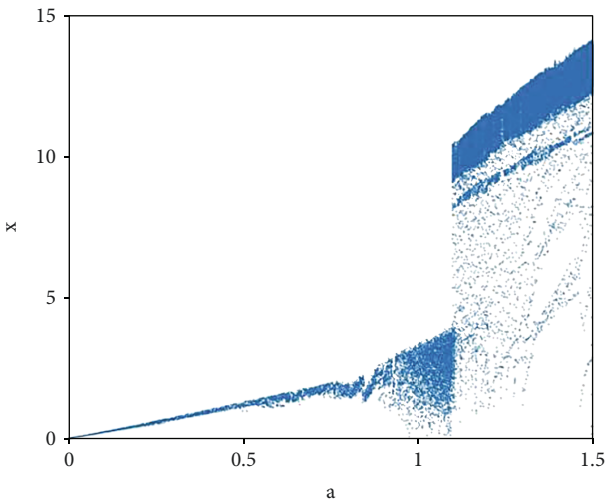


FIGURE 6: The bifurcation diagram.

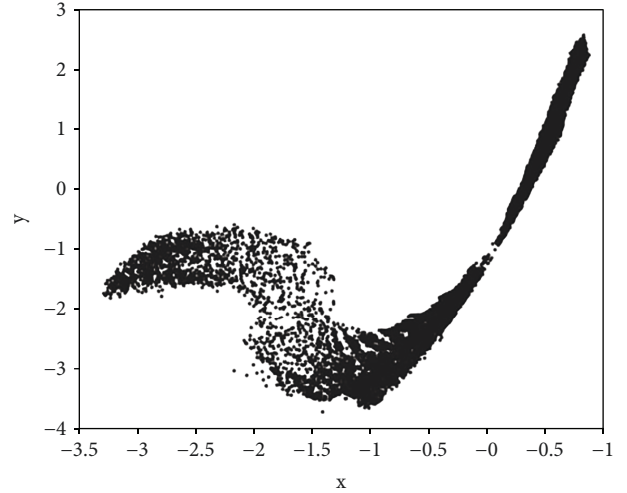


FIGURE 7: The Poincaré graph.

graph in $x - y$ plane is shown in Figure 7. The law of phase trajectory can be obtained by Poincaré map. It confirms the chaotic behavior of the proposed memductor-based chaotic system for the aforementioned set of parameters.

3.4. Synchronous Stability Analysis Based on Active Control. Chaotic synchronization means that the trajectory of a chaotic system converges to another chaotic system and maintains a consistent dynamic phenomenon from a physical standpoint [38]. Here, the chaotic drive system or the transmitter in the secure communication system is defined as follows:

$$\dot{X} = M(X, t). \quad (32)$$

Then, the chaotic response system or the receiver in the secure communication system is defined as follows:

$$\dot{Y} = M'(Y, t) + N, \quad (33)$$

where N is the controller, t is the time, and vectors are $X, Y \in \mathbb{R}^n$. And they have the n -dimensional elements (x_1, x_2, \dots, x_n) and (y_1, y_2, \dots, y_n) , respectively. In addition, the two chaotic systems can be the same or different, but their initial conditions are different. If the two chaotic systems are interrelated to some extent through the controller N , $X(t; t_0, X_0)$ and $Y(t; t_0, Y_0)$ are considered to be the solutions of system (32) and system (33), respectively, where they satisfy the smooth condition of the function, when \mathbb{R}^n has a subset of $W(t_0)$, and the initial value is satisfied to $X_0, Y_0 \in D(t_0)$, and then when $t \rightarrow \infty$ exists:

$$\zeta \equiv \lim_{t \rightarrow \infty} \|X(t; t_0, X_0) - Y(t; t_0, Y_0)\| \rightarrow 0. \quad (34)$$

Thus, it can be obtained that the chaotic response system (32) is synchronized with the chaotic drive system (33).

In this way, the active synchronization error system between the chaotic drive system and the chaotic response system is defined by $\dot{e} = \dot{y} - \dot{x}$, which means the asymptotic

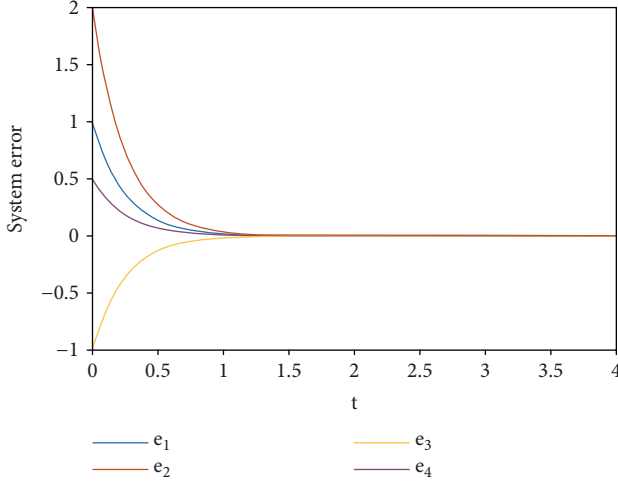


FIGURE 8: The history of synchronization errors.

stability at the origin of the synchronization error system on the basis of the Lyapunov stability theory. It is obvious that the controller N plays a key role in stabilizing the synchronization error system at the origin. Consequently, various synchronization methods will be realized by designing different controllers.

Then, the novel 4D memductor-based system (24) is rewritten. And we consider the novel memductor-based drive system which is described as follows:

$$\begin{cases} \dot{x}_1 = \xi x_1 + \alpha x_2 + cx_4 - dx_1 x_4^2, \\ \dot{x}_2 = \eta x_1 - x_2 + \mu x_3, \\ \dot{x}_3 = -\beta x_2 - \gamma x_3, \\ \dot{x}_4 = -\rho x_1. \end{cases} \quad (35)$$

When choosing $\xi = 4$, $\alpha = 2$, $c = 0.025$, $d = 2$, $\eta = 8$, $\mu = 6$, $\beta = 2.5$, $\gamma = 0.5$, and $\rho = 4$, the novel memductor-based system (35) is chaotic. Thereafter, the novel memductor-based response system is considered as follows:

$$\begin{cases} \dot{y}_1 = \xi y_1 + \alpha y_2 + cy_4 - dy_1 y_4^2 + u_1, \\ \dot{y}_2 = \eta y_1 - y_2 + \mu y_3 + u_2, \\ \dot{y}_3 = -\beta y_2 - \gamma y_3 + u_3, \\ \dot{y}_4 = -\rho y_1 + u_4, \end{cases} \quad (36)$$

where y_1, y_2, y_3, y_4 are the states and u_1, u_2, u_3, u_4 are the designed controllers, whereas the synchronization error based on the active control method is defined as follows:

$$\dot{e}_i = \dot{y}_i - \dot{x}_i, \quad (i = 1, 2, 3, 4). \quad (37)$$

According to (37), the synchronization error system between the memductor-based drive system (35) and the memductor-based response system (36) is easily obtained as follows:

$$\begin{cases} \dot{e}_1 = \xi e_1 + \alpha e_2 + ce_4 - d(y_1 y_4^2 - x_1 x_4^2) + u_1, \\ \dot{e}_2 = \eta e_1 - e_2 + \mu e_3 + u_2, \\ \dot{e}_3 = -\beta e_2 - \gamma e_3 + u_3, \\ \dot{e}_4 = -\rho e_1 + u_4. \end{cases} \quad (38)$$

Then, the active controller system is designed as follows:

$$\begin{cases} u_1 = -\xi e_1 - \alpha e_2 - ce_4 + d(y_1 y_4^2 - x_1 x_4^2) - k_1 e_1, \\ u_2 = -\eta e_1 + e_2 - \mu e_3 - k_2 e_2, \\ u_3 = \beta e_2 + \gamma e_3 - k_3 e_3, \\ u_4 = \rho e_1 - k_4 e_4, \end{cases} \quad (39)$$

where k_1, k_2, k_3, k_4 are the control gains, and they are positive values, respectively. Substituting (39) into (38), the active synchronization error system is obtained as follows:

$$\begin{cases} \dot{e}_1 = -k_1 e_1, \\ \dot{e}_2 = -k_2 e_2, \\ \dot{e}_3 = -k_3 e_3, \\ \dot{e}_4 = -k_4 e_4. \end{cases} \quad (40)$$

Next, the Lyapunov function V is defined as follows:

$$V = \frac{e_1^2 + e_2^2 + e_3^2 + e_4^2}{2}. \quad (41)$$

Thus, it is obvious that V is positively definite. Differentiating V ,

$$\begin{aligned} \dot{V} &= e_1 \dot{e}_1 + e_2 \dot{e}_2 + e_3 \dot{e}_3 + e_4 \dot{e}_4 \\ &= e_1(-k_1 e_1) + e_2(-k_2 e_2) + e_3(-k_3 e_3) + e_4(-k_4 e_4) \\ &= -k_1 e_1^2 - k_2 e_2^2 - k_3 e_3^2 - k_4 e_4^2. \end{aligned} \quad (42)$$

According to (42), $\dot{V} = -k_1 e_1^2 - k_2 e_2^2 - k_3 e_3^2 - k_4 e_4^2 \leq 0$ is easily obtained. That is to say, \dot{V} is negatively semidefinite. Based on the Lyapunov stability theory, if V is positively definite and \dot{V} is negatively semidefinite, then the system is consistent and stable at the origin of the equilibrium state [38]. Accordingly, the active synchronization error system (38) is asymptotically stable at the origin. Thus, $\lim_{t \rightarrow \infty} |e(t)| \rightarrow 0$. It is proved that the synchronization between the novel memductor-based drive system and the novel memductor-based response system is achieved. In the following numerical simulations, the initial values of the novel memductor-based system are chosen as $x_1(0) = -0.17528$, $x_2(0) = -1.0872$, $x_3(0) = 1.6368$, and $x_4(0) = -3.2852$. The control gains are chosen as $k_1 = k_2 = k_3 = k_4 = 10$.

The history of the synchronization errors between the novel memductor-based drive system and the novel memductor-based response system is shown in Figure 8. It is clear from Figure 8 that the active synchronization errors e_1, e_2, e_3, e_4 can be asymptotically stabilized at the origin in

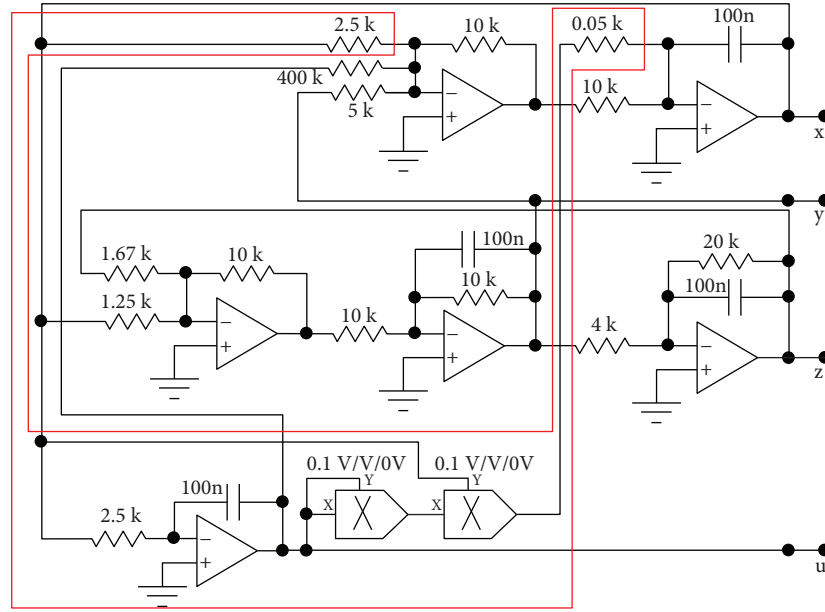


FIGURE 9: The novel memductor-based chaotic circuit schematic.

a very short period of time. The active control method is simple, practical, and easier to be implemented in an electronic circuit. It can be applied to other complex memductor-based chaotic systems to implement synchronization and chaotic secure communication.

4. Circuit Design and Hardware Implementation

4.1. Circuit Design. Based on the novel 4D memductor-based chaotic system (23), the normalized resistor is set as $R_{\text{normalization}} = 100 \text{ k}\Omega$ in order to design the memductor-based chaotic circuit. In view of the need for higher accuracy, the low-power AD633 analog multipliers are chosen in the

chaotic circuits, which enjoy the precision of laser trimming and remain stable between -10 V and $+10 \text{ V}$. Taking into considering the convenience of power supply and the feasibility of the circuit, as well as saving components, the selected operational amplifiers are LF347N and LF353N with the power supply voltage ranging from -15 V to $+15 \text{ V}$. In order to prevent the voltage in the circuit from exceeding the range of operational amplifier, the ranges of the variables in system (22) have been adjusted appropriately, and a new memductor-based chaotic system (23) was obtained after scale transformation. Because the precision provided by AD633 is $1/10 \text{ V}$, the input factor for analog multiplier is 0.1 V . Conclusively, the state equation of the memductor-based chaotic circuit is obtained by rewriting (23):

$$\begin{cases} \dot{x} = \frac{100 \text{ k}}{2.5 \text{ k}} \times 0.1x + \frac{100 \text{ k}}{5 \text{ k}} \times 0.1y + \frac{100 \text{ k}}{400 \text{ k}} \times 0.1u - \frac{100 \text{ k}}{0.05 \text{ k}} \times 0.001xu^2, \\ \dot{y} = \frac{100 \text{ k}}{1.25 \text{ k}} \times 0.1x - \frac{100 \text{ k}}{10 \text{ k}} \times 0.1y + \frac{100 \text{ k}}{1.67 \text{ k}} \times 0.1z, \\ \dot{z} = -\frac{100 \text{ k}}{4 \text{ k}} \times 0.1y - \frac{100 \text{ k}}{20 \text{ k}} \times 0.1z, \\ \dot{u} = -\frac{100 \text{ k}}{2.5 \text{ k}} \times 0.1x. \end{cases} \quad (43)$$

Thus, the novel memductor-based chaotic circuit schematic is designed as shown in Figure 9 according to (43). The circuit is divided into two parts: the nonmemristor part and the independent memristor part. The memristor part is

the red circuit marked in Figure 9. The rest of the circuit is the nonmemristor part, a linear part. What is seen from Figure 9 is that the novel memductor-based chaotic circuit is composed of six operational amplifiers and two analog

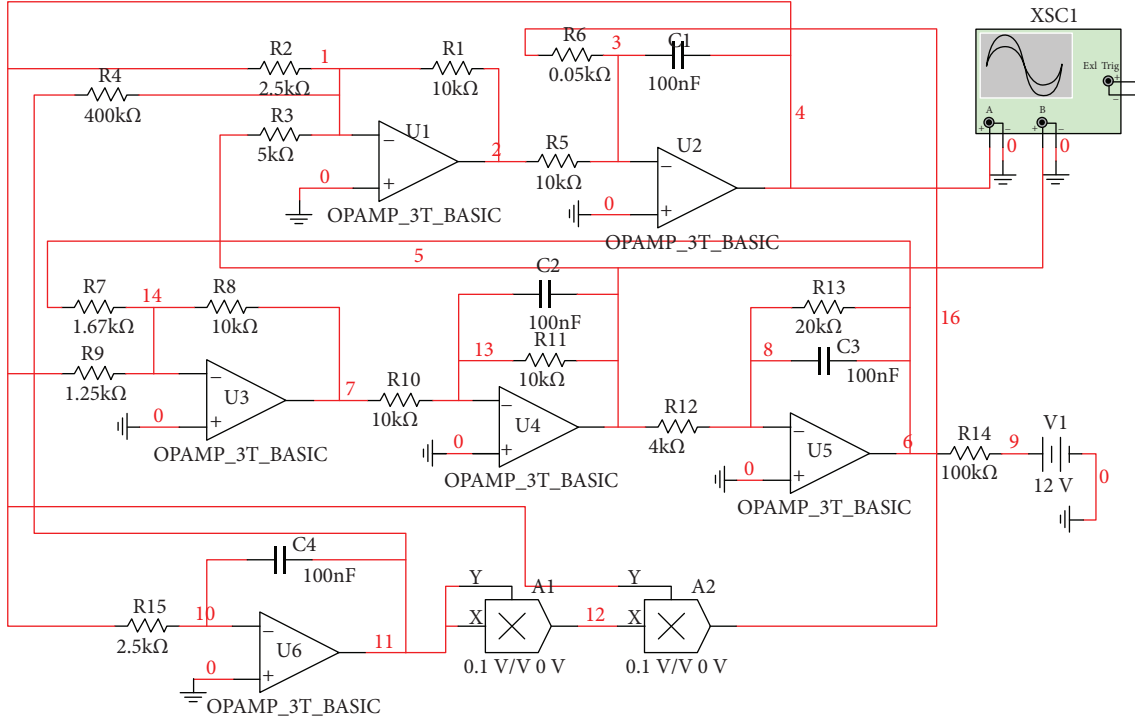


FIGURE 10: The novel memductor-based chaotic circuit with Multisim.

multipliers. It outputs four signal waveforms, six phase portraits, and stable fourth-order double vortex chaotic signals. Accordingly, Figure 10 shows the novel memductor-based chaotic circuit with Multisim.

All of the electronic components are easily available. The memductor-based chaotic phase portraits of the novel memductor-based chaotic circuit by Multisim are shown in Figure 11. It can be shown from the simulation results that it outputs six chaotic phase portraits of xy , xz , zy , xu , yu , and zu . Moreover, the Multisim simulation results are consistent with the MATLAB simulation results as shown in Figure 3. That is, it fully conforms to the requirements of circuit design in practical applications.

4.2. Hardware Implementation. Most researchers highlight the study of memristor chaos theory in numerical simulation; in that case, there is a certain deviation in the physical memristor circuit system. Based on the correct simulation results shown in Figure 11, with the purposes to verify that the novel memductor-based chaotic circuit enjoys high accuracy and good robustness and further study the chaotic dynamical characteristics of the novel memductor-based chaotic system (23), a practical electronic circuit is constructed by using some general electronic components such as operational amplifiers, analog multipliers, resistors, and capacitors according to the circuit model of Figure 9.

It should be noted that the problems easily occurring in the process of constructing the memductor-based chaotic circuit should be tackled. For example, the chaotic circuit is more sensitive to the initial value because of adding the memristor, and any minor change will lead to unpredictable results. Therefore, we chose the values of the resistors closer

to the simulation resistor to construct the circuit and test whether each module of the circuit works properly in the process of constructing. Afterwards, input voltage to the system and access the oscilloscope, the output phase portrait photos of the novel memductor-based chaotic circuit are shown in Figure 12. Figure 13 shows the experimental circuit board photo.

What should be seen from the experimental results shown in Figure 12 is that the phase portraits of the novel memductor-based chaotic attractors displayed by oscilloscope coincide with the simulation results of MATLAB and Multisim. That is, it proves true that the memductor-based chaotic attractors exist in real. The proposed memductor-based chaotic circuit design method provides a reliable and straightforward way for realizing memristive chaotic circuits, and the method plays a significant role in easily handling and avoiding the output voltage beyond the limitation of the amplifier linear region efficiency.

4.3. Experimental Results Analysis. Through careful experiments on the proposed memductor-based chaotic circuit shown in Figure 9, the following important conclusions can be obtained:

- (i) The impact of switching power seems to exist. Once the chaotic state is entered, the chaotic attractors begin to become stable. The memductor-based chaotic circuit characteristics of this phenomenon are presented as follows: when the power is turned on, two attractors contribute to establish a stable state of the circuit. One is a chaotic attractor, which tells the fact that the voltage amplitude is less than the

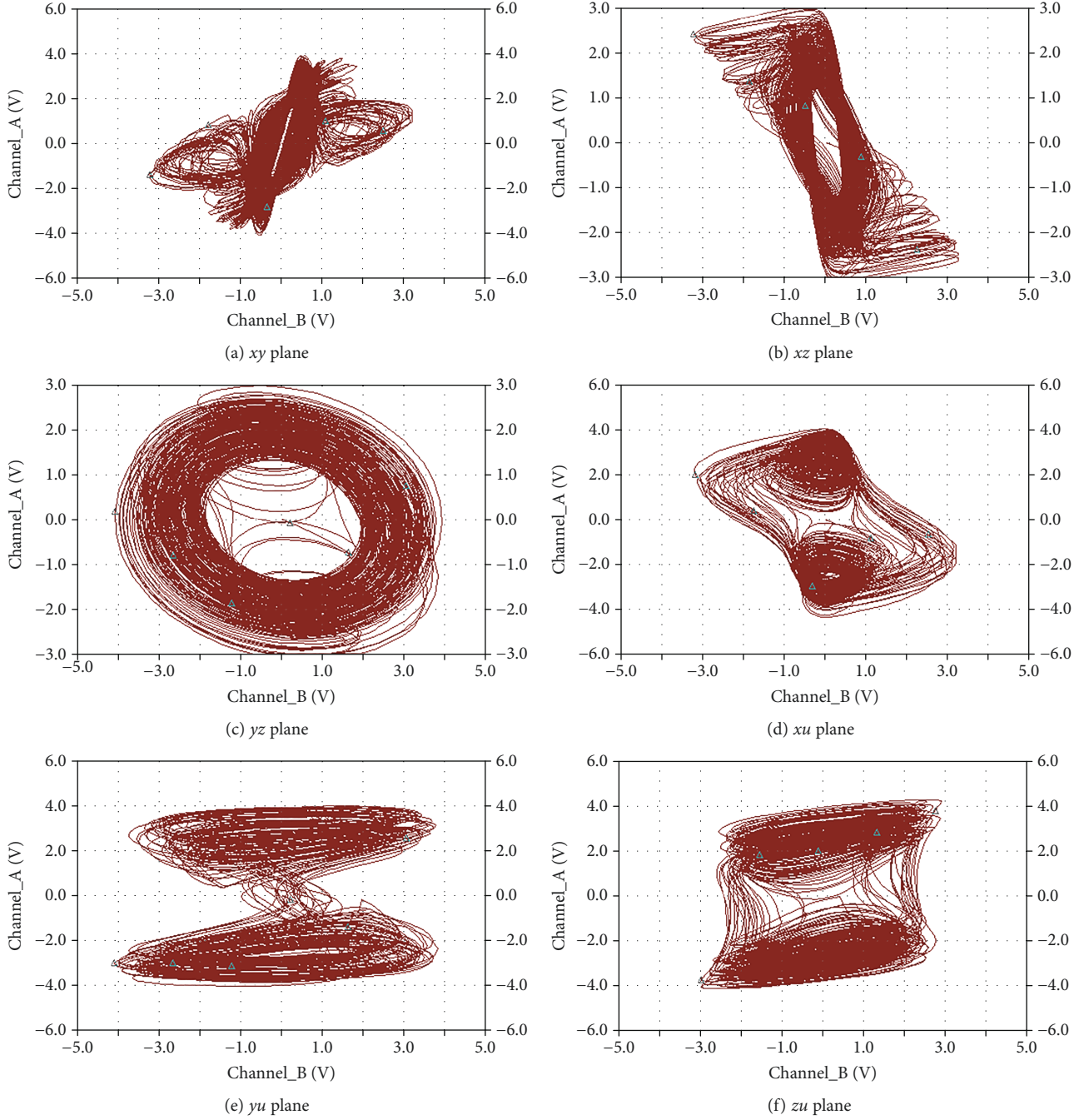


FIGURE 11: The chaotic attractors of the novel memductor-based chaotic circuit with Multisim.

supply voltage, and no amplitude limiting condition occurs. The other is the possibility of entering a state of limiting amplitude and not breaking out of the limiting amplitude state, but entering the traditional periodic oscillation, and this oscillation is a stable oscillation

- (ii) The ranges of the physical variables measured in this experiment are presented as follows: x ranges from -2.2 V to $+2.2\text{ V}$, y ranges from -4.4 V to $+4.4\text{ V}$, z ranges from -4.4 V to 4.4 V , and u ranges from -4.8 V to $+4.8\text{ V}$. This set of data is easy to be

controlled. So as long as the resistance of the 4 K resistor is adjusted, the amplitude of the chaos varies accordingly and the shape remains unchanged, which is extremely convenient

- (iii) A good memductor-based chaotic circuit must be designed without defects. One of the defects is the voltage limit of the regulated power supply. The defects may appear in designing of the operational amplifier and inverting integrator. As for the design defect of operational amplifier, the feedback resistor of the operational amplifier R_f is greater

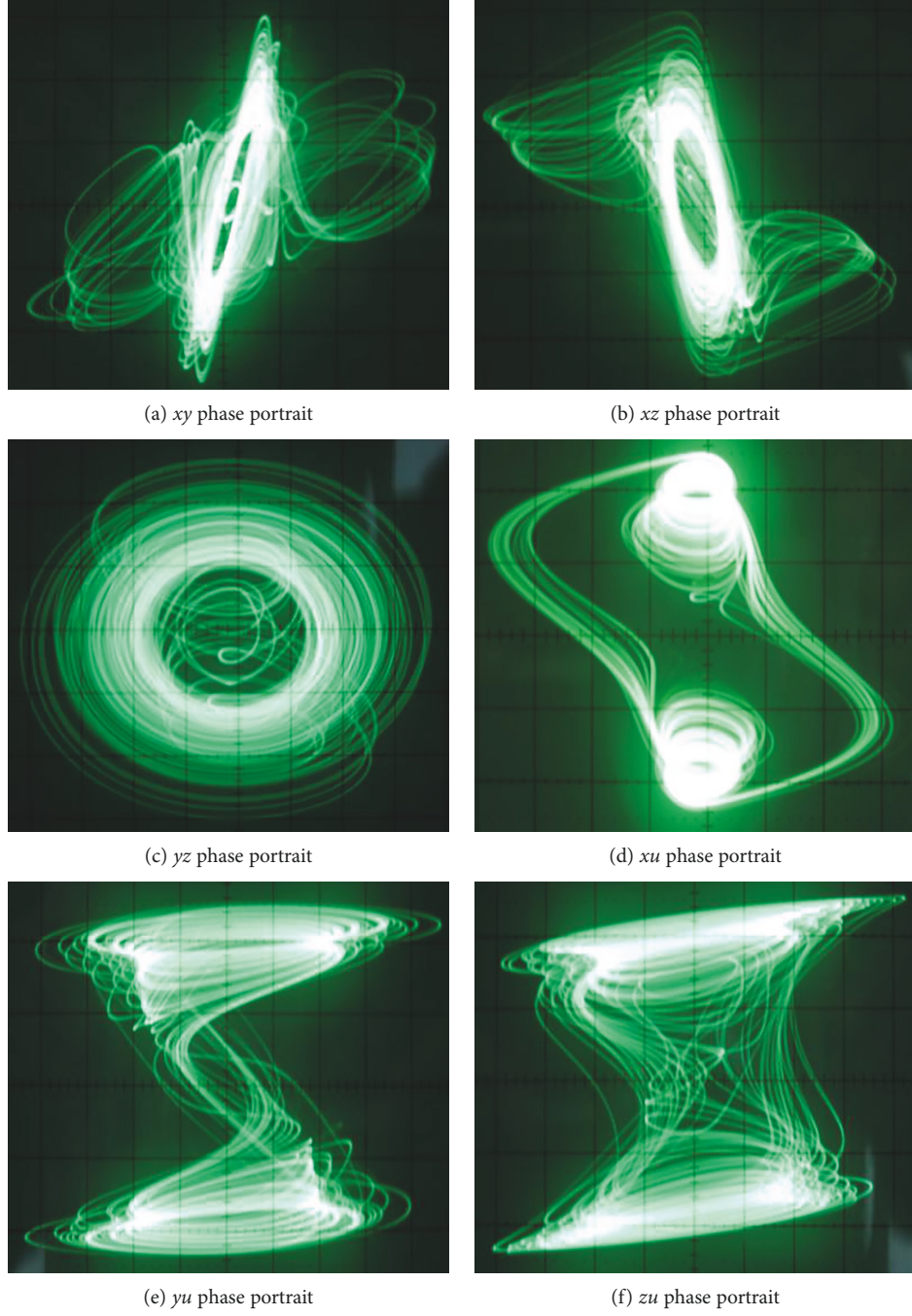


FIGURE 12: The output phase portrait photos.

than that of the input circuit R_{in} . That is, the design defect is presented as

$$R_f > R_{in}. \quad (44)$$

Moreover, if the operational amplifier is equipped with two input resistors, the design defect is presented as follows:

$$R_f > \frac{1}{(1/R_{in1}) + (1/R_{in2})}. \quad (45)$$

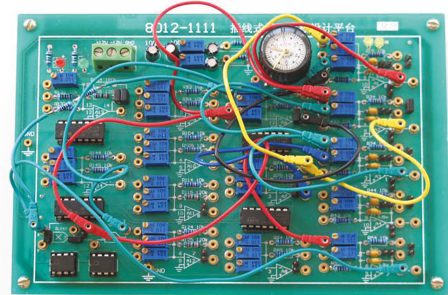


FIGURE 13: Experimental circuit board photo.

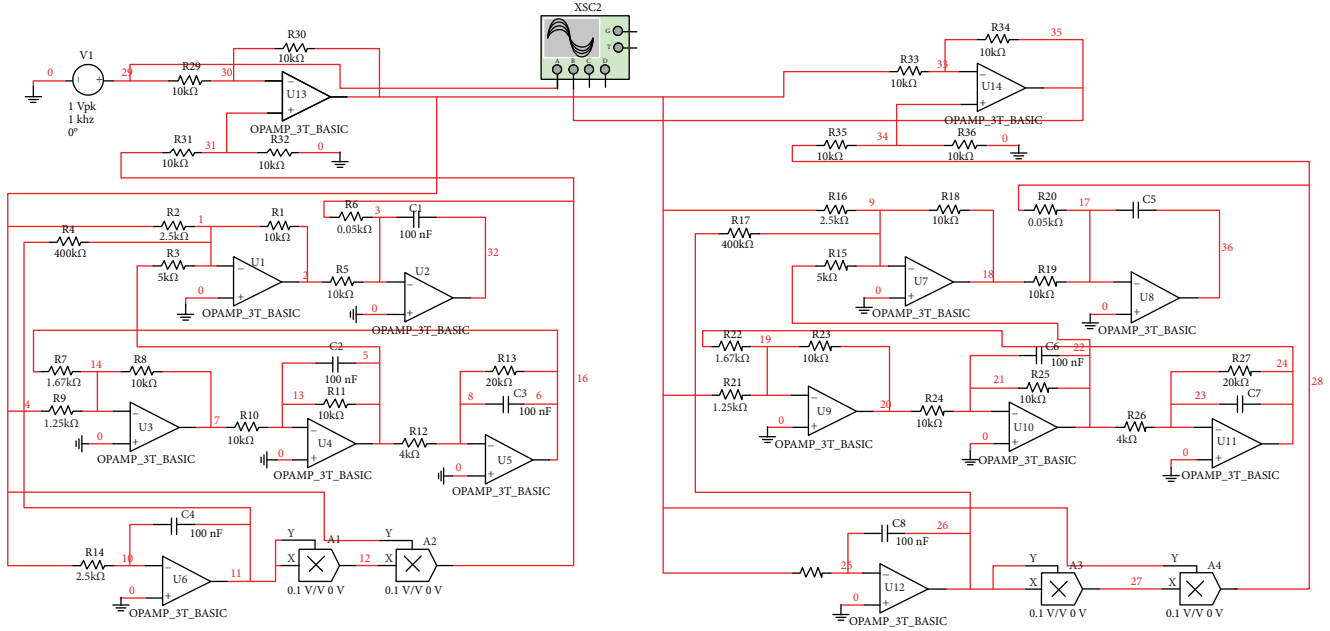


FIGURE 14: A novel memductor-based secure communication circuit by Multisim.

Therefore, both of these conditions may cause amplitude limiting distortion, which makes the design of memductor-based circuits deviates from the original intention of chaotic mathematical model.

And as for the design defect of the inverting integrator, the normalized resistance of the inverting integrator is set as $R_{\text{normalization}}$; thus, the possible defect of the memductor-based circuit design is presented as follows:

$$R_{\text{in}} < R_{\text{normalization}}, \quad (46)$$

which is hard to achieve, since in some cases, the mathematical model itself is involved, and it is not just the circuit design but also the circuit model involved. Therefore, the reason why the steady phase portraits have not been debugged is that the design of the operational amplifier violates (44) or (45).

- (iv) Here, a new concept, called “the memductor-based chaotic circuit defect quantification index”, is first proposed. The new concept of quantification consists of two parts logically. First of all, the single-stage defect coefficient is considered. For a stage operational amplifier, if the operational amplifier does not violate (44) and (45), the defect coefficient of the memductor-based chaotic circuit is equal to zero. If (44) and (45) are violated, the defect coefficient of the operational amplifier is defined as

$$\varepsilon_{\text{defect}} = \frac{R_f}{R_{\text{in}}} - 1 = \frac{R_f - R_{\text{in}}}{R_{\text{in}}}. \quad (47)$$

Secondly, the defect coefficient of the whole memductor-based circuit system is the sum of the defect coefficient at

all levels of the unit circuit. Physical experiments in this paper show that the chaotic output of the memductor-based circuit with the parameters shown in Figure 9 is the most stable, and they are consistent with the MATLAB and Multisim simulation results.

5. Application of the Proposed Memductor-Based Chaotic Circuit

Since the memductor-based chaotic signal is more sensitive to the initial value than the ordinary chaotic signal, it is especially suitable for the secure communication field. In order to improve the security of secure communication system, it is considered that the novel memductor-based chaotic system should be selected as the chaotic system. In the proposed memductor-based chaotic secure communication scheme, the memristive secure communication circuit is implemented by using some electronic components containing analog multipliers, operational amplifiers, resistors, and capacitors with a novel 4D memductor-based chaotic system as chaos generator. Based on the proposed memductor-based chaotic circuit shown in Figure 9, the memductor-based secure communication circuit schematic by Multisim is shown in Figure 14. Its circuit principle is carefully presented as follows:

It consists 14 operational amplifiers together with 4 analog multipliers. Its basic circuit is composed of two proposed identical memductor-based chaotic circuit units with a little change. The left side of the circuit is the transmitter and the right side of the circuit is the receiver. The inverting input end of transmitter-modulator is connected with the transmitted signal to be transmitted. The same phase input end is connected with the x output terminal of the novel memductor-based chaotic circuit. In this way, the receiving system and the transmitting system are easier to maintain synchronization, and the robustness of the memductor-

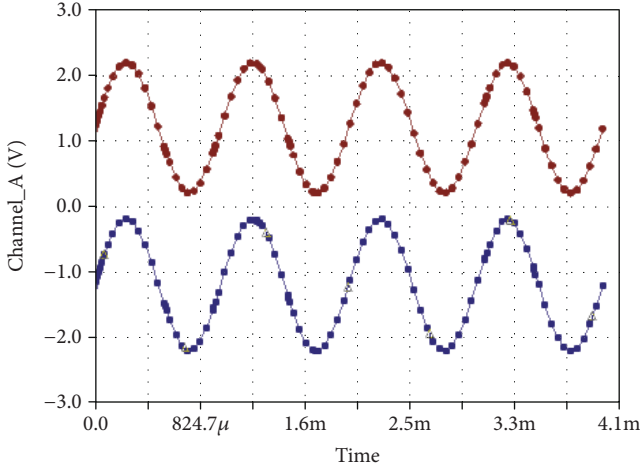


FIGURE 15: Transmitting and receiving waveforms.

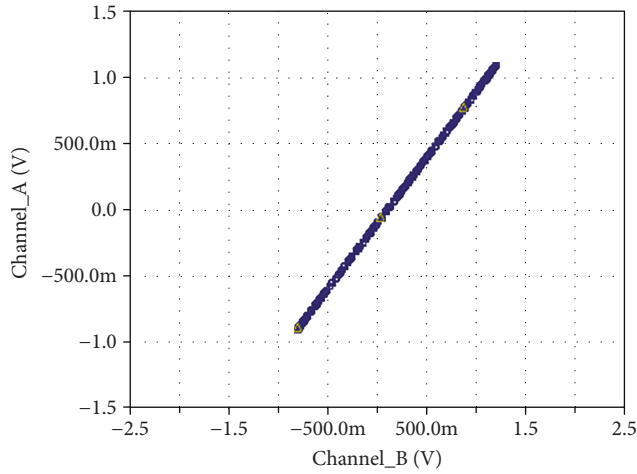


FIGURE 16: Synchronous phase portrait.

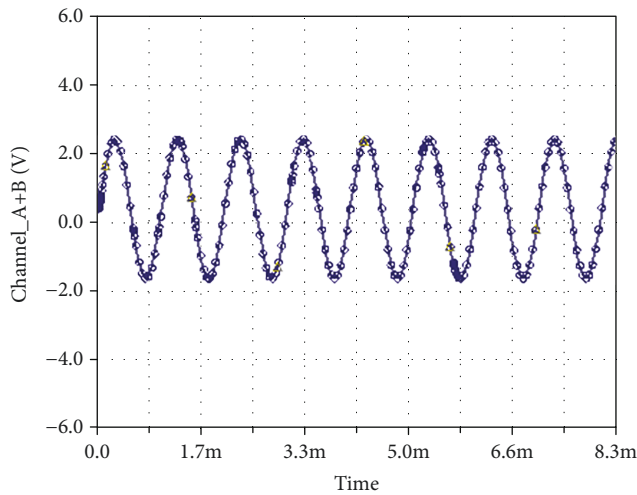


FIGURE 17: Superimposed signal waveform.

based chaotic circuit is also maintained. This method prevents effective information from being intercepted in the secure communication process.

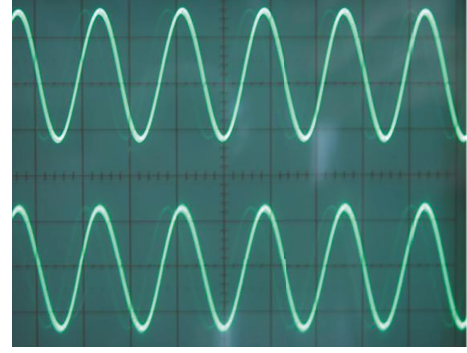


FIGURE 18: Transmitting and receiving signal photo.

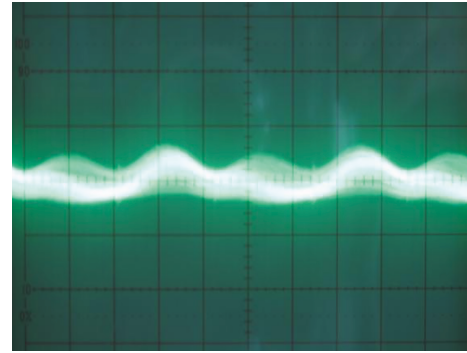


FIGURE 19: Modulation and demodulation waveform subtraction.

In what follows, the simulation experiments are presented to verify whether two identical parameters of the memductor-based chaotic circuits can effectively achieve the signal transmission and reception without distortion. Suppose an input sine wave with amplitude of 1 V and frequency of 1 kHz is given in the circuit simulation, the transmitting and receiving signal waveform by Multisim is shown in Figure 15. The synchronous phase portrait is shown in Figure 16. And Figure 17 shows the superimposed signal waveform of the modulation and demodulation signal. It is obvious from the simulation results that, no matter what kinds of signals are input, the two identical memductor-based chaotic circuits entirely maintain synchronization with each other if the component parameters of the transmitting circuit are exactly the same with the receiving circuit. Almost no distortion can be seen.

Subsequently, the hardware circuit experiments of the proposed chaotic secure communication circuit based on the memductor-based chaotic circuit are implemented successfully. To verify the above Multisim simulation results, accordingly, an input sine wave with amplitude of 1 V and frequency of 1 kHz is taken in the practical electronic circuit experiment. It should be noted that the transmitting and receiving signal waveform photo is shown in Figure 18. Figure 19 shows the modulation and demodulation waveform subtraction. It is evident that the difference between the two waves (i.e., noise) is only 10 microvolts when the most sensitive gear of the oscilloscope is 10 μV . The synchronous phase portrait photo is shown in Figure 20. Figure 21 shows the superimposed signal photo of the modulation

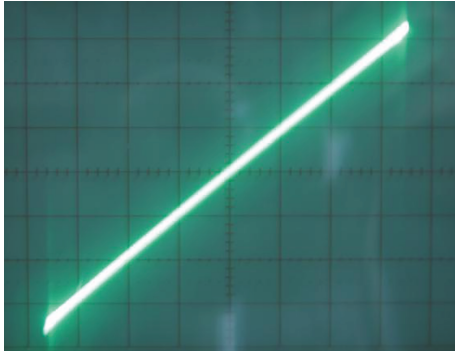


FIGURE 20: Synchronous phase portrait photo.

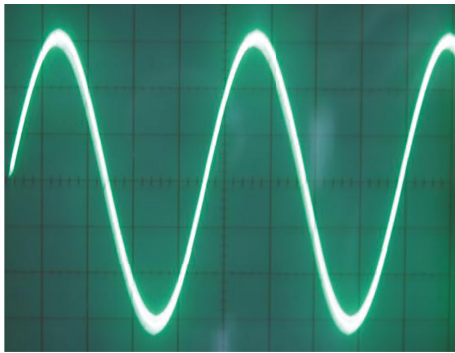


FIGURE 21: Superimposed signal photo.

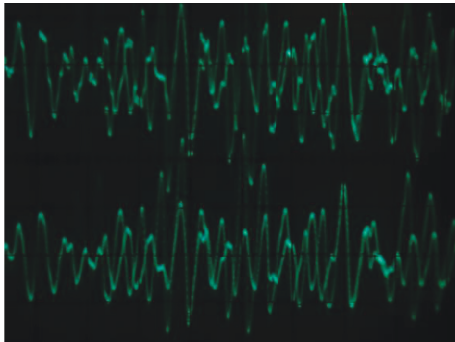


FIGURE 22: The transmitting modulation signal and the receiving demodulation signal photo.

and demodulation waveform. Figure 22 shows the transmitting modulation signal and the receiving demodulation signal waveform photo on the oscilloscope. According to the experimental measurement results of the memductor-based chaotic secure communication circuit, it is obvious that the transmitting and receiving signal waveform photo and the synchronous phase portrait photo displayed by oscilloscope coincide with the Multisim simulation results.

Nevertheless, the memductor-based chaotic circuits composed of conventional operational amplifiers and analog multipliers still have some limitations, mainly because of the frequency limitations of the operational amplifiers. As already shown in [38], the operational amplifiers allow us to implement any type of circuit that is useful in analog

processing applications. However, its performance in realizing chaotic circuits is limited. In work [38], the signals can be transmitted from 1 Hz to 500 kHz without distortion for the hyperchaotic secure communication circuit. When the signal frequency exceeds 500 kHz, the signal distortion will be very obvious. Thus, in order to transmit high-speed data, the chaotic attractors should work at high frequency. In addition, high frequency should be enhanced from the aspect of improving the security and confidentiality of chaotic secure communication circuits.

6. Conclusion

In this paper, a novel memductor-based chaotic system is proposed by adding a one-dimensional memristor equation to a particular three-dimensional chaotic system according to the physical nonlinear characteristics of memductor through looking for suitable parameters. And this paper is an attempt to investigate the dynamical behaviors and synchronous stability of the novel memductor-based chaotic system and realize these dynamics in a new physical circuit. What can be seen from the simulation results and experimental results is that they do not only output six phase portraits but also output stable fourth-order double vortex chaotic signals, respectively. In order to enhance the security performance of transmission signal and improve the vulnerability of the novel memristive system, the novel memductor-based chaotic circuit is applied to construct a new memductor-based chaotic secure communication circuit. Comparisons among Multisim simulation, MATLAB simulation results, and physical experimental results show that they are consistent with each other, and the attractors of the novel memductor-based chaotic system exist. What is more, the concept of “the memductor-based chaotic circuit defect quantification index” is proposed for the first time to verify whether the chaotic output is consistent with the mathematical model, which provides a powerful theoretical basis for the successful design and implementation of memductor-based chaotic circuits. These proposed circuit design methods can also be applied in other complex memristor-based chaotic systems.

Nevertheless, the conventional operational amplifiers have somewhat performance limitations in implementing memductor-based chaotic circuits. It is quite hard to improve the frequency response for analog implementation of chaotic oscillator when it is designed with integrated circuits. Perhaps the implementation based on FPGA can be used as a solution to observe memductor-based attractors at higher frequencies. Thus, our future research will devote to the circuit realization of memductor-based systems by using FPGA.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors have declared that no competing interests exist.

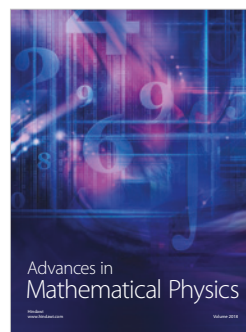
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