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Research Article

Fully Integrated Memristor and Its Application on the Scroll-Controllable Hyperchaotic System

Jie Jin[1,2] **and Li Cui**[1]

[1]*School of Information and Electrical Engineering, Hunan University of Science and Technology, Xiangtan 411201, China*
[2]*College of Information Science and Engineering, Jishou University, Jishou 416000, China*

Correspondence should be addressed to Jie Jin; jj67123@sina.com

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In this paper, a fully integrated memristor emulator using operational amplifiers (OAs) and analog multipliers is simulated. Based on the fully integrated memristor, a scroll-controllable hyperchaotic system is presented. By controlling the nonlinear function with programmable switches, the memristor-based hyperchaotic system achieves controllable scroll numbers. Moreover, the memristor-based hyperchaotic system is fully integrated in one single chip, and it achieves lower supply voltage, lower power dissipation, and smaller chip area. The fully integrated memristor and memristor-based hyperchaotic system are verified with the GlobalFoundries' 0.18 μm CMOS process using Cadence IC Design Tools. The postlayout simulation results demonstrate that the memristor-based fully integrated hyperchaotic system consumes 90.5 mW from ±2.5 V supply voltage and it takes a compact chip area of 1.8 mm^2.

1. Introduction

Memristor and multiscroll chaos systems are two research hotspots in recent years. Although, memristor is not commercially available, many memristive emulators have been reported [1–5]. Based on these memristive emulators, various kinds of memristor-based chaotic circuits have been presented [6–12] and they effectively promote the development of the memristive circuit theories.

Most of the existing memristive emulators and memristor-based chaotic circuits are realized using commercially available off-the-shelf discrete components with breadboard or field programmable gate array (FPGA). The breadboard or FPGA-based chaotic circuits are difficult to achieve low-voltage and low-power conditions. As we all know, the fully integrated circuits have the advantages of lower supply voltage, less power consumption, more stable and convenient than their breadboard-based counterparts. Cruz and Chua [13, 14] realized fully integrated Chua's circuit and nonlinear resistor in 1992 and 1993. Elwakil et al. [15] realized another integrated chaotic system in 2002, which further verified the advantages of the integrated chaotic circuits. However, the existing integrated chaotic circuits are very simple; they could not realize more complicated chaos.

In order to realize more practical and complicated integrated memristor-based chaotic circuits, a fully integrated memristor emulator and a scroll-controllable hyperchaotic system are presented and verified in this paper. The Cadence IC Design Tools post-layout simulation results verify that the presented fully integrated memresistor and memristor-based scroll-controllable hyperchaotic system are all feasible and achievable and the fully integrated method will further promote the practical applications of chaotic circuits and systems.

2. Fully Integrated Scroll-Controllable Hyperchaotic System and Its Dynamics Analysis

2.1. Implementation of the Operational Amplifier. In a fully integrated chaotic system, complex and high-performance OA is not necessary, and the designed low-voltage and low-power two-stage OA with simple structure for the fully

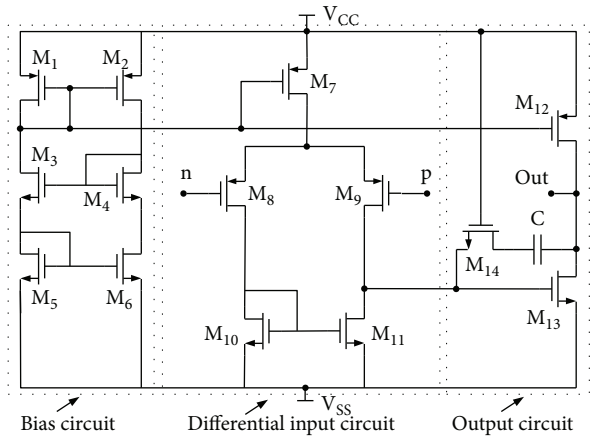

Figure 1: The designed OA.

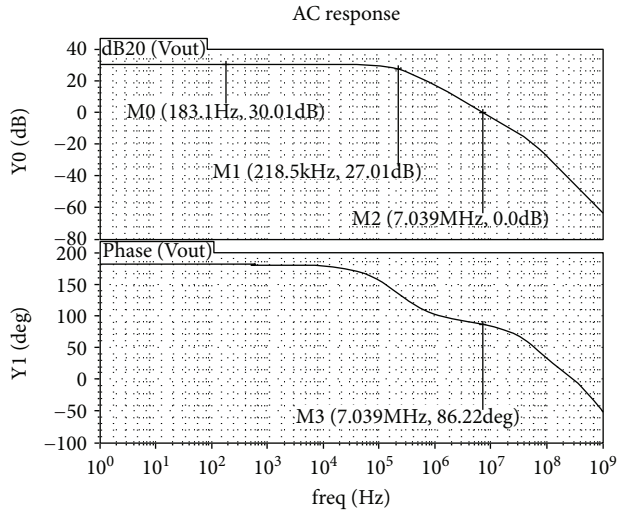

Figure 2: The amplitude and phase frequency of the OA.

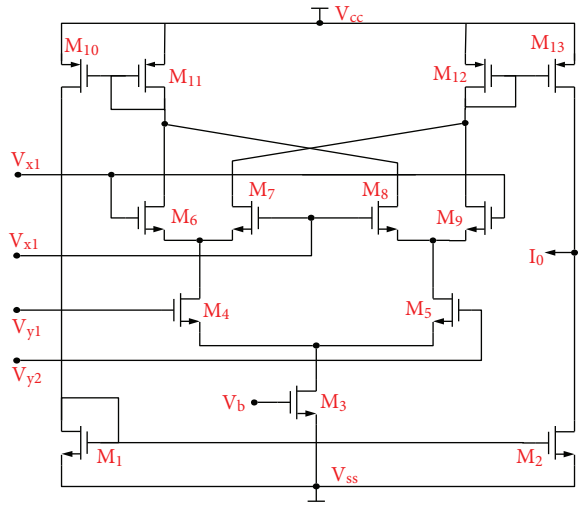

Figure 3: The designed analog multiplier.

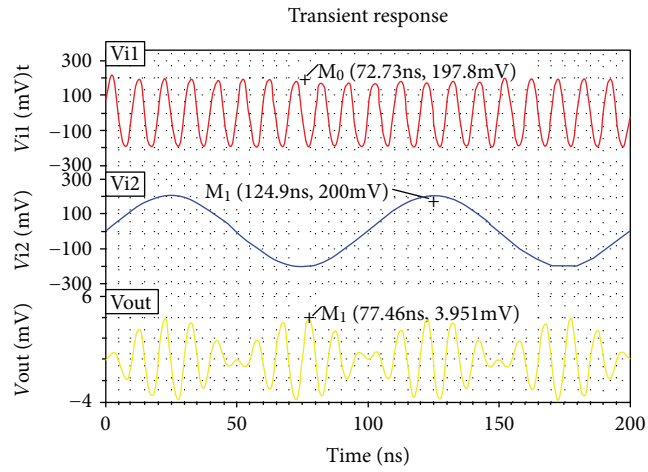

Figure 4: The transient response of the analog multiplier.

integrated chaotic system is presented in Figure 1 [16]. The supply voltage of the designed operation amplifier is $V_{CC} = -V_{SS} = 2.5\,V$. The P-channel transistors M_7–M_9 [17] and N-channel transistors M_{10}–M_{11} consist of a double-ended input single-ended output differential input stage; M_{12} and M_{13} consist of the second common source amplifier stage; M_{14} and capacitor C consist of the frequency compensation network between the two stages; the transistors M_1–M_6 consist of the bias circuit of the OA.

The simulated amplitude and phase-frequency characteristics of the operation amplifier are presented in Figure 2. From the marks M_0–M_3, it is clear that the voltage gain of the operation amplifier is about 30 dB, its 3 dB bandwidth is 218.5 kHz, and the phase margin is about 86.22°. Its static power consumption is about 5.85 mW with ±2.5 V supply voltage.

2.2. Implementation of the Analog Multiplier. The analog multiplier used in the memristor is presented in Figure 3. The classic Gilbert structure [18–20] is adopted. M4 and M_5 consist of the transconductance stage; M_6–M_9 consist of the Gilbert switch stage, and M_{10}–M_{13} consist of the load stage of the analog multiplier. The supply voltage of the designed analog multiplier is $V_{CC} = -V_{SS} = 2.5\,V$.

The transient responses of the designed analog multiplier are presented in Figure 4. V_{i1} and V_{i2} are the two input voltages; their input powers are all −10 dBm, and their frequencies are 100 MHz and 10 MHz, respectively. V_{out} is the output voltage of the analog multiplier. From the above simulation results, it is clear that V_{i1} is the high-frequency carrier, V_{i2} is the low-frequency input signal, and the multiplication is realized in the output voltage V_{out}.

2.3. The Fully Integrated Memristor. Memristors could be classified as flux-dependent and charge-dependent memristors. A fully integrated flux-controlled memristor is adopted in this work, and its circuit realization using operation amplifier and multipliers is presented in Figure 5.

The voltage and current relation of the flux-controlled memristor could be expressed as

$$i = W(\varphi)v, \quad \dot{\varphi} = v, \tag{1}$$

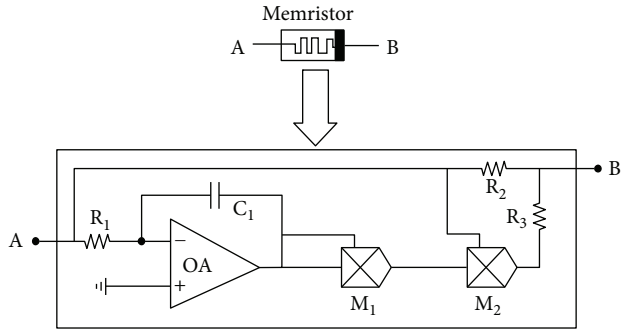

Figure 5: The fully integrated memristor.

where $W(\varphi)$ is an incremental memductance function [21]. In order to research the characteristics and application of memristor, various mathematical models and emulator circuits of memristor have been reported in recent years [1–3, 22]. According to [6, 23], a quadric nonlinearity is used to indicate memductance function:

$$W(\varphi) = a + 3b\varphi^2, \tag{2}$$

where a and b are two positive constants.

Figure 6 shows the Cadence simulation results of the frequency-dependent pinched hysteresis loop of the memristor in Figure 5 operating at various frequencies. The circuit elements used in the memristor are $R_1 = 250$ kΩ, $R_2 = 500$ kΩ, $R_3 = 40$ kΩ, $C_1 = 220$ pF, and the supply voltages of the OA and multiplier are all ±2.5 V.

Figure 6(a) is the simulation result while the frequency of the input voltage equals to 100 kHz, and a clear pinched hysteresis loop is obtained. Figure 6(b) is the simulation result while the frequency of the input voltage equals to 1 MHz; the edges of the pinched hysteresis loop become a bit blurry, and the center of the pinched hysteresis loop becomes narrow. Figure 6(c) is the simulation result while the frequency of the input voltage equals to 5 MHz; the edges of the pinched hysteresis loop become more blurred, and the center of the pinched hysteresis loop becomes more narrow. From the simulation results in Figure 6, it is clear that the fully integrated memristor could operate properly from 1 kHz to 1 MHz. Compared with the memristor using off-the-shelf discrete components with breadboard [24–28], the fully integrated memristor could be used in higher frequency applications.

2.4. The Programmable Staircase Function Circuit. The proposed fully integrated programmable staircase function circuit is presented in Figure 7, and it is realized using the designed OA in Figure 2. The circuit elements used in the memristor are $R_1 = R_4 = R_7 = 1$ kΩ, $R_2 = R_5 = R_8 = 350$ kΩ, $R_3 = R_6 = R_9 = 19.8$ kΩ, $R_{10} = 2.20$ kΩ, and $R_{11} = R_{12} = 10$ kΩ. The programmable MOS switches used in the proposed programmable staircase function circuit is presented in Figure 8. The programmable MOS switch consists of a NMOS and a PMOS transistor, and it can be turned on and off by controlling the bias voltages V_{s+} and V_{s-} [29, 30].

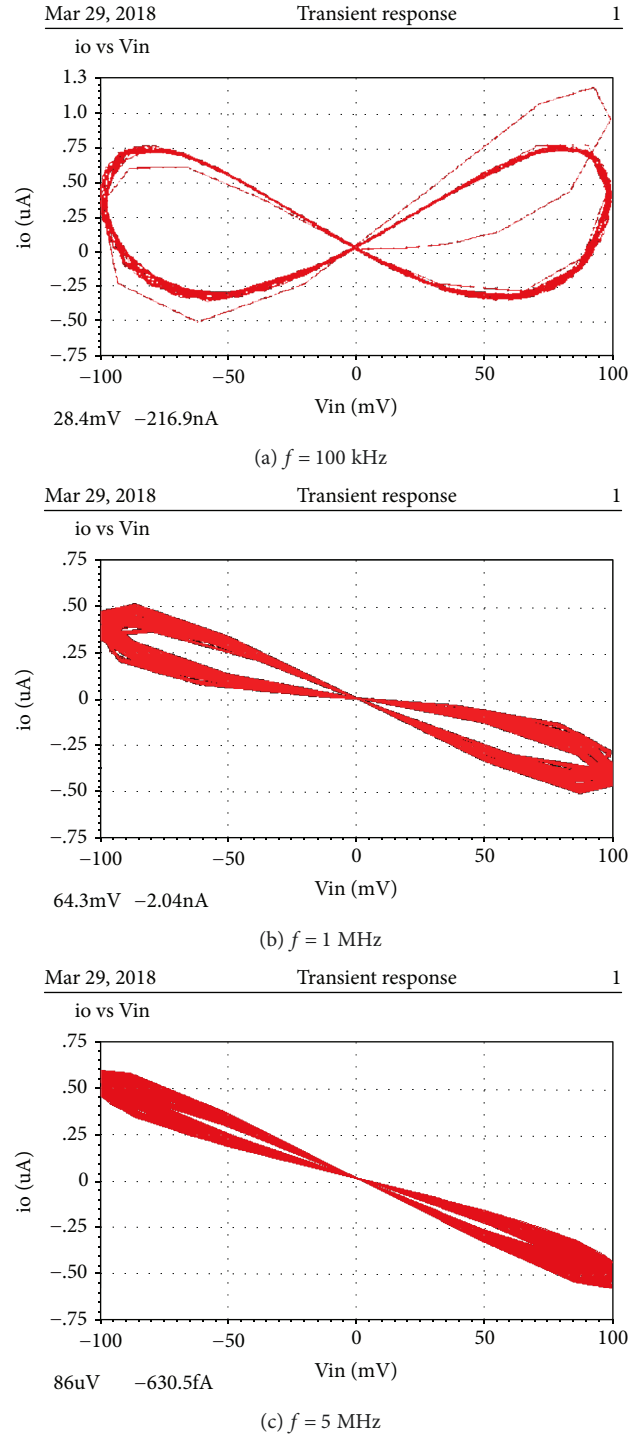

Figure 6: Cadence simulation results of the frequency-dependent pinched hysteresis loop operating at (a) 100 kHz, (b) 1 MHz, and (c) 5 MHz.

By controlling the switches S_1, S_2, and S_3 in Figure 7, the numbers of stairs could be changed. When the switches S_1 and S_3 are turned off, a stair is obtained (Figure 9(a) $N = 1$). When the switch S_2 is turned off, S_1 and S_3 are turned on and two stairs are obtained (Figure 9(b) $N = 2$). When the switches S_1, S_2, and S_3 are all turned on, three stairs are

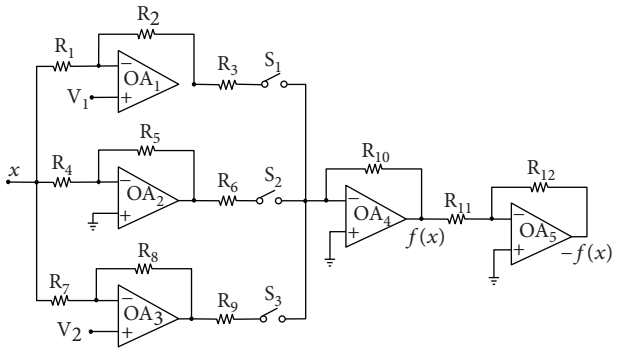

Figure 7: The programmable staircase function circuit.

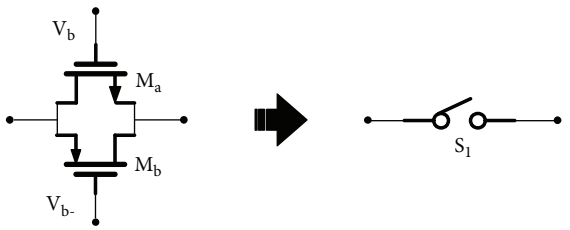

Figure 8: The digitally programmable MOS switch.

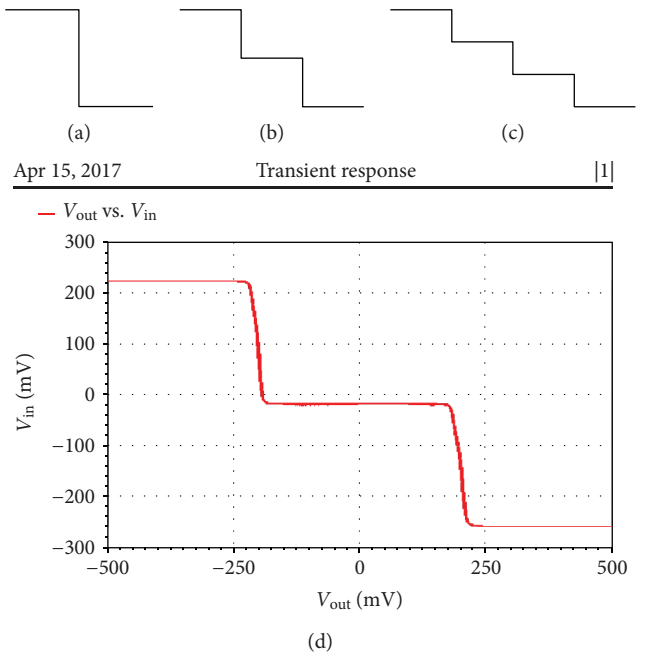

Figure 9: The staircase function: (a) $N = 1$, (b) $N = 2$, and (c) $N = 3$. (d) Simulated staircase function circuit with $N = 2$.

obtained (Figure 9(c) $N = 3$). As an example, when the switch S_2 is turned off, S_1 and S_3 are turned on; the simulated staircase function circuit with $N = 2$ is presented in Figure 9(d).

2.5. The Proposed Fully Integrated Scroll-Controllable Hyperchaotic System and Its Dynamics Analysis. The proposed fully integrated scroll-controllable hyperchaotic system is presented in Figure 10. It consists of a classic Jerk system [31–35] and a flux-controlled memristor in Figure 5. There are three integrators (OA_1, OA_2, and OA_4) and two reverse proportional operators (OA_3 and OA_5) in the fully integrated scroll-controllable hyperchaotic circuit. The circuit elements used in the chaotic circuit are $R_1 = R_2 = R = 4.9$ kΩ, $R_5 = R_6 = R_7 = R_8 = R_k = 9.45$ kΩ, $R_3 = R_4 = R_9 = R_{10} = 10$ kΩ, and $C_1 = C_2 = C_3 = C = 35$ pF.

From Figure 10, the following expression could be obtained:

$$\begin{cases} \dot{x} = \dfrac{y}{RC}, \\ \dot{y} = \dfrac{z}{RC} - \dfrac{W(\varphi)z}{C}, \\ \dot{z} = -\dfrac{x}{R_kC} - \dfrac{y}{R_kC} - \dfrac{z}{R_kC} + \dfrac{f(x)}{R_kC}, \\ \dot{\varphi} = z, \end{cases} \tag{3}$$

where $W(\varphi)$ is the memductance of the memristor and $f(x)$ is the output of the staircase function circuit in Figure 5. The stairs of $f(x)$ can be changed by the programmable switches, and the scrolls of the chaotic system are controllable.

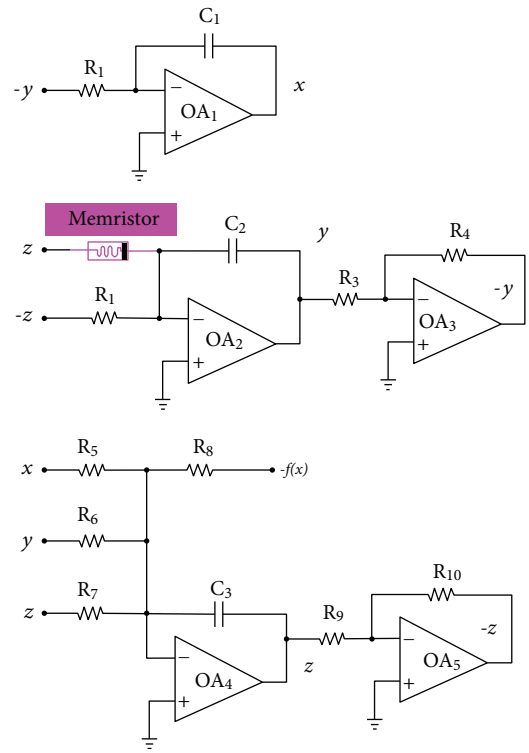

Figure 10: Proposed scroll-controllable hyperchaotic circuit.

In order to explore the nonlinear dynamics of the fully integrated hyperchaotic system, the Lyapunov exponents and bifurcation diagrams are investigated using the MATLAB simulation results.

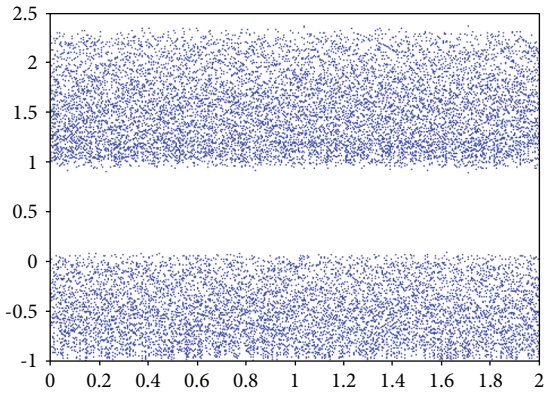

Figure 11: Bifurcation diagram by adjusting α from 0 to 2.

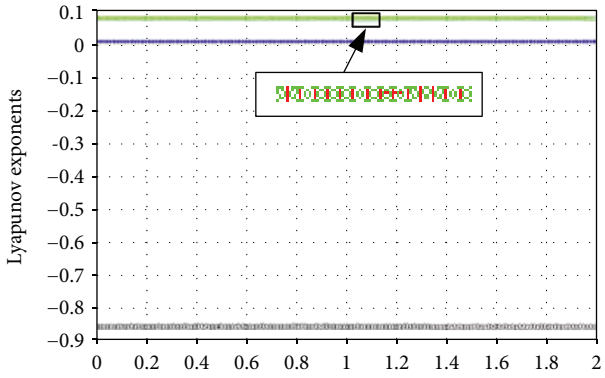

Figure 12: Lyapunov exponents by adjusting α from 0 to 2.

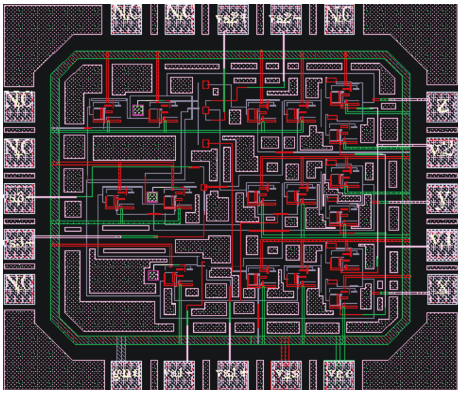

Figure 13: Chip layout diagram of the chaotic circuit (1.8 mm^2).

The dimensionless equations of the chaotic system could be expressed as

$$\begin{cases} \dot{x} = y, \\ \dot{y} = z - \alpha W(\varphi) z, \\ \dot{z} = -\beta(x + y + z) + f(x), \\ \dot{\varphi} = z, \end{cases} \tag{4}$$

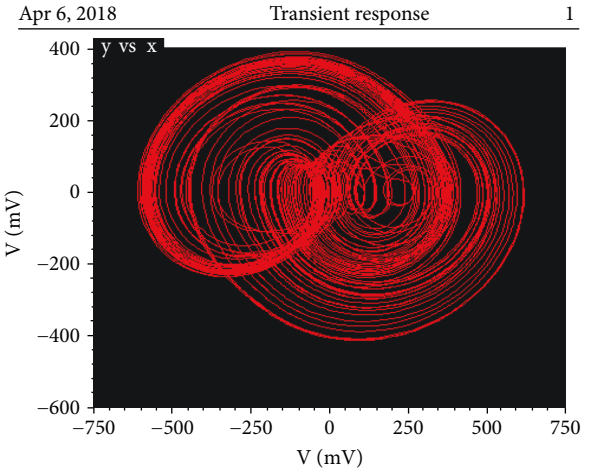

Figure 14: The phase portrait in the x-y plane (S_2 is turned on, S_1 and S_3 are turned off).

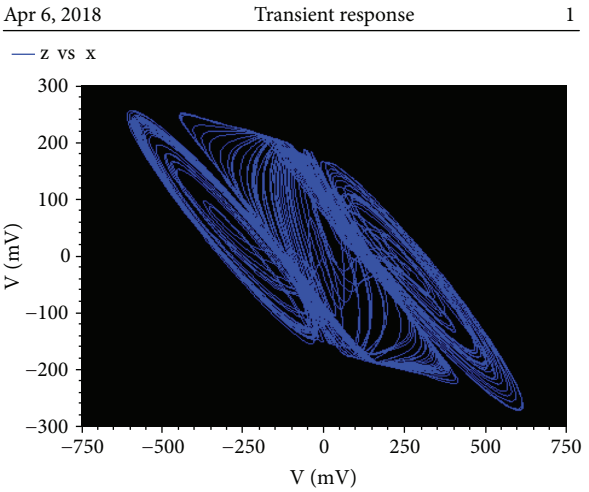

Figure 15: The phase portrait in the x-z plane (S_2 is turned on, S_1 and S_3 are turned off).

where $W(\varphi) = a + 3b\varphi^2$ and α and β are two positive parameters.

Let $\beta = 0.72$, the bifurcation diagram is presented in Figure 11. From Figure 11, it is clear that the system is chaotic, when α is changing from 0 to 2. The Lyapunov exponents of the system by adjusting α from 0 to 2 are presented in Figure 12. From Figure 12, it is clear that there are two Lyapunov exponents more than zero in the system and the proposed system is a hyperchaotic system. Considering Figures 11 and 12, both of the Lyapunov exponents and the bifurcation diagram indicate that the proposed system is chaotic and it could generate complex dynamic behaviors.

3. Postlayout Simulation Results of the Fully Integrated Scroll-Controllable Hyperchaotic Circuit

The proposed fully integrated scroll-controllable hyperchaotic system is verified using the Cadence IC Design Tools

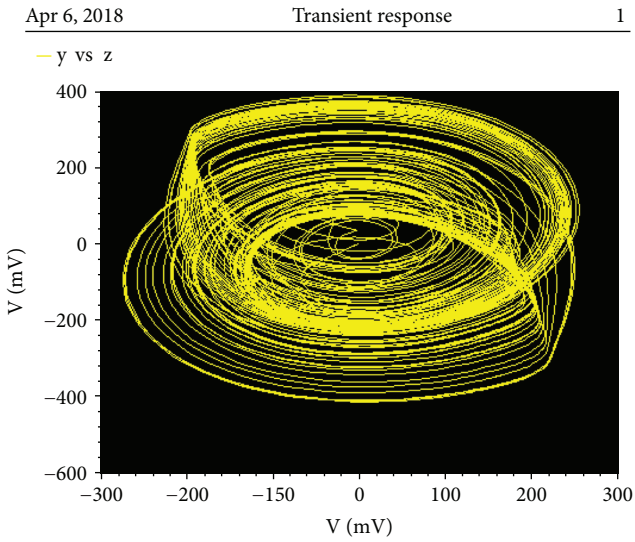

Figure 16: The phase portrait in the y-z plane (S_2 is turned on, S_1 and S_3 are turned off).

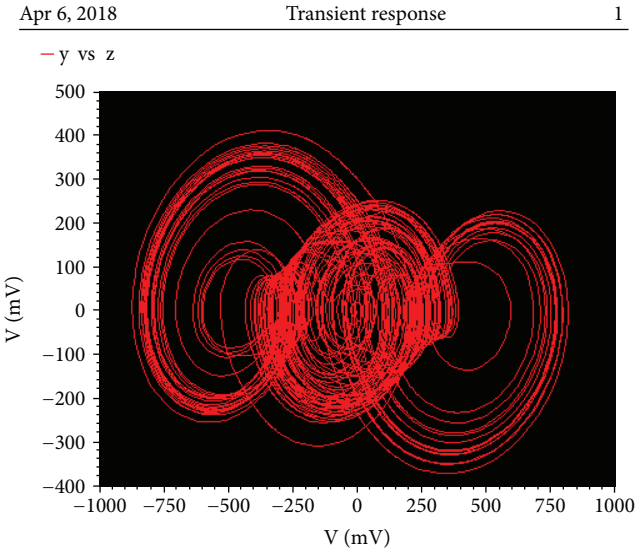

Figure 17: The phase portrait in the x-y plane (S_1 and S_3 are turned on, S_2 is turned off).

5.1.41 Spectre simulator with GlobalFoundries' 0.18 μm CMOS technology. The supply voltage of the OAs and multipliers is all ±2.5 V, and the power consumption of the whole chaotic system is about 90.5 mW. According to the standard GlobalFoundries' 0.18 μm CMOS process, there are two problems that should be considered in the full integration of chaotic circuits. First, the capacitors and inductors should not exceed 1 nF and 1 mH, because large capacitors and inductors cannot be realized in the standard integration process. Second, it is difficult to realize complex chaotic systems, because the supply voltages are very low in integrated circuits (less than 5 V).

The chip layout diagram of the chaotic oscillator is presented in Figure 13, and it takes a compact chip area of

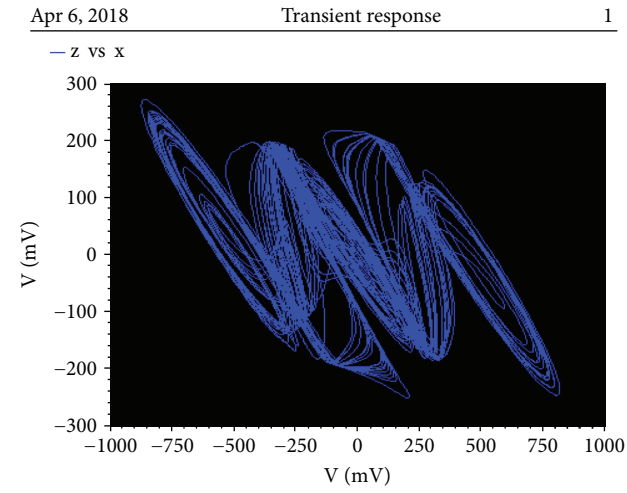

Figure 18: The phase portrait in the x-z plane (S_1 and S_3 are turned on, S_2 is turned off).

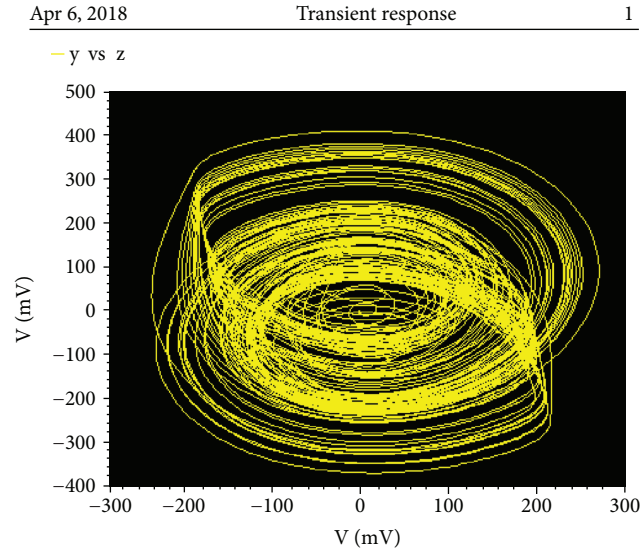

Figure 19: The phase portrait in the y-z plane (S_1 and S_3 are turned on, S_2 is turned off).

1.8 mm^2 including the testing pads. The Mentor Calibre software is used for the design rule check (DRC), layout versus schematic (LVS), and parasitic extraction (PEX) of the chaotic system. Based on the chip layout in Figure 13 and considering the parasitics extracted from the chip layout, the postlayout simulation results are presented in Figures 14–22.

When the switch S_2 is turned on, S_1 and S_3 are turned off, a single-stair nonlinear staircase function is added in the chaotic system, and the simulation results are presented in Figures 14–16.

Figures 14–16 are the phase portraits in the x-y, x-z, and y-z planes. Because the nonlinear staircase function is added in the x axis, there are two scrolls in the x-y and x-z planes and one scroll in the y-z plane.

When the switches S_1 and S_3 are turned on, S_2 is turned off and a two-stair nonlinear staircase function is added in

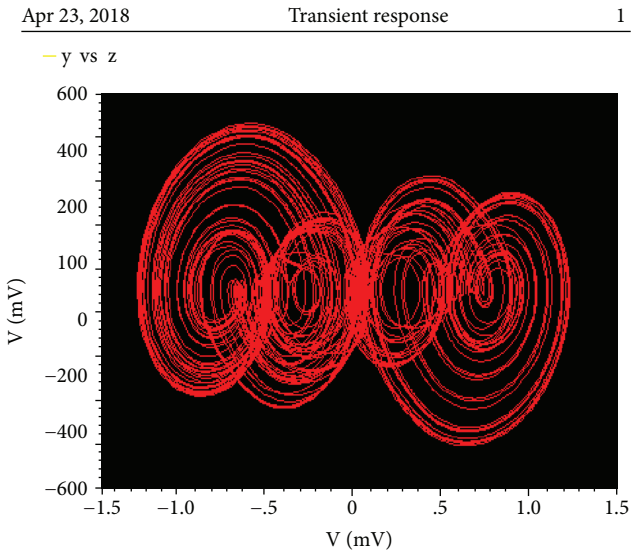

Figure 20: The phase portrait in the x-y plane (S_1, S_2, and S_3 are all turned on).

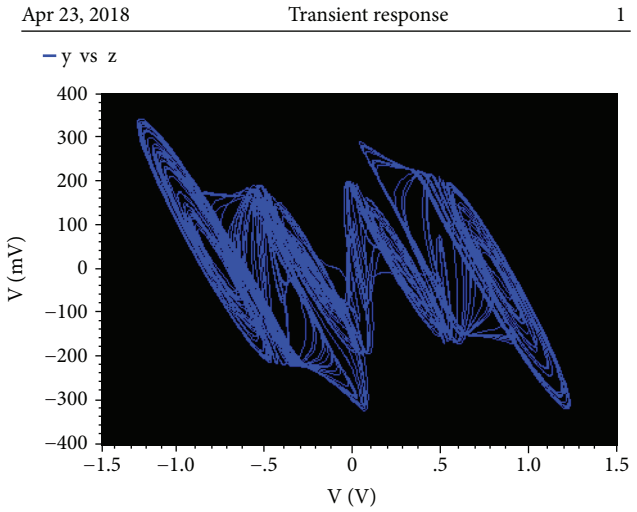

Figure 21: The phase portrait in the x-z plane (S_1, S_2, and S_3 are all turned on).

the chaotic system, and the simulation results are presented in Figures 17–19.

Figures 17–19 are the phase portraits in the x-y, x-z, and y-z planes. Similarly, the nonlinear staircase function is also added in the x axis, there are three scrolls in the x-y and x-z planes, and one scroll in the y-z plane.

When the switches S_1, S_2, and S_3 are all turned on, a three-stair nonlinear staircase function is added in the chaotic system, and the simulation results are presented in Figures 20–22.

Figures 20–22 are the phase portraits in the x-y, x-z, and y-z planes. Similarly, the nonlinear staircase function is also added in the x axis, there are four scrolls in the x-y and x-z planes, and one scroll in the y-z plane.

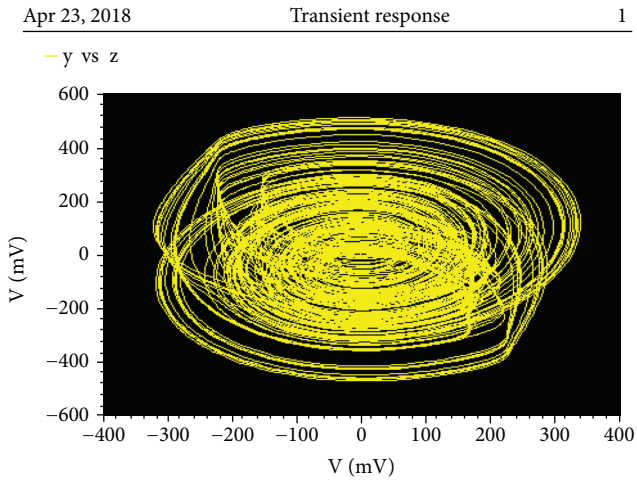

Figure 22: The phase portrait in the y-z plane (S_1, S_2, and S_3 are all turned on).

Obviously, by using programmable switches in the staircase circuit, it is easy to generate controllable scrolls in the proposed fully integrated scroll-controllable hyperchaotic system.

4. Conclusion

This work proposed a novel fully integrated memristor-based scroll-controllable hyperchaotic system. The chaotic system is verified via bifurcation diagram and Lyapunov exponents. In addition, the new chaotic system is realized using the designed OA and multiplier and simulated using Cadence IC Design Tools with the GlobalFoundries' 0.18 μm CMOS process. It is hoped that the investigation of this work will lead to more effective and systematic studies of fully integrated low-voltage and low-power chaotic circuits and enhance the practical applications of chaotic circuits.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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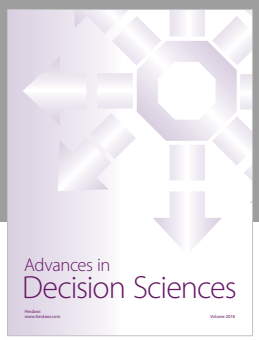

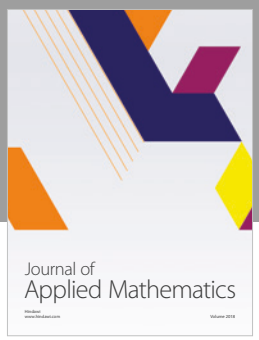

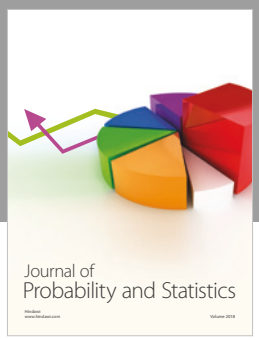

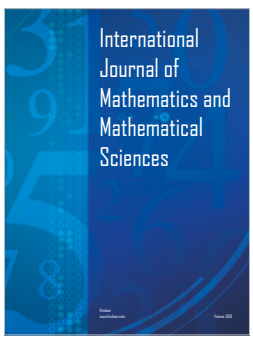

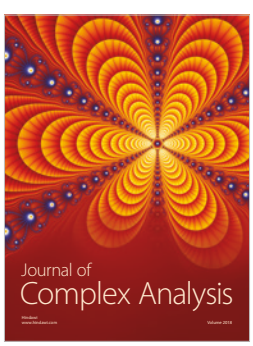

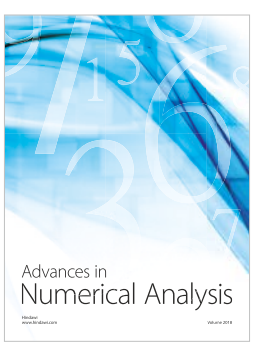

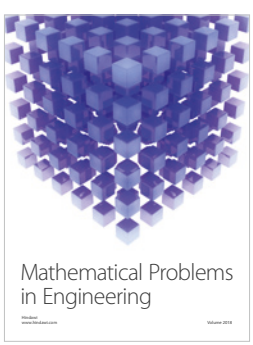

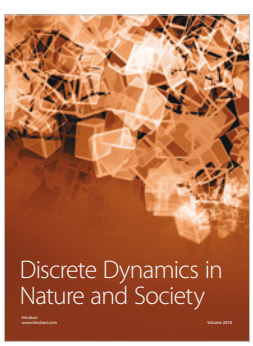

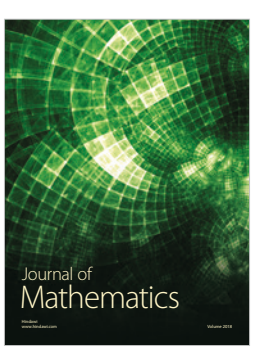

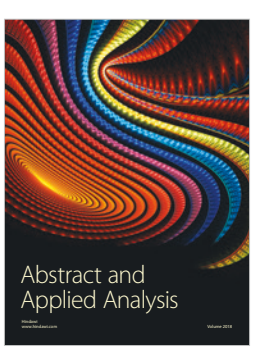

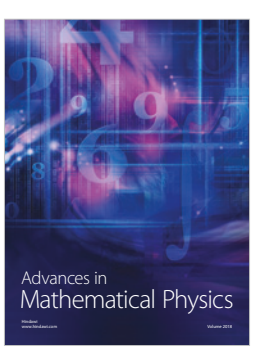

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