Research Article

Sliding Mode Controller-Based BFCL for Fault Ride-Through Performance Enhancement of DFIG-Based Wind Turbines

Mehdi Firouzi ⓘ,[1] **Mojtaba Nasiri ⓘ,**[1] **Saleh Mobayen ⓘ,**[2,3] **and G. B. Gharehpetian ⓘ**[4]

[1]*Department of Electrical Engineering, Faculty of Engineering, Abhar Branch, Islamic Azad University, Abhar, Iran*
[2]*Department of Electrical Engineering, University of Zanjan, Zanjan, Iran*
[3]*Future Technology Research Center, National Yunlin University of Science and Technology, 123 University Road, Section 3, Douliou, Yunlin 64002, Taiwan*
[4]*Electrical Engineering Department, Amirkabir University of Technology, Tehran, Iran*

Correspondence should be addressed to Mehdi Firouzi; paper_mehdi12@yahoo.com

The fault ride-through (FRT) capability and fault current issues are the main challenges in doubly fed induction generator- (DFIG-) based wind turbines (WTs). Application of the bridge-type fault current limiter (BFCL) was recognized as a promising solution to cope with these challenges. This paper proposes a nonlinear sliding mode controller (SMC) for the BFCL to enhance the FRT performance of the DFIG-based WT. This controller has robust performance in unpredicted voltage sag level and nonlinear features. Theoretical discussions, power circuit, and nonlinear control consideration of the SMC-based BFCL are conducted, and then, its performance is verified through time-domain simulations in the PSCAD/EMTDC environment. To reduce the chattering phenomenon and decrease the reaching time, it used the exponential reaching law (ERL) for designed SMC. Also, the SMC-based BFCL performance is compared with the conventional and PI controller-based BFCL for both symmetrical and asymmetrical short-circuit faults. Simulation results reveal that the SMC-based BFCL provides better performance compared with the conventional and PI controller-based BFCL to enhance the FRT.

1. Introduction

Due to the increment of energy demand and depletion of fossil fuels, the demand for electric power generations from renewable energy resources (RESs) is gradually growing [1, 2]. The electric power generation from wind energy is growing so quickly, which can be mostly credited to DFIG-based wind turbines (WTs) due to some advantages such as using partial converter ratings (25–30%) of the nominal-rated wind generator, decoupled active and reactive power control, variable speed operation, low cost, and weight [3]. However, under grid fault conditions, the stator current increases due to the direct connection of the DFIG stator windings to the grid. It results in the transient rotor overcurrent and DC-link overvoltage due to magnetically coupling of the stator and rotor circuit. This may lead to damage in the rotor-side converter (RSC) of the DFIG and disconnecting from the grid [4, 5]. This

contrasts with the fault ride-through (FRT) requirement. This requirement states that the WTs must stay connected when the connecting point voltage remains above limit line 1, as shown Figure 1. Also, in the above limit line 2, all WTs should be able to experience a fault without disconnection [6].

In the literature, several approaches including software [7–12] and hardware [13–32] methods have been proposed and documented. The software approaches such as robust control [7], virtual damping flux-based control [8], inductance-emulating control [9], scaled current tracking control [10], and sliding mode control [11, 12] are based on the modification of the RSC control system, which has low cost. They can satisfy the FRT requirements under low voltage sag but cannot guarantee the FRT under severe voltage sag and limit fault current. Therefore, it is necessary to apply hardware approaches to meet the FRT requirements under severe voltage sag [13, 14].
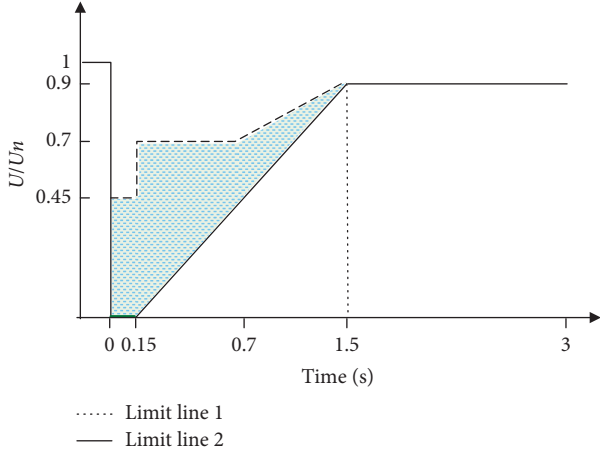
FIGURE 1: LVRT curve of the E.ON grid code.

In the literature, several hardware schemes such as application of the static synchronous compensator (STATCOM) [15], dynamic voltage restorer (DVR) [16, 17], unified interphase power controller (UIPC) [18], series dynamic resistor (SDR) [19, 20], energy storage system (ESS) [21], and fault current limiters (FCLs) [22–33] have been reported and documented. Since the most common cause of voltage drop is short-circuit fault in the downstream of the grid, many researchers are currently studying fault current mitigation techniques to reduce the voltage sag and enhance the WT FRT performance [22–24]. From this perspective, the applications of FCLs are getting more attention to meet the FRT requirements under voltage sag conditions [22–33]. Regarding this background, some studies focus on superconducting-type FCLs (SFCLs) [24–27] and bridge-type FCLs (BFCLs) [28–33]. In [24, 25], the application of the resistive-type SFCL has been suggested for FRT performance enhancement of the DFIG-based WT. In [24], scholars proposed the resistive-type SFCL in the DFIG rotor circuit to mitigate the RSC transient overcurrent and the DC-link overvoltage to meet the FRT. In [26, 27], the active-type SFCL and a flux coupling-type SFCL are proposed to enhance the DFIG FRT performance under grid fault condition. The research results confirm that SFCLs offer a promising solution to meet the FRT requirements of the DFIGs. However, they require high construction cost.

In [28], the BFCL with a discharging resistor in the DC side is used to enhance the FRT performance for the first time. In [29, 30], scholars have changed the BFCL configuration by inserting the discharging resistor in the AC side of the BFCL as the limiting impedance to enhance the FRT performance of the DFIG. From this view, BFCLs with different limiting impedances from the ones used in [28] have been proposed. In [31], a parallel resonance circuit is used as the limiting impedance instead of the discharging resistor to enhance the FRT performance of the DFIG. Kartijkolaie et al. and Firouzi and Gharehpetian [32, 33] proposed a capacitor as the limiting impedance to provide the reactive power for supporting the DFIG terminal voltage under fault condition.

In all of them, the BFCL inserts the limiting impedance in the fault path to reduce the voltage sag at the coupling point

voltage for FRT enhancement under fault conditions. However, the power system has dynamic nonlinear characteristics, especially under fault conditions. Furthermore, the connection of DFIG-based WTs by the nonlinear power electronic converters makes it more nonlinear [17]. Therefore, the integration of a nonlinear controller to the BFCL instead of the conventional linear controllers can enhance the FRT performance of the DFIG under fault conditions. Considering this matter, this paper presents a sliding mode controller- (SMC-) based BFCL to enhance the FRT performance of the DFIG. To achieve this, a nonlinear SMC is designed and implemented to the BFCL to enhance the FRT response of the DFIG under grid fault condition. The efficiency of the SMC-based BFCL is verified by time-domain simulations in the PSCAD/EMTDC software environment. Also, the FRT performance of the SMC-based BFCL is compared with the conventional and PI controller-based BFCL under both symmetrical and asymmetrical short-circuit faults.

2. DFIG-Based Wind Turbine Model

Figure 2(a) shows the schematic diagram of the DFIG-based wind turbine. The wind turbine, drive train, generator model, and its controller are the main parts of the DFIG-based WT and are modelled as follows.

2.1. Aerodynamic Modeling of the Wind Turbine. There are two wind turbine models in the master library of PSCAD/ EMTDC software. In this study, the mode 2 wind turbine model is used. In this model, the captured mechanical power (P_m) from the conversed wind power is expressed by the following equation [34]:

$$P_m = 0.5 \, \pi \, \rho \, R^2 C_p \left(\lambda, \beta\right) V_w, \tag{1}$$

where ρ, R, and V_w represent the air density, radius of blades, and wind speed, respectively. C_p is the power coefficient and is expressed by

$$C_p \left(\lambda, \beta\right) = 0.22 \left(\frac{116}{\lambda_c} - 0.4\beta - 5\right) e^{-12.5\lambda_c}, \tag{2}$$

$$\lambda_c = \frac{1}{\left(\left(1/\left(\lambda + 0.08\beta\right)\right) - \left(0.035/\left(\beta^3 - 1\right)\right)\right)}, \tag{3}$$

where λ and β are the tip speed ratio and pitch angle, respectively. Also, the drive train model used in this study is based on the commonly two-mass model [35] as demonstrated in Figure 2(b), which is described by the following:

$$
\begin{bmatrix} \dot{\omega}_g \\ \dot{\omega}_t \\ \dot{\delta}_{tg} \end{bmatrix} =
\begin{bmatrix} \dfrac{D_{tg}}{2H_g} & \dfrac{-D_{tg}}{2H_g} & \dfrac{K_{tg}}{2H_g} \\[2mm] \dfrac{D_{tg}}{2H_t} & \dfrac{-D_{tg}}{2H_t} & \dfrac{-K_{tg}}{2H_t} \\[2mm] -1 & 1 & 0 \end{bmatrix}
\begin{bmatrix} \omega_g \\ \omega_t \\ \delta_{tg} \end{bmatrix} +
\begin{bmatrix} \dfrac{-1}{2H_g} & 0 & 0 \\[2mm] 0 & \dfrac{1}{2H_t} & 0 \\[2mm] 0 & 0 & 0 \end{bmatrix}
\begin{bmatrix} T_g \\ T_t \\ 0 \end{bmatrix},
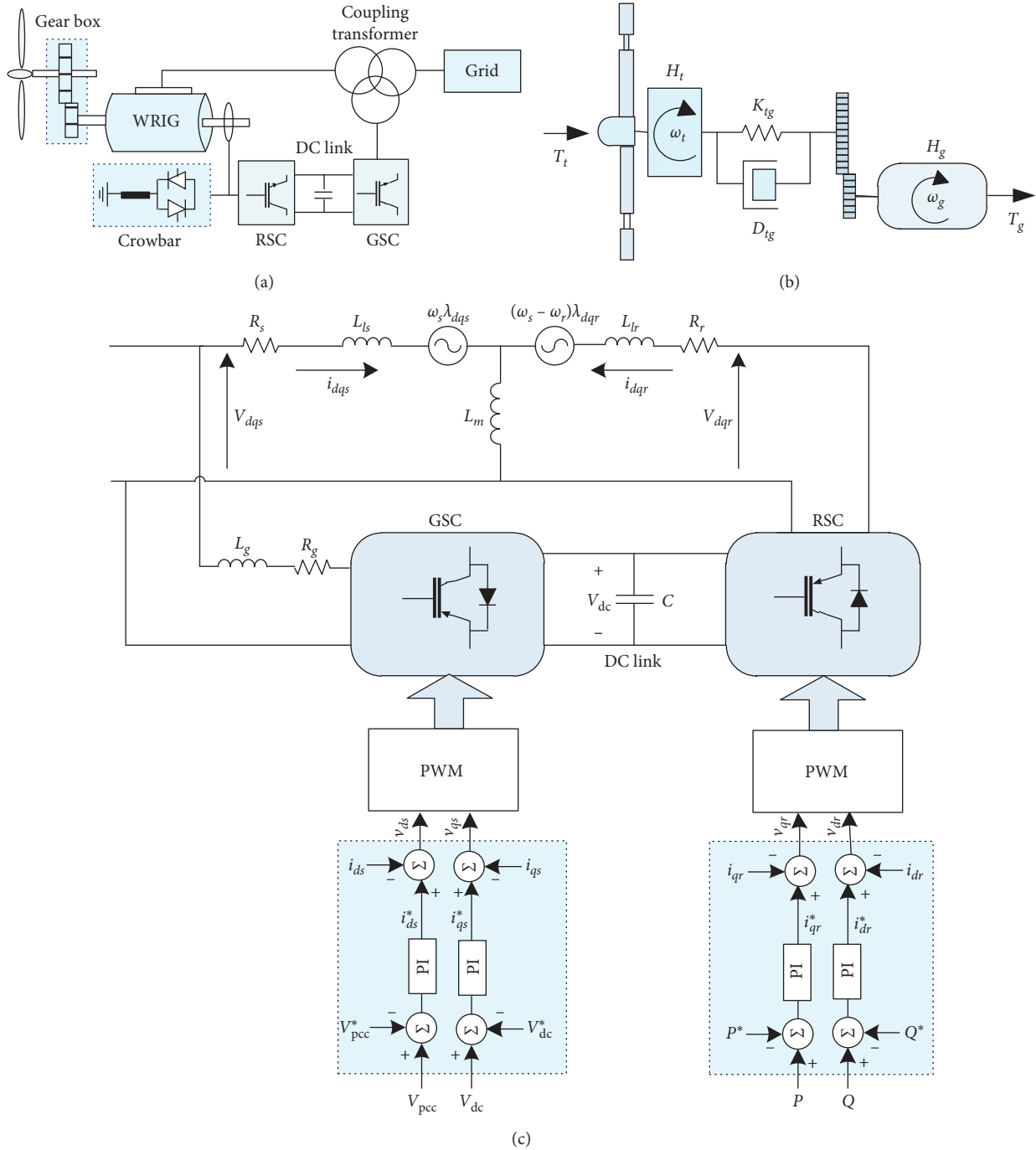$$

$$\tag{4}$$

(a)

(b)

(c)

FIGURE 2: (a) Schematic diagram of the DFIG-based wind turbine, (b) two-mass drive train system, and (c) equivalent power circuit of the DFIG and its controller.

where T_t and T_g are the mechanical turbine and electromagnetic generator torque, respectively, H_t and H_g are the equivalent turbine-blade and the generator inertia, respectively, ω_t and ω_g are the turbine and the generator angular speed, respectively, and K_{tg}, D_{tg}, and δ_{tg} are the shaft stiffness, the damping constant, and the angular displacement between two ends of the shaft, respectively [34, 35].

2.2. DFIG Model and Control System. As demonstrated in Figure 2(a), the DFIG consists of the wounded rotor induction generator (WRIG), the rotor-side converter (RSC), DC link, and grid-side converter (GSC). Considering the equivalent circuit of the DFIG as depicted in Figure 2(c) and using the *dq* synchronous reference frame, the *d-q* components of the voltage and flux equations of the DFIG are expressed as follows [7]:

$$V_{dqs} = R_s i_{dqs} + \frac{d\lambda_{dqs}}{dt} - \omega_s \lambda_{dqs}, \tag{5}$$

$$V_{dqr} = R_r i_{qr\,dqr} + \frac{d\lambda_{dqr}}{dt} - (\omega_s - \omega_r)\lambda_{dqr}, \tag{6}$$

$$\lambda_{dqs} = L_s i_{dqs} + L_m i_{dqs}, \tag{7}$$

$$\lambda_{dqr} = L_s i_{dqr} + L_m i_{dqr}, \tag{8}$$

where $L_s = L_s L_m/(L_s + L_m)$ and $L_r = L_r L_m/(L_r + L_m)$. i_{dqs} and i_{dqr} are the d-q components of the stator and rotor currents. ω_s and ω_r are the supply and rotor angular frequencies, respectively. Also, the GSC and DC link dynamic equations are expressed as follows:

$$V_{dqs} = V_{dqg} + R_g i_{dqg} + L_g \frac{d\lambda_{dqg}}{dt} + \omega_s L_g i_{dqg}, \tag{9}$$

$$V_{dc} i_{dc} = P_g - P_r - P_{\text{loss}}. \tag{10}$$

In this case, P_g and Q_g are

$$P_g = \frac{3}{2}\left(V_{qg} i_{qg} + V_{dg} i_{dg}\right), \tag{11}$$

$$P_r = \frac{3}{2}\left(V_{qr} i_{qr} + V_{dr} i_{dr}\right). \tag{12}$$

In addition, the active and reactive output power of the DFIG is defined as follows:

$$P_S = \frac{3}{2}\left(V_{qs} i_{qs} + V_{ds} i_{ds}\right) = -\frac{3}{2}\left(\frac{L_m}{L_S}V_{qs} i_{qr}\right), \tag{13}$$

$$Q_S = \frac{3}{2}\left(V_{qs} i_{ds} - V_{ds} i_{qs}\right) = \frac{3}{2}\frac{L_m}{L_S}V_{qs}\left(i_{ms} - i_{dr}\right). \tag{14}$$

Figure 2(c) demonstrates the control system of the DFIG under steady-state condition. The main objective of the RSC is controlling the output active power (P_s) and reactive power (Q_s) by regulating q- and d-axis components of the rotor currents (i.e., i_{qr} and i_{dr}), respectively. To achieve this capability, the GSC regulates the DC link and coupling point voltage in the reference values by controlling the q- and d-axis components of the stator currents (i.e., i_{qs} and i_{ds}), respectively.

3. SMC-Based BFCL

In [28], the application of the BFCL is proposed to enhance the FRT performance of the wind turbine for the first time. In this structure, the limiting resistor is configured in the DC side of the BFCL. It can control the DC reactor current to regulate the PCC voltage. In this paper, a SMC is implemented to the BFCL to regulate the terminal voltage at the determined value for different voltage sag levels by controlling the DC reactor current. The power circuit, principle operation, and designing of SMC for the BFCL are described as follows.

3.1. BFCL Power Circuit. The power circuit of the BFCL is illustrated in Figure 3. It includes the following elements:

(1) A three-phase bridge rectifier including diodes D_1–D_6

(2) An IGBT switch, which is represented by T to switch the limiting resistor

(3) A DC reactor L_D to limit the rate of increasing of fault current and di/dt

(4) A limiting resistor (R)

(5) Three single-phase series coupling transformers (T_a, T_b, and T_c)

3.2. Principle Operation of the BFCL. Based on the situation of the IGBT switch, two paths, low impedance path (LIP) and high impedance path (HIP), are provided to carry the normal and fault operation mode currents. Figure 3(b) demonstrates the line and DC reactor currents under normal and fault operation modes. The LIP consists of L_D-r_D-T path to carry the normal operation mode current, and the HIP consists of L_D-r_D-R path to carry the fault operation mode current. Under the normal operation mode ($t < t_0$), the control system of the BFCL closes T. The line current (i_L) converts to DC current (i_d) and flows through the LIP. Figure 3(c) demonstrates the DC reactor current path in this mode. In this condition, the BFCL generates some power losses and voltage drop due to the BFCL switches and DC reactor resistance, which are negligible. When a fault occurs, the line current and subsequently the DC reactor current start to increase. Figure 3(c) demonstrates the DC reactor current path in this mode ($t_0 < t < t_1$). When the DC reactor current reaches to i_1, the control system of the BFCL opens T to insert the limiting resistor in the fault path. In this condition ($t > t_1$), i_d flows through the HIP. Therefore, i_d and subsequently i_L are limited under fault condition [36–39].

3.3. PI and Conventional Controller-Based BFCL. In the conventional control approach of the BFCL, the PCC voltage is used as a control signal. Figure 4(a) demonstrates the conventional control system of the BFCL. Under the steady-state operation of the system $V_{\text{PCC}} > V_{\text{TH}}$, T is turned on, and the LIP carries the line current. When $V_{\text{PCC}} < V_{\text{TH}}$, T is turned off to force the fault current towards the HIP and limits the fault current.

Figure 4(b) demonstrates the PI control system of the BFCL. In this approach, the PI controller is used to regulate the terminal voltage at the reference value.

3.4. Design and Implementation of the SMC to the BFCL. In recent years, nonlinear controllers due to their good performances in parametric uncertainties and unmodeled dynamics are extended. One of the main powerful controllers is SMC which has a robust performance for unmodeled and noisy systems [40–43]. Consider the single input-single output system by the following state equation:
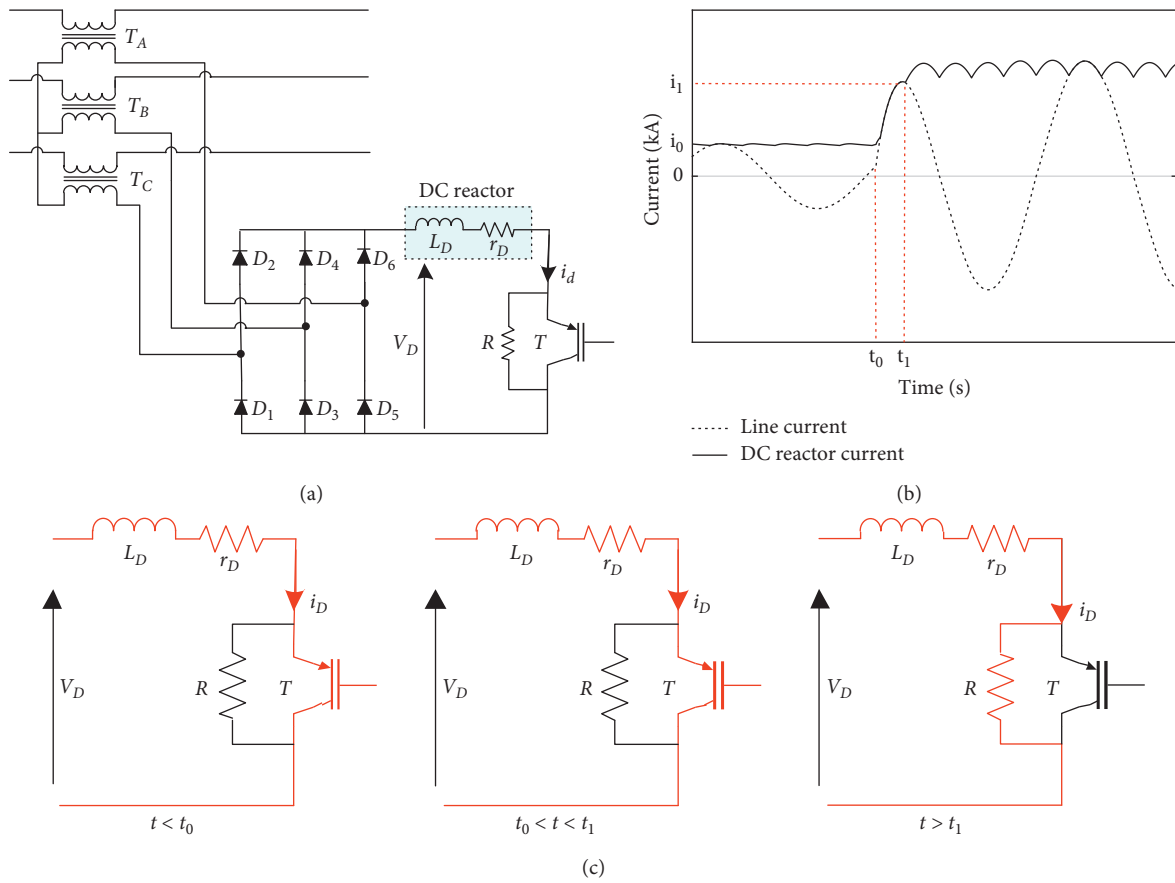
(a)

(b)

(c)

FIGURE 3: (a) Power circuit of the BFCL, (b) BFCL performance under fault condition, and (c) equivalent circuit of the BFCL under normal and fault operation modes.
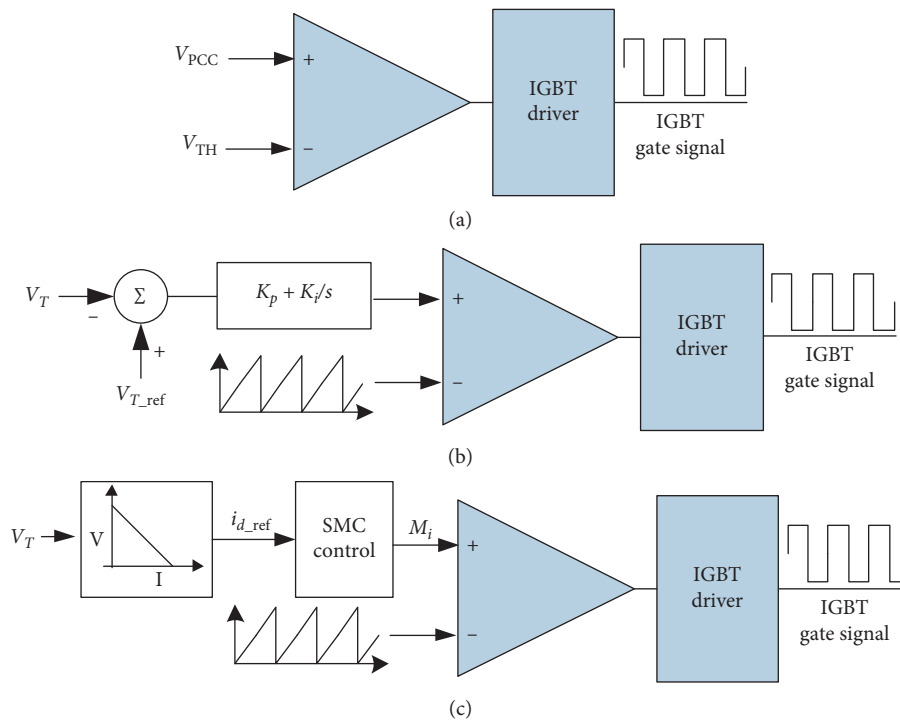

(a)

(b)

(c)

FIGURE 4: Different control systems of the BFCL: (a) the conventional voltage control, (b) PI control, and (c) SMC control.

$$\dot{x} = f(x) + b(x)u, \tag{15}$$

where x and u are the state variable and system input, respectively. $f(x)$ and $b(x)$ are bounded nonlinear functions of state variables. Let $\tilde{x} = x - x_d$ be the trajectory error in state x. The time-varying sliding surface for the system is chosen as

$$s(x;t) = \left(\frac{\mathrm{d}}{\mathrm{d}t} + \Lambda\right)^{n-1}\tilde{x}, \tag{16}$$

where Λ is a strictly positive constant and n is the order of the system. By satisfying the following term, the trajectories of the system are remained in the sliding surface:

$$\frac{1}{2}\frac{\mathrm{d}}{\mathrm{d}t}s^2 \leq -\mu|s|, \tag{17}$$

where μ is strictly positive. The above equation can be rewritten as follows:

$$s\dot{s} \leq 0. \tag{18}$$

According to (17), the reaching time will be as follows:

$$t_{\text{reach}} \leq \frac{|s(t=0)|}{\eta}, \tag{19}$$

where t_{reach} is the reaching time. To satisfying (17), generally, $\dot{s}$ is considered as follows:

$$\dot{s} = -K\text{sign}(s), \tag{20}$$

where K is the positive constant. In [42], to decrease the reaching time and the chattering phenomenon in the input controller, the variable gain was used which was known as the exponential reaching law (ERL). Hence, according to Firouzi et al. [43], (16) can be rewritten as

$$\dot{s} = -\frac{K}{D(s)}\text{sign}(s), \tag{21}$$

where

$$D(s) = \alpha + (1-\alpha)e^{-\beta|s|}, \tag{22}$$

where $0 < \alpha < 1$, $0 < \beta$. Hence, the reaching time will reduce to the following term:

$$t_{\text{reach}} \leq \frac{1}{K}\left(\alpha|s(t=0)| + \frac{(1-\alpha)}{\beta}\left[1 - e^{-\beta|s(t=0)|}\right]\right). \tag{23}$$

In order to design the BFCL controller, the average model of the system is used. By using Kirchhoff's voltage law (KVL) in the DC side of the BFCL circuit, it can be written for each phase the following equation:

$$V_d = R_D i_d + L_D \dot{i}_d, \tag{24}$$

where i_d is the reactor DC current, V_d is the DC side voltage. It should be note that the value of R_D can be varied by the value of the modulation index (M_i). Hence, M_i can be defined as follows:

$$M_i = \frac{R_D}{R}. \tag{25}$$

By inserting (25) in (24), (24) can be rewritten as follows:

$$i_d = \frac{1}{L_D}(V_d - M_i R i_d). \tag{26}$$

The sliding surface of the DC-link current of the BFCL is defined as

$$s = i_d^{\text{ref}} - i_d. \tag{27}$$

By taking the time derivative of (27), it becomes

$$\dot{s} = \dot{i}_d^{\text{ref}} - \dot{i}_d. \tag{28}$$

To eliminate the tracking error, the sliding surface and time derivative of it must be zero. Hence, it can be written as

$$M_i = \frac{V_d \dot{i}_d^{\text{ref}} L_D}{R i_d} - \frac{K}{D(s)}\text{sign}(s). \tag{29}$$

Stability proof: to prove the stability of the controller, (14) should be satisfied. Hence, by using (27)–(29), (14) will be satisfied as follows:

$$-\frac{K}{D(s)}\text{sign}(s)s \leq 0. \tag{30}$$

It shows that the designed controller is stable. To provide the T gate signal, the modulation index (M_i) obtained from (29) is compared with the triangular signal. The triangular frequency is set to be 1 kHz as shown in Figure 4(c).

3.5. DC Reactor Design.

The main purpose of using the DC reactor in the BFCL circuit is limiting the rate of increase of fault current before fault detection time. The cost and inductance of the DC reactor are decisive factors. High value of the DC reactor inductance results in high power losses and cost, which are not acceptable. However, the inductance value of the DC reactor should be sufficient to achieve this purpose. Considering Figure 3(c), which presents the equivalent circuit during $t_0 < t < t_1$ time, the DC reactor current is approximately given by the following equation:

$$V_D = ri + L\frac{\mathrm{d}i}{\mathrm{d}t}, \tag{31}$$

where $r = r_D$ and $L = L_D$. Considering (t_1-t_0) as the necessary time for increasing fault current from i_0 to i_1 and solving (31), the inductance value of the DC reactor is obtained by the following equation:

$$L_D = \frac{r_D}{(t_1 - t_0)}\ln\left(\frac{V_D - ri_0}{V_D - ri_1}\right). \tag{32}$$

V_D is the mean value of the source voltage on the DC side of the bridge circuit and is approximately as follows:

$$V_D = \frac{3\sqrt{3}AV_m}{\pi}, \tag{33}$$

where V_m is the magnitude of the source voltage. Furthermore, by determining t_1 and i_1, the DC reactor inductance is designed.
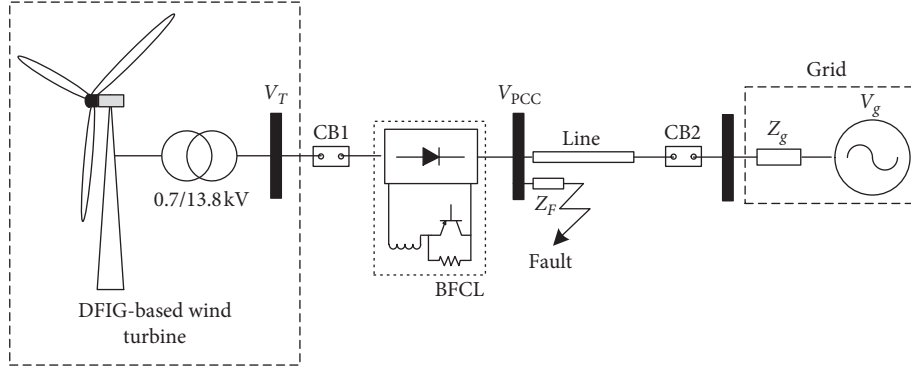
FIGURE 5: Study system.

3.6. Limiting Resistance Design. When a fault occurs, the BFCL inserts the limiting resistor (R_D) in the fault path to dissipate the excess output active power of the DFIG (P_G) during the fault. To make sure the least disturbance reaches to the DFIG during the fault, R_D should be sufficient to dissipate the active power transferred by the faulted line. Therefore, the active power dissipated by the BFCL (P_D) should be equal with P_G during the fault. P_D is determined as follows:

$$P_D = \frac{V_{pcc}^2}{R_D} = P_G. \tag{34}$$

Using (34), the minimum value of R_D can be derived as follows:

$$R_D = \frac{V_{pcc}^2}{P_G}. \tag{35}$$

4. Simulation and Discussion

To verify the proposed SMC-based BFCL performance, the system shown in Figure 5 is used. It includes a 2 MW DFIG-based wind turbine, which is connected to the main grid through a step-up 0.7 kV/13.8 kV transformer. Both symmetrical three-line-to-ground (3LG) and asymmetrical single-line-to-ground (SLG) short-circuit faults were applied at the PCC bus to evaluate the capability of the proposed SMC-based BFCL. The simulated system and DFIG parameters are illustrated in Table 1. Both short-circuit faults occur at $t = 10$s and continue for 150 ms. V_T represents the terminal voltage in Figure 5. Simulations were performed for the following cases:

Case A: using the conventional-controller BFCL

Case B: using the PI-controller BFCL

Case C: using the sliding mode controller BFCL

4.1. Symmetrical 3LG Fault Condition. Figure 6 demonstrates the performance of the BFCL for three cases under 3LG fault condition. In this condition, the PCC voltage drops to zero, approximately. As demonstrated in Figure 6(a), the BFCL performances in three cases have the

TABLE 1: Simulated system parameters.

	Parameters	Value
Grid	Grid voltage	13.8 kV
	Grid frequency	50 Hz
	X/R ratio	5
Induction generator	Rated active power	2 MW
	Rated voltage	690 V
	Rated frequency	50 Hz
	Inertia constant	1 s
	Stator resistance	0.0057 Ω
	Stator leakage reactance	0.078 Ω
	Rotor resistance	0.0159 Ω
	Rotor leakage reactance	0.1022 Ω
	Mutual reactance	2.434 Ω
BFCL	DC reactor inductance	0.01 H
	Limiting resistance	R 100 Ω

same trend in response to severe voltage sag. However, the SMC-controlled BFCL has the lowest voltage sag and oscillation in the fault period. Figure 6(b) demonstrates the DFIG active power for three cases. In cases A and B, the active power drops to 0.8 pu in the fault period, approximately. Also, it is increased to 1.5 pu after fault clearance in case A. However, it has the lowest fluctuation in case C by using the SMC-controlled BFCL. Figure 6(c) demonstrates the DFIG speed under this condition. It demonstrates the least rotor speed deviation for case C. Figure 6(d) demonstrates the DC link voltage of the DFIG under this condition. It can be seen from this figure that the DC link voltage remains constant during and after fault by using the SMC-controlled BFCL.

Figure 7 demonstrates the DFIG stator current under this condition. It can be seen from this figure that the fault current is limited in 0.4 pu. In cases B and C, the fault current is 0.5 pu, and they have the same trend. However, the SMC-controlled BFCL has superior performance in both ends of the fault period.

4.2. Asymmetrical SLG Fault Condition. Figure 8 demonstrates the performance of the BFCL for three cases under 1LG fault condition. As demonstrated in Figure 8(a), the PCC voltage drops to 0.75 pu for this condition. In case A, the terminal voltage of the DFIG is increased to 1.4 pu in the
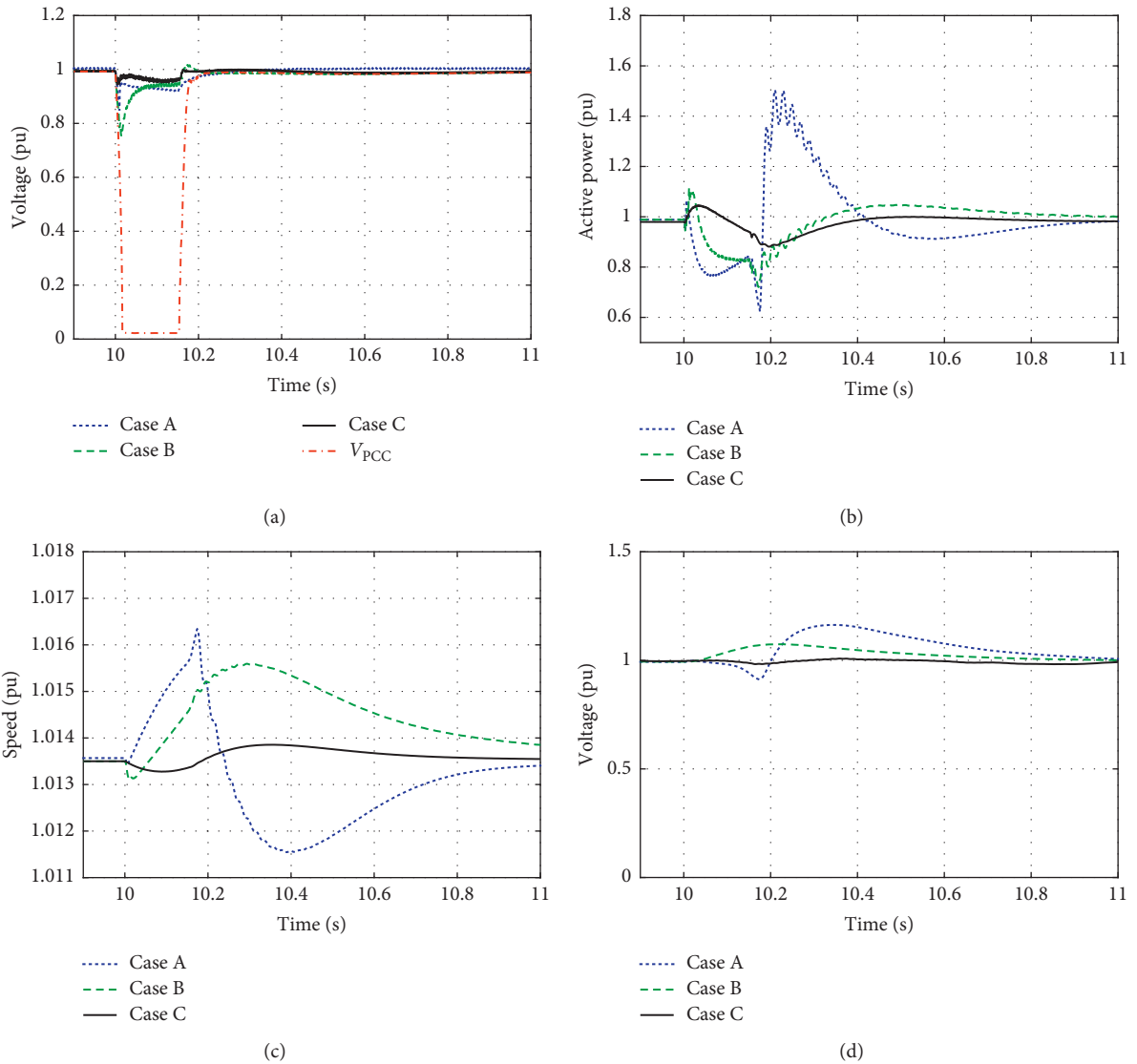
(a)

(b)

(c)

(d)

FIGURE 6: WT response under the 3LG fault: (a) DFIG terminal voltage, (b) DFIG active power, (c) DFIG rotor speed, and (d) DC link voltage.

(a)

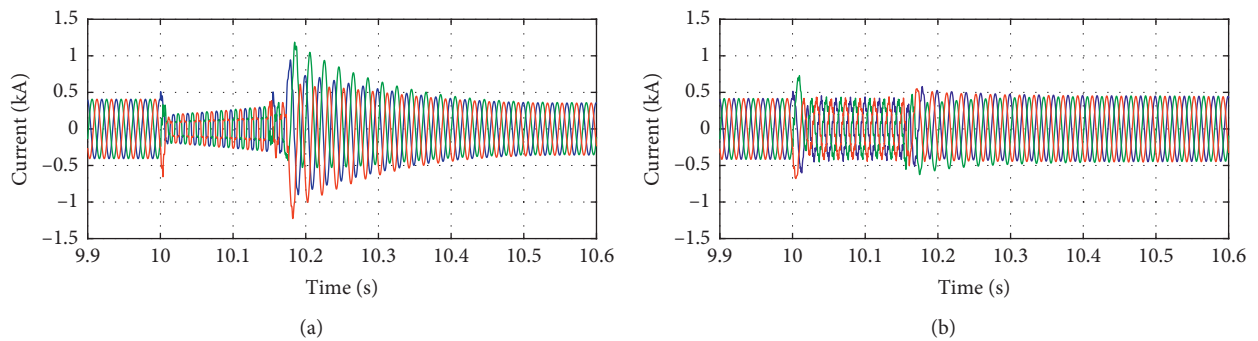(b)

FIGURE 7: Continued.

(c)

FIGURE 7: DFIG fault current under the 3LG fault: (a) Case A, (b) Case B, and (c) Case C.

(a)

(b)

(c)

(d)

FIGURE 8: WT response under the 1LG fault: (a) DFIG terminal voltage, (b) DFIG active power, (c) DFIG rotor speed, and (d) DC link voltage.

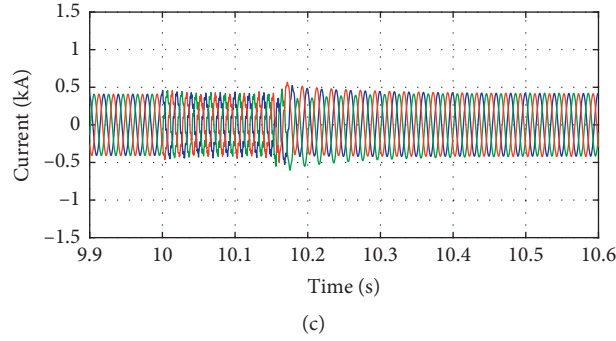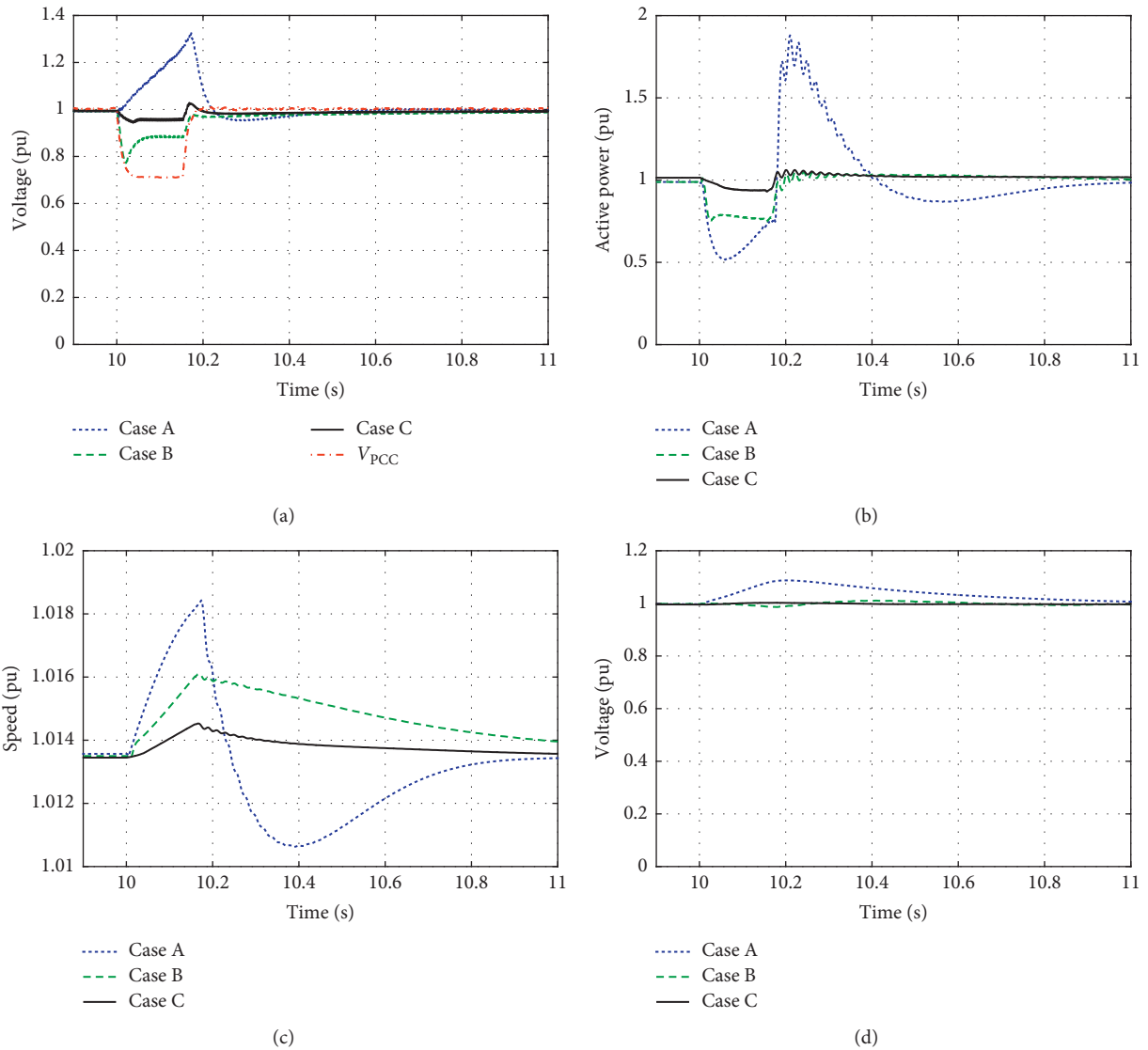end of the fault period. In case B, the PI control of the BFCL cannot control the terminal voltage at the reference value; however, it remains in acceptable voltage level. In case C, by

using the SMC-based BFCL, the terminal voltage is controlled at the reference level by controlling the DC reactor current. Figure 8(b) demonstrates the active power of the
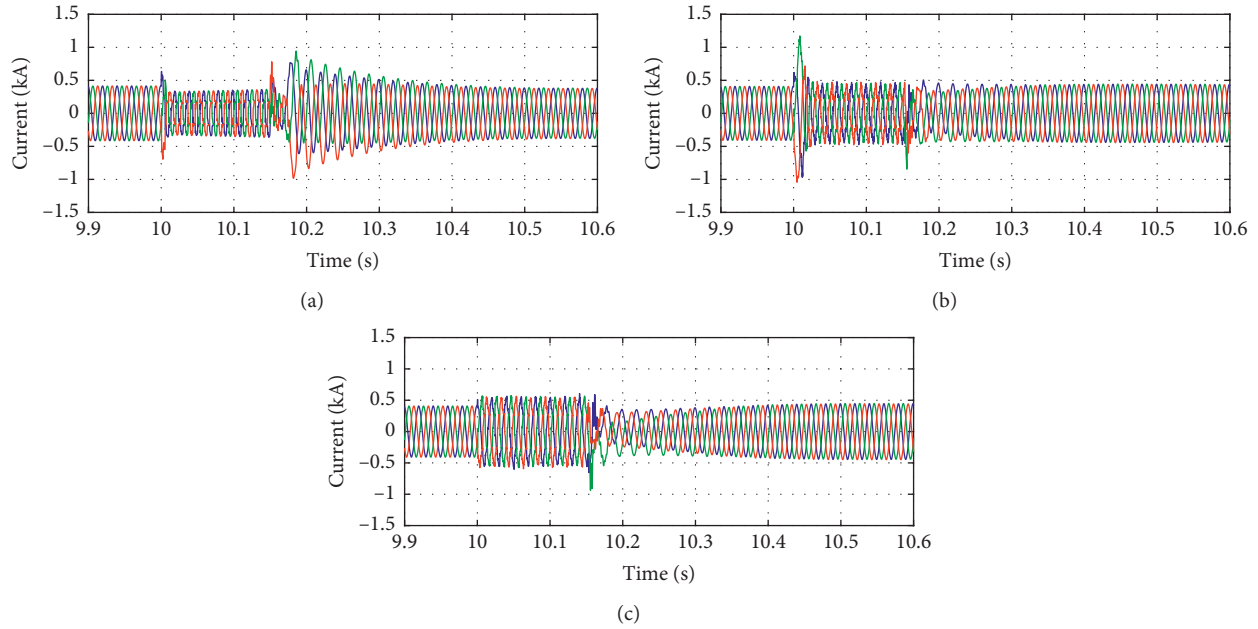
(a)

(b)

(c)

FIGURE 9: DFIG fault current under the 1LG fault: (a) Case A, (b) Case B, and (c) Case C.

DFIG in three cases. As demonstrated in this figure, the active power fluctuation is lowest in the case of using the SMC-based BFCL, which leads to the least rotor speed deviation, as demonstrated in Figure 8(c). Figure 8(d) demonstrates the DC link voltage of the DFIG. It can be seen that the DC link voltage increases to 1.1 pu for scenario A. However, in scenarios B and C, the DC link voltage remains constant.

Figure 9 demonstrates the DFIG stator current for three cases under this condition. In case A, the fault current is lower than the per-fault current due to full insertion of the limiting impedance in the fault path. In cases B and C, the fault current is limited in 0.5 pu; however, the SMC-based BFCL has superior performance under fault condition.

5. Conclusions

In this paper, a sliding mode controller has been designed to control the BFCL for enhancing the FRT capability of the DFIG-based wind turbine under severe and low voltage sag levels. The DC reactor current of the BFCL has been considered as a state variable in the SMC to control the DFIG terminal voltage. Also, to show the efficiency of the proposed SMC-based BFCL, its performance has been compared with the PI- and conventional controller-based BFCL. Based on the PSCAD/EMTDC simulation results, the following points are obtained:

(i) By using the SMC-based BFCL, the DFIG terminal voltage is effectively controlled at the reference value at different voltage sag levels. This subject leads to the lowest DFIG speed and active power deviations under voltage sag conditions.

(ii) The SMC-based BFCL limits the transient fault current in both ends of the fault period.

(iii) The SMC has a robust and efficient performance under uncertainty conditions in comparison with the PI and conventional voltage control.

Data Availability

The PSCAD file data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References

[1] M. A. El-Hameed, M. M. Elkholy, and A. A. El-Fergany, "Efficient frequency regulation in highly penetrated power systems by renewable energy sources using stochastic fractal optimiser," *IET Renewable Power Generation*, vol. 12, no. 13, pp. 2174–2183, 2019.

[2] M. Nasiri, J. Milimonfared, and S. H. Fathi, "A review of low-voltage ride-through enhancement methods for permanent magnet synchronous generator based wind turbines," *Renewable and Sustainable Energy Reviews*, vol. 47, no. 47, pp. 399–415, 2015.

[3] H. Li and Z. Chen, "Overview of different wind generator systems and their comparisons," *IET Renewable Power Generation*, vol. 2, no. 2, pp. 123–138, 2008.

[4] J. Mohammadi, S. Vaez-Zadeh, S. Afsharnia, and S. Farhangi, "Improved fault ride through strategy for doubly fed induction generator based wind turbines under both symmetrical and asymmetrical grid faults," *IET Renewable Power Generation*, vol. 10, no. 8, pp. 1114–1122, 2016.

[5] M. Firouzi, G. B. Gharehpetian, and B. Mozafari, "Power-flow control and short-circuit current limitation of wind farms

using unified interphase power controller," *IEEE Transactions on Power Delivery*, vol. 32, no. 1, pp. 62–71, 2017.

[6] M. Tsili and S. Papathanassiou, "A review of grid code technical requirements for wind farms," *IET Renewable Power Generation*, vol. 3, no. 12, pp. 308–332, 2009.

[7] R. Cardenas, R. Pena, S. Alepuz, and G. Asher, "Overview of control systems for the operation of DFIGs in wind energy applications," *IEEE Transaction Industrial Electronic*, vol. 60, no. 7, pp. 2776–2798, 2013.

[8] R. Zhu and Z. Chen, "Closure to discussion on "virtual damping flux-based LVRT control for DFIG-based wind turbine"" *IEEE Transactions on Energy Conversion*, vol. 31, no. 1, pp. 408-409, 2016.

[9] D. Zhu, X. Zou, L. Deng, Q. Huang, S. Zhou, and Y. Kang, "Inductance-emulating control for DFIG-based wind turbine to ride-through grid faults," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8514–8525, 2017.

[10] Q. Huang, X. Zou, D. Zhu, and Y. Kang, "Scaled current tracking control for doubly fed induction generator to ride-through serious grid faults," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2150–2165, 2016.

[11] M. J. Morshed and A. Fekih, "A new fault ride-through control for DFIG-based wind energy systems," *Electric Power Systems Research*, vol. 146, pp. 258–269, 2017.

[12] M. J. Morshed and A. Fekih, "Integral terminal sliding mode control to provide fault ride-through capability to a grid connected wind turbine driven DFIG," in *Proceedings of the 2015 IEEE International Conference on Industrial Technology (ICIT)*, pp. 1059–1064, Seville, Spain, March 2015.

[13] K. Goweily, M. S. El Moursi, M. Abdel-Rahman, and M. A. L. Badr, "Voltage booster scheme for enhancing the fault ride-through of wind turbines," *IET Power Electronics*, vol. 8, no. 10, pp. 1853–1863, 2015.

[14] M. Firouzi, G. B. Gharehpetian, and S. B. Mozafari, "Application of UIPC to improve power system stability and LVRT capability of SCIG-based wind farms," *IET Generation, Transmission & Distribution*, vol. 11, no. 9, pp. 2314–2322, 2017.

[15] K. S. Latha and M. V. Kumar, "STATCOM for enhancement of voltage stability of a DFIG driven wind turbine," in *Proceedings of the 2014 Power and Energy Systems: Towards Sustainable Energy*, pp. 1–5, Bangalore, India, March 2014.

[16] C. Wessels, F. Gebhardt, and F. W. Fuchs, "Fault ride-through of a DFIG wind turbine using a dynamic voltage restorer during symmetrical and asymmetrical grid faults," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 807–815, 2017.

[17] L. Yan, X. Chen, X. Zhou, H. Sun, and L. Jiang, "Perturbation compensation-based non-linear adaptive control of ESS-DVR for the LVRT capability improvement of wind farms," *IET Renewable Power Generation*, vol. 12, no. 13, pp. 2174–2183, 2018.

[18] M. Firouzi, G. B. Gharehpetian, and Y. Salami, "Active and reactive power control of wind farm for enhancement transient stability of multi-machine power system using UIPC," *IET Renewable Power Generation*, vol. 11, no. 8, pp. 1246–1252, 2017.

[19] J. Yang, J. E. Fletcher, and J. O. Reilly, "A series-dynamic-resistor-based converter protection scheme for doubly-fed induction generator during various fault conditions," *IEEE Transaction Energy Conversion*, vol. 25, no. 2, pp. 422–432, 2010.

[20] K. E. Okedu, S. M. Muyeen, R. Takahashi, and J. Tamura, "Wind farms fault ride through using DFIG with new protection scheme," *IEEE Transactions on Sustainable Energy*, vol. 3, no. 2, pp. 242–254, 2012.

[21] J. Liu, W. Yao, J. Fang, J. Wen, and S. Cheng, "Stability analysis and energy storage-based solution of wind farm during low voltage ride through," *International Journal of Electrical Power & Energy Systems*, vol. 101, pp. 75–84, 2018.

[22] Y. Salami, "Dynamic performance of wind farms with bridge-type superconducting fault current limiter in distribution grid," in *Proceedings of the 2011 2nd International Conference on Electric Power and Energy Conversion Systems (EPECS)*, pp. 1–6, Sharjah, UAE, November 2011.

[23] A. E. Naggar and I. Erlich, "Short-circuit current reduction techniques of the doubly-fed induction generator based wind turbines for fault ride through enhancement," *IET Renewable Power Generation*, vol. 11, no. 7, pp. 1033–1040, 2017.

[24] Z. Zou, X. Chen, C. Li, X. Xiao, and Y. Zhang, "Conceptual design and evaluation of a resistive-type SFCL for efficient fault ride through in a DFIG," *IEEE Transactions on Applied Superconductivity*, vol. 26, no. 1, Article ID 5600209, 2016.

[25] M. E. Elshiekh, D. E. A. Mansour, and A. M. Azmy, "Improving fault ride-through capability of DFIG-based wind turbine using superconducting fault current limiter," *IEEE Transactions on Applied Superconductivity*, vol. 23, no. 3, Article ID 5601204, 2013.

[26] L. Chen, C. Deng, F. Zheng, S. Li, Y. Liu, and Y. Liao, "Fault ride-through capability enhancement of DFIG-based wind turbine with a flux-coupling-type SFCL employed at different locations," *IEEE Transactions on Applied Superconductivity*, vol. 25, Article ID 5201505, 2015.

[27] L. Chen, F. Zheng, C. Deng, Z. Li, and F. Guo, "Fault ride-through capability improvement of DFIG-based wind turbine by employing a voltage-compensation-type active SFCL," *Canadian Journal of Electrical and Computer Engineering*, vol. 38, no. 2, pp. 132–142, 2015.

[28] M. Firouzi and G. B. Gharehpetian, "Improving fault ride-through capability of fixed-speed wind turbine by using bridge-type fault current limiter," *IEEE Transactions on Energy Conversion*, vol. 28, no. 2, pp. 361–369, 2013.

[29] G. Rashid and M. H. Ali, "Nonlinear control-based modified BFCL for LVRT capacity enhancement of DFIG based wind farm," *IEEE Transactions on Energy Conversion*, vol. 32, no. 1, pp. 284–295, 2017.

[30] G. Rashid and M. H. Ali, "Transient stability enhancement of double fed induction machine based wind generator by bridge-type fault current limiter," *IEEE Transactions on Energy Conversion*, vol. 30, no. 3, 2015.

[31] G. Rashid and M. H. Ali, "Application of parallel resonance fault current limiter for fault ride through capability augmentation of DFIG based wind farm," in *Proceedings of the 2016 IEEE/PES Transmission and Distribution Conference and Exposition (T&D)*, pp. 1–5, Dallas, TX, USA, May 2016.

[32] H. S. Kartijkolaie, M. Radmehr, and M. Firouzi, "LVRT capability enhancement of DFIG-based wind farms by using capacitive DC reactor-type fault current limiter," *International Journal of Electrical Power & Energy Systems*, vol. 102, pp. 287–295, 2018.

[33] M. Firouzi and G. B. Gharehpetian, "LVRT performance enhancement of DFIG-based wind farms by capacitive bridge-type fault current limiter," *IEEE Transactions on Sustainable Energy*, vol. 9, no. 3, pp. 1118–1125, 2018.

[34] L. M. Fernández, C. A. García, J. R. Saenz, and F. Jurado, "Equivalent models of wind farms by using aggregated wind turbines and equivalent winds," *Energy Conversion and Management*, vol. 50, no. 3, pp. 691–704, 2009.

[35] F. Mei and B. C. Pal, "Modeling of doubly fed induction generator for power system stability study," in *Proceedings of the Power and Energy Society General Meeting—Conversion and Delivery of Electrical Energy in the 21st Century*, IEEE, Pittsburgh, PA, USA, pp. 1–8, July 2008.

[36] M. Firouzi, G. B. Gharehpetian, and B. Mozafari, "Improvement of power system stability by using new switching technique in bridge-type fault current limiter," *Electric Power Components and Systems*, vol. 43, no. 2, pp. 234–244, 2014.

[37] M. Firouzi, G. B. Gharehpetian, and B. Mozafari, "Bridge-type superconducting fault current limiter effect on distance relay characteristics," *International Journal of Electrical Power & Energy Systems*, vol. 68, pp. 115–122, 2015.

[38] M. Nasiri, S. Mobayen, and Q. M. Zhu, "Super-twisting sliding mode control for gearless PMSG-based wind turbine," *Complexity*, vol. 2019, Article ID 6141607, 15 pages, 2019.

[39] M. Nasiri, J. Milimonfared, and S. H. Fathi, "Robust control of PMSG-based wind turbine under grid fault conditions," *Indian Journal of Science and Technology*, vol. 8, p. 13, 2015.

[40] S. M. Mozayan, M. Saad, H. Vahedi, H. Fortin-Blanchette, and M. Soltani, "Sliding mode control of PMSG wind turbine based on enhanced exponential reaching law," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 10, pp. 6148–6159, 2016.

[41] C. J. Fallaha, M. Saad, H. Y. Kanaan, and K. Al-Haddad, "Sliding-mode robot control with exponential reaching law," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 2, pp. 600–610, 2011.

[42] M. Firouzi, G. B. Gharehpetian, and M. Pishvaei, "THD reduction of PCC voltage by using the bridge-type FCL," *International Transactions on Electrical Energy Systems*, vol. 23, no. 5, pp. 665–668, 2013.

[43] M. Firouzi, G. B. Gharehpetian, and M. Pishvaei, "A dual-functional bridge type FCL to restore PCC voltage," *International Journal of Electrical Power & Energy Systems*, vol. 46, pp. 49–55, 2013.