Research Article

Complex Dynamics and Effects of Memristive Load Using Current-Mode-Controlled in Buck Converter

Alain Soup Tewa Kammogne (ID),[1] **Edwige Mache Kengne,**[1]
Sundarapandian Vaidyanathan (ID),[2] **Hilaire Bertrand Fotsin** (ID),[1]
and Thomas Tatietse Tamo (ID)[1]

[1]*Laboratory of Condensed Matter, Electronics and Signal Processing (LAMACETS), Department of Physic, Faculty of Sciences, University of Dschang, P.O. Box 67, Dschang, Cameroon*
[2]*Research and Development Centre, Vel Tech University, Vel Nagar, Avadi, Chennai 600 062, Tamil Nadu, India*

Correspondence should be addressed to Alain Soup Tewa Kammogne; kouaneteoua@yahoo.fr

Electronic power converters are in a state of exhibiting some complex features which can be influenced by the converter's structure parameters and load, as well as its pulse period. In this paper, we propose to investigate these phenomena occurring in the dc/dc buck converter by carrying out the dynamics of the said system when it exhibits the fingerprints of frequency-dependent pinched hysteresis loops. The essential part of this study is consecrated to the nonlinear dynamics when the converter load is memristive. Under two kinds of switch states, the independent nonlinear models and equations are derived which provide a complete dynamics description of the system under investigation. The dynamics analysis is performed by making use of bifurcation tools, phase portraits, and two parameters Lyapunov diagrams showing that the system depicts very rich and striking behaviors such as periodic orbits, period-doubling bifurcation, quasiperiodicity, chaos, and pinched hysteresis loops of the memristive load. Finally, the numerical simulation results are in almost perfect agreement with the analog result obtained with PSIM. The results obtained in this work have not yet been reported in the literature to the best of our knowledge and thus deserve dissemination.

1. Introduction

Dc/dc power converters are considered as the most vital empowering devices of electrical and electronic engineering as they act as a buffer between a power source of electronic equipment and a load [1]. These devices are used to convert an unregulated dc voltage to a regulated or variable dc output voltage by stockpiling the input energy momentarily and debit the energy to the output stage to ensure adequate current and voltage regulation. They are also known to have a significant variety of complex nonlinear behaviors such as subharmonic oscillations bifurcation phenomena that can lead to chaotic phenomena, and period-1 oscillations, due to

switching actions and feedback control. We recall that the nonlinear dynamics have been experimentally observed in different types of dc/dc buck converters where there are a series of modulation strategies, such as current-mode control [2, 3], voltage-mode control [4, 5], PWM voltage-current hybrid control [6–10], hysteresis-current or -voltage control [10, 11], one-cycle control [12, 13], and model predictive control [14–16]. Unfortunately, the nonlinear switching of power converters can put their stability at risk and make them prone to exhibit various nonlinear instable phenomena. This can have harmful effects on the converter since stability and efficiency are two fundamental criteria for the design of these converters. It is therefore imperative to

understand and establish the mechanism of formation of various complex phenomena occurring in the buck converters when the circuit parameters, circuits topologies, control schemes, and load change.

Many researchers investigated the dynamic analysis of dc/dc converters according to the system parameters and loads in the literature. Several types of load are reported such as capacitive voltage load [17–19], the linear load [20–24], and the constant current load [25, 26]. The complete dynamic of the dc/dc converter is determined by the type of the load which leads to various complex phenomena with respect to different switching modes. For the sake of brevity, we mention the chaos issue, quasiperiodicity, and some stringent behavior such as the coexistence of attractors and pulse bursting, etc (the reader is referring to References [17, 19, 27] and the references therein). Other important characteristics such as chaos transition in buck-boost [28] and hidden attractors in multilevel dc/dc converters have been investigated by Zhusubaliyeu and Wang [29], respectively. The dynamic modeling and analysis of the bidirectional dc/dc boost-buck converter for renewable energy applications were presented by Spier et al. [30], while Kamal and coworkers developed a buck-boost converter small signal model: dynamic analysis under system uncertainties [31]. Recently, the study of complex dynamics in dc/dc boost converter with dspace-based real-time controller is presented by Ghosh et al. [32]. Another relevant work is proposed by Mandal et al. in which the modeling and analysis of complex dynamics for dspace controlled closed-loop dc/dc boost converter is investigated. Despite extensive investigations on the complex behavior of the basic dc/dc topology converters over the past decade [33], such phenomena in the resonant dc/dc converters with memristive load issues remain largely unexplored in the buck converter which still remains challenging and thus deserves more dissemination.

Motivated by the pioneer works of Zhang and Bao dealing with the dynamical behaviors and circuit experiments of the switching dc/dc boost converter have been efficiently studied [34]. In addition, the dynamical effects of memristive load on peak current mode buck-boosts witching converter have been considered [35] which shows that the memristors can be applied to create very complex dynamics (rich texts are provided in References [36, 37]). Due to various applications of this device, it is very important to demonstrate that the current-mode-controlled buck converter with memristance load has a large impact on the exhibited nonlinear dynamics such as chaotic and subharmonic oscillations. We then investigate in this paper the nonlinear dynamical behaviors, i.e., chaotic and subharmonic oscillations, of the dc/dc buck converter with memristance load by numerical simulations and PSIM circuit analysis.

The rest of the paper is organized as follows. In Section 2, the circuit topology and fundamental operating principle of the current-mode-controlled dc/dc buck converter are introduced, respectively. Section 3 presents the system equations and their dimensionless forms based on the schematic of the buck converter with memristance load. We discuss the equilibrium points of these dimensionless circuit systems and their stability in Section 4. Section 5 is devoted to the forming mechanism of the chaotic and subharmonic dynamics through numerical simulations. Furthermore, the PSIM circuit topology is designed and the results are in perfect agreement with the numerical plots in Section 6. Finally, some conclusions are drawn in Section 7.

2. Background and System Description

In this section, we present a basic knowledge on the dc/dc buck converter with a memristive load. Before designing and analyzing the circuit system, it is necessary to mention that, so far, various dc/dc power converters with resistance load have been predominantly studied, with different types of converters such as boost, buck-boost, and buck converters. The single-stage buck converter presents some specific design details on the dynamics which is highly interesting to investigate in behavior when the load is memristive, as presented in Figure 1.

3. dc/dc Single-Stage Buck Converter

A single dc/dc buck power converter under investigation is presented in Figure 1. The inductor and capacitor stand as energy storage elements, two semiconductors such as diode and the switch ensures two conduction modes of the circuit, the current-mode-controlled feedback loop consists of a comparator U and an RS trigger, and the load which can be regarded as a memristive load. Let us denote the reference current as I_{ref} and the current through inductor L by I. The fundamental operation of a buck converter consists of two distinct states (i.e., ON-state and OFF-state), which can be described as in (Table 1).

In summary, the states of the buck converter are controlled by the switch S. As long as the switch S is neither on nor off, both ON-state and OFF-state occur in a switching period. From the circuit of Figure 1, it is not obvious to obtain the link between the switching period T_s and the pulse period T of the clock; their ratio depends strongly on the dynamical behaviors of the buck converter. This measuring element remains fixed or variable when the buck converter is periodic or quasiperiodic, respectively.

3.1. Modeling of the Memristor. Memristor is commonly known as the fourth key circuit element, first introduced by Chua in 1971 [38]. In exact terms, memristor has an elegant effect to memorize the past quantity of electric charge. The current-voltage (i, v) is known as a fingerprint of a memristor i.e., it displays a pinched hysteresis loop whose shape varies with frequency. The fundamental mathematical expressions describing the memristor are defined as follows: $v_M = M(\sigma)i_M$ or $i_M = W(\varphi)v_M$ where $M(\sigma)$ and $W(\varphi)$ denote the memristor controlled by charge σ and flux φ, respectively, which satisfies the following relations:
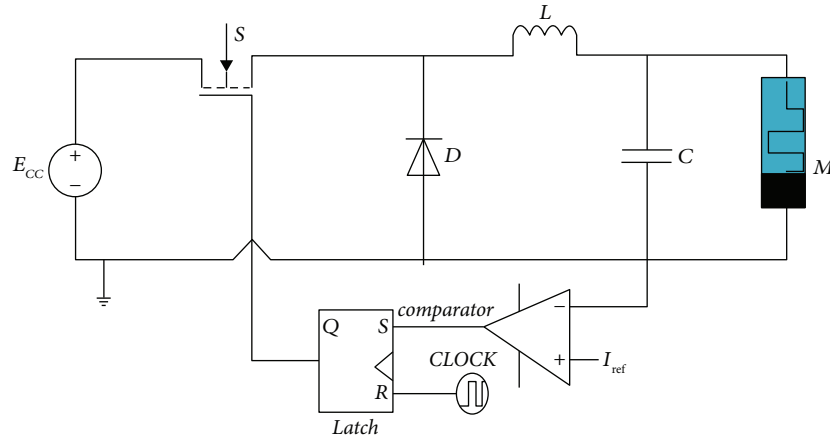
FIGURE 1: A novel circuit system having a dc/dc buck converter and a memristance load.

TABLE 1: Operation principle of the buck converter.

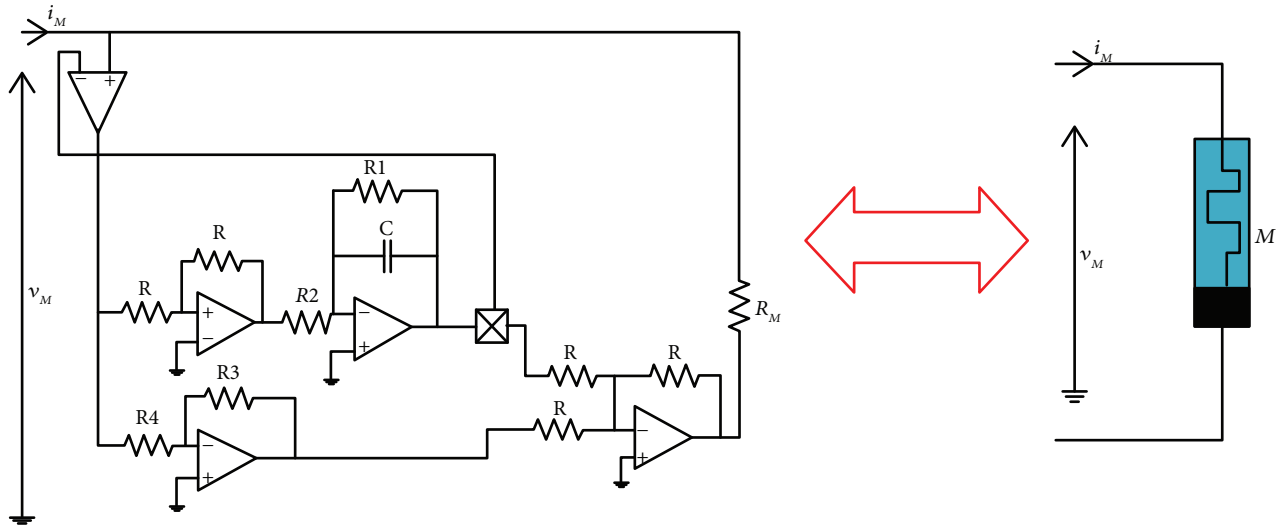| Switch	Initial value of i_L	Current variation	Buck state
ON	$i_L(0) = I_{min}$	i_L increasing and reaches I_{ref}	ON-state
OFF	$i_L(T_S/2) = I_{ref}$	i_L pass through the diode D and the capacitor C	OFF-state

FIGURE 2: Memristive load emulator circuit. Electrosymbol of a memristor.

$$\begin{cases} \dfrac{dq}{dt} = h(i_M, \sigma, z), \\[2mm] \dfrac{d\varphi}{dt} = k(v_M, \varphi, z), \end{cases} \tag{1}$$

where $h(i_M, \sigma, z)$ and $k(v_M, \varphi, z)$ denote the internal state functions of a memristor.

Using Kirchhoff laws and some techniques for circuits analysis, we derive the following equations from Figure 2;

$$\begin{cases} i_M = \left[\left(\dfrac{1}{R_M} - \dfrac{R_3}{R_4 R_M} \right) + \dfrac{1}{R_M} \varphi \right] v_M, \\[3mm] \dfrac{d\varphi}{dt} = \dfrac{v_M}{R_2 C} - \dfrac{\varphi}{R_1 C}. \end{cases} \tag{2}$$

Letting $v_M = v_c$, $(1/R_2 C) = \alpha m$, $(1/R_1 C) = \alpha n$, $p = (R_3/R_4 R_M) - (1/R_M)$, $r = (1/R_M)$, equation (2) becomes

$$\begin{cases} i_M = (r\varphi - p) v_M, \\[2mm] \dfrac{d\varphi}{dt} = \alpha(m v_M - n\varphi), \end{cases} \tag{3}$$

where i_M is the current passing through the memristive emulator (emulator refers to the electronic circuit that imitates the behavior of a complex phenomenon) load where the simplified electrosymbol is represented in Figure 2. The circuit parameters of the memristive load emulator are recorded in Table 2. Taking the input voltage of the terminal of the memristor load emulator as $v_M = 4\sin(5000\pi t)V$ and f chosen as 200 Hz. The loci in the $v_M - i_M$ phase plane and the memductance curves are plotted in Figures 3(a)–3(d).

TABLE 2: Parameter values.

Circuit component	Values
CLOCK frequency f	5000 Hz
Inductance L	0.6 mH
Capacitance C	200 μF
DC source V-I	12 V
Resistance R_3	30 kΩ
Resistance R	10 Ω
Reference current I_{ref}	0.6 A
Resistance R_1	5 kΩ
Resistance R_2	10 kΩ
Resistance R_M	1 Ω
Resistance R_4	10 kΩ

From these figures, we observe the zero-crossing property of the memristor which stipulates that the output i_M is always equal to the input v_{in} at zero. This important feature shows the existence of memristive fingerprint. We recall that, in the past few years, various memristor emulators implemented by already-existing electronic components have been reported in the literature [4, 39]. Most of the hardware topologies mainly include multiplier-based memristor equivalent circuits [40] and op-amps. Many researchers used different memristive loads to capture some special dynamical behaviors in memristive systems [41] and the references therein. Compared with other memristor emulators reported previously, the memristor emulator shown in Figure 2 presents an important feature. The hysteresis curve is located in the quadrants (1 and 3); instead, in references [35, 38], the same curve is located in the quadrants (2 and 4) which corresponds respectively to the active and passive zone of the operation of the memristor. As an active device (as in our case), it provides energy to the system and also allows for chaotic oscillations. However, as a passive device, it consumes energy in the system and obtaining oscillations can only be possible when exploiting a nonlinearity of the system, not of the memristor.

Remark 1. We note that the hysteresis loop falls into the second and the fourth quadrants. The memristor is a passive component and then efficiently stores information because the value of its electrical resistance changes permanently when a current is applied. A memristor can also have a high resistance value and a low resistance value. For instance, for a very high resistance value, it is observed that the resulting characteristic is located in the first and fourth quadrants, and for a low resistance value, it can be observed in the second and the third quadrants [42].

Remark 2. In real applications, there is no resistive load in nature because the linear component does not exist in real life. Since the load can reveal a plethora of complex behaviors, it seems interesting to investigate the case that the load is characterized by the hysteresis phenomenon such as memristor. We recall that the intrinsic nature of the memristor modifies the current-voltage characteristic of the converter and has a considerable impact on the dynamics of the buck converter.

3.2. System Description. We recall that the analysis of the dynamics is strongly determined by the state of the switch. We then propose to obtain the mathematical model from Figure 1 based on the electrical circuit analysis.

Case 1. Switch D is ON

When the switch S is ON, there are two independent loops denoted by red dashed lines in Figure 4. According to Kirchhoff's law, we have

$$L\frac{di_L}{dt} = E - v_c,$$

$$C\frac{dv_c}{dt} = i_L - (r\varphi - p)v_c, \tag{4}$$

where v_c denotes the voltage across the flux contused memristor. If we consider the expression $(d\varphi/dt) = \alpha(mv_c - n\varphi)$ as the memristor's internal state of function, we derive the following equations:

$$L\frac{di_L}{dt} = E - v_c,$$

$$C\frac{dv_c}{dt} = i_L - (r\varphi - p)v_c, \tag{5}$$

$$\frac{d\varphi}{dt} = \alpha(mv_c - n\varphi).$$

Equation (4) is the state of equation when the circuit of Figure 2 is in the ON-state. This state will be sustained until i reaches i_{ref}.

Case 1. Switch S is OFF

When the switch S is OFF, the diode D conducts. Also, another two independent loops denoted by red dashed line are shown in Figure 4. Combining these two loop equations, we obtain

$$L\frac{di_L}{dt} = -v_c,$$

$$C\frac{dv_c}{dt} = i_L - (r\varphi - p)v_c, \tag{6}$$

$$\frac{d\varphi}{dt} = \alpha(mv_c - n\varphi).$$

These two system equations can be summarized into the following system of equations as follows:

$$\frac{di_L}{dt} = -a_1\left(E(1-u) - v_c\right),$$

$$\frac{dv_c}{dt} = a_2\left(i_L - (r\varphi - p)v_c\right), \tag{7}$$

$$\frac{d\varphi}{dt} = \alpha(mv_c - n\varphi),$$

where $u = \begin{cases} 1, & \text{for turn} - \text{off} \\ 0, & \text{for turn} - \text{on} \end{cases}$.
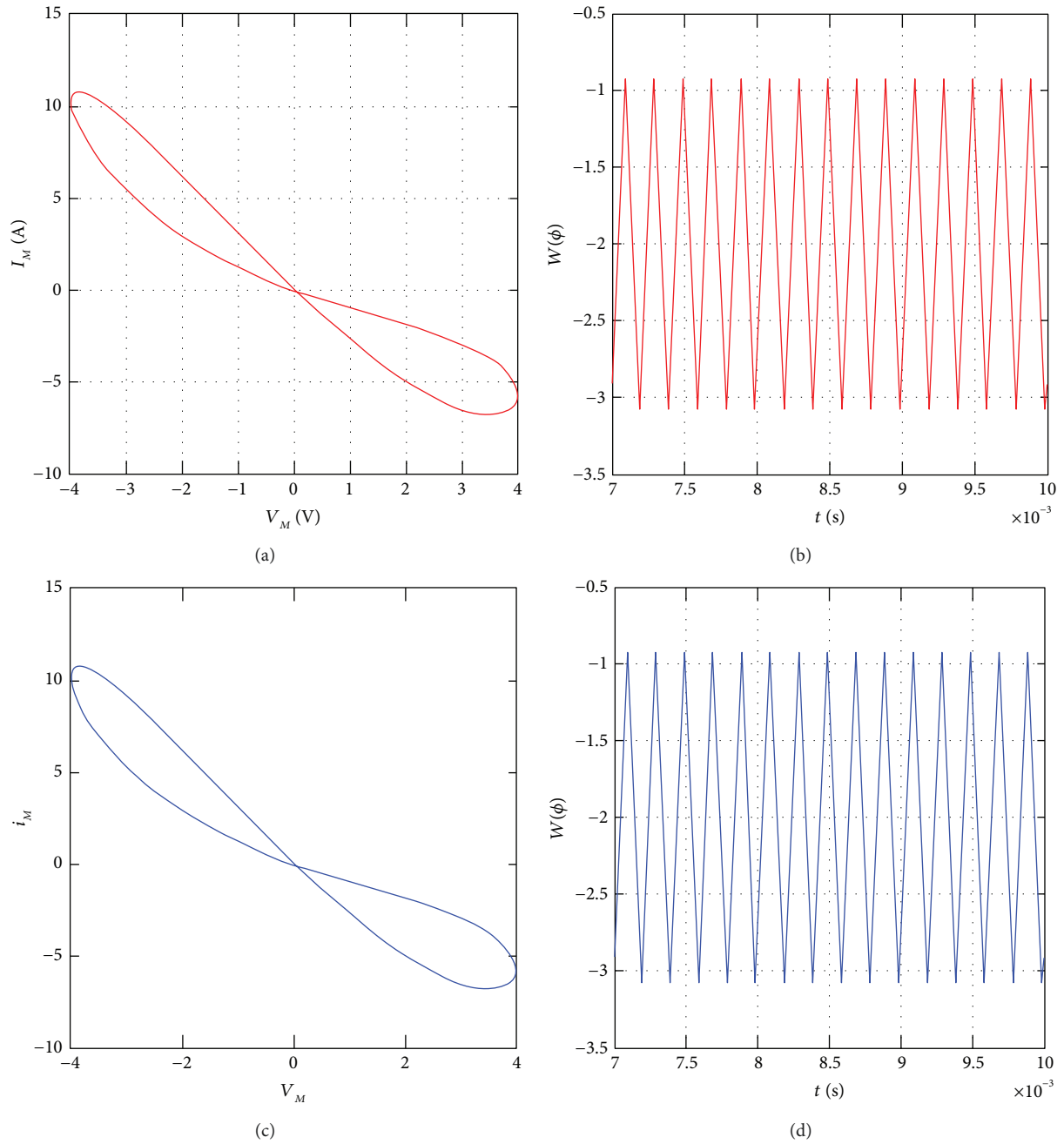
(a)

(b)

(c)

(d)

Figure 3: Numerical and analog simulation of the pinched hysteresis loops and memductance curves of the memristive load. (a, c) PSIM circuit simulations; (b, d) Fortran numerical simulations; (a, b) pinched hysteresis loops in the $(v_M - i_M)$ plane; (c, d) memductance curves versus time.
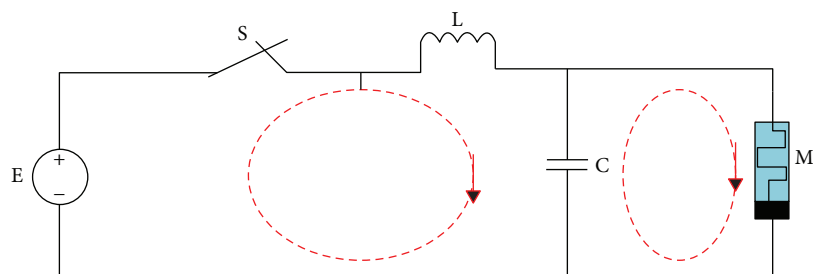

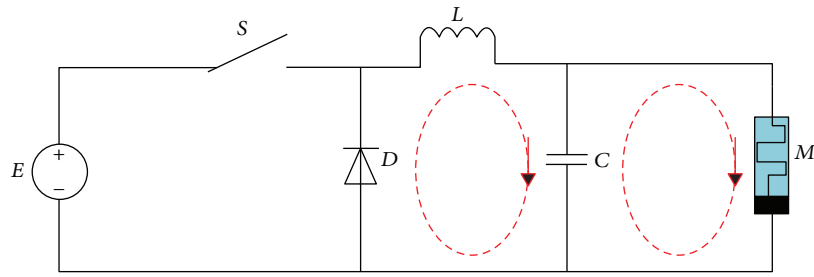Figure 4: Electrical circuit of a switch ON buck chopper.

FIGURE 5: Electrical circuit of a switch OFF buck chopper.

TABLE 3: Nature of the roots of the characteristic equation computed for various values of E.

| Values of the bifurcation parameter (E)	Eigenvalues at $(\lambda_1, \lambda_2, \lambda_3)$ nontrivial fixed $O_0 (((mr/n)E - p)E, E, (m/n)E)$	Eigenvalues at $(\lambda_1, \lambda_2, \lambda_3)$ the origin $O_1 (0, 0, 0)$
$E = 0$	-2.000×10^4; 0.9082×10^4; 0.0918×10^4 (unstable)	-2.000×10^4; 0.9082×10^4, 0.0918×10^4; (unstable)
$E = 5$	$(-1.0968 \pm 1.3254i) \times 10^4$; -1.0563×10^4 (stable)	-2.000×10^4, 0.9082×10^4; 0.0918×10^4 (unstable)
$E = 8$	$(-1.4861 \pm 1.9474i) \times 10^4$, -0.0278×10^4; (stable)	-2.000×10^4; 0.9082×10^4; 0.0918×10^4 (unstable)
$E = 12$	$(-1.9917 \pm 2.4597i) \times 10^4$, -0.0166×10^4; (stable)	-2.000×10^4; $0.9082 * 10^4$; 0.0918×10^4 (unstable)
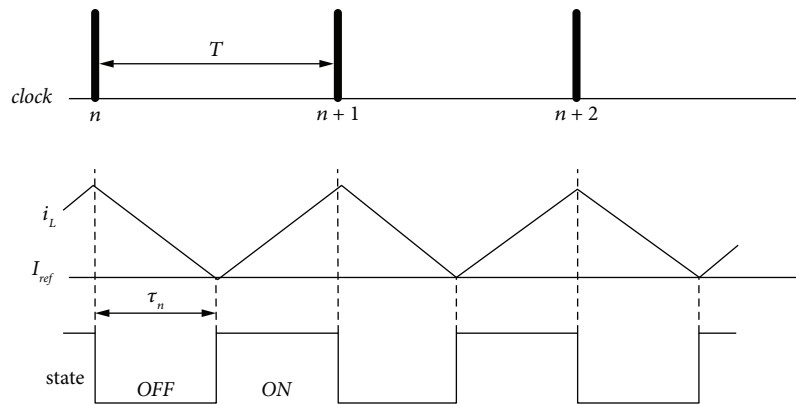
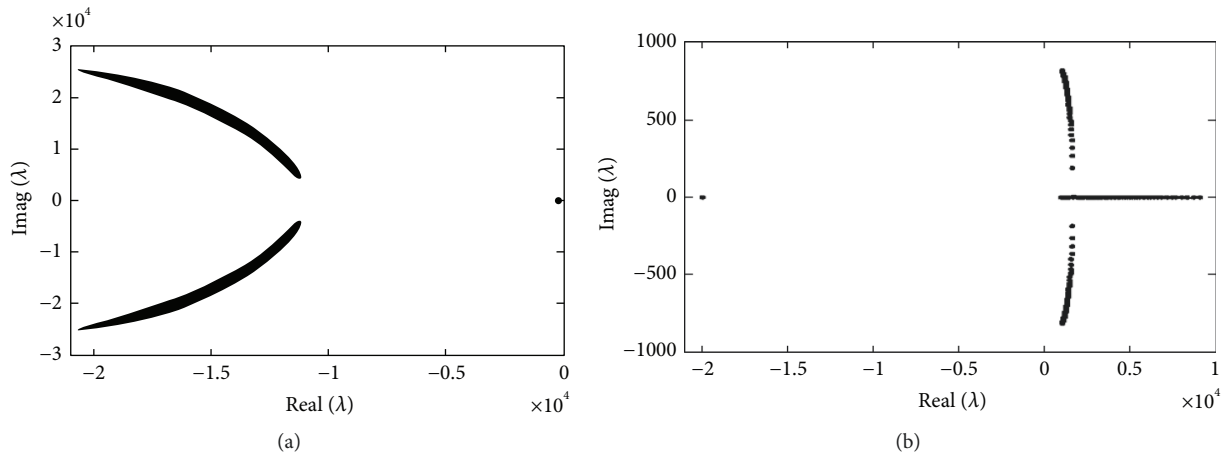FIGURE 6: Operation waveforms i_L operating in CCM.

(a)

(b)

FIGURE 7: Stability analysis for $u = 0$ (a) and $u = 1$ (b), stability curves (a, b) plotted with the set of parameters as follows: $n = 2; m = 1; p = 2; r = 1; \alpha = 10000; L = 0.6\,\text{mH}; E \in [9.5\,\text{V}, 12.5\,\text{V}]$ and $C \in [200\,\mu\text{F}, 1\,\text{mF}]$.

(a)   (b)
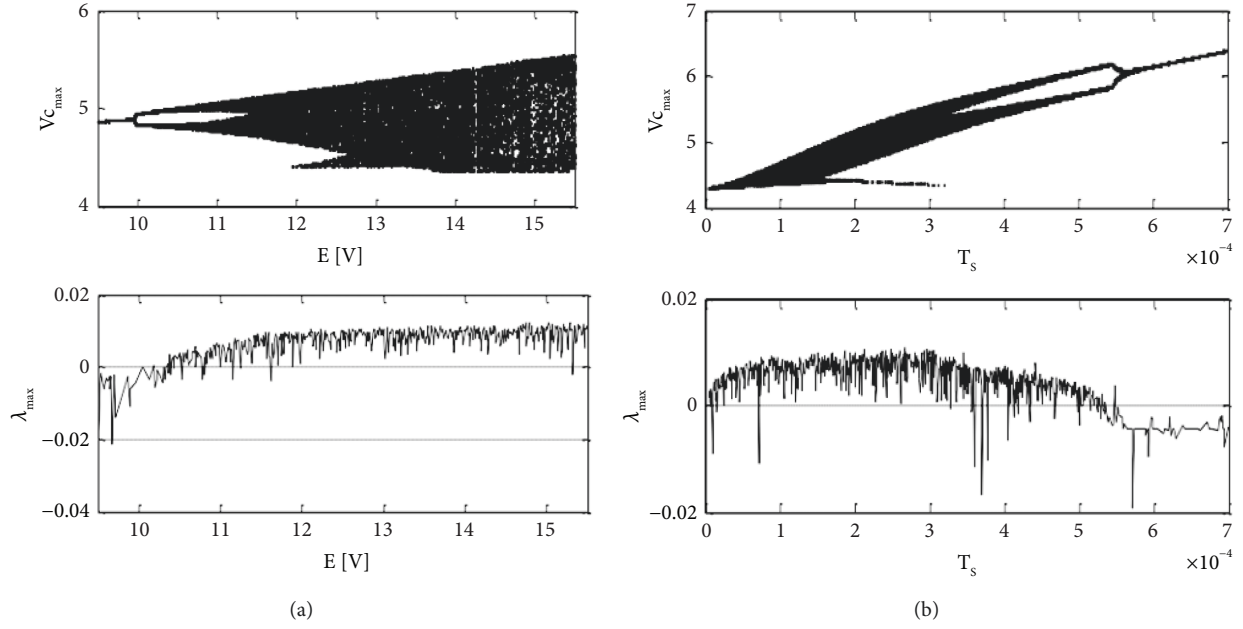
FIGURE 8: Bifurcation diagram versus E and T_s: (a) $E \in [10; 16]$; (b) $T_s \in [0; 7 \times 10^4]$ and the corresponding graph of maximum Lyapunov exponent. A positive value of Lyapunov exponent indicates chaos while regular oscillations are related to negative values of Lyapunov exponent.
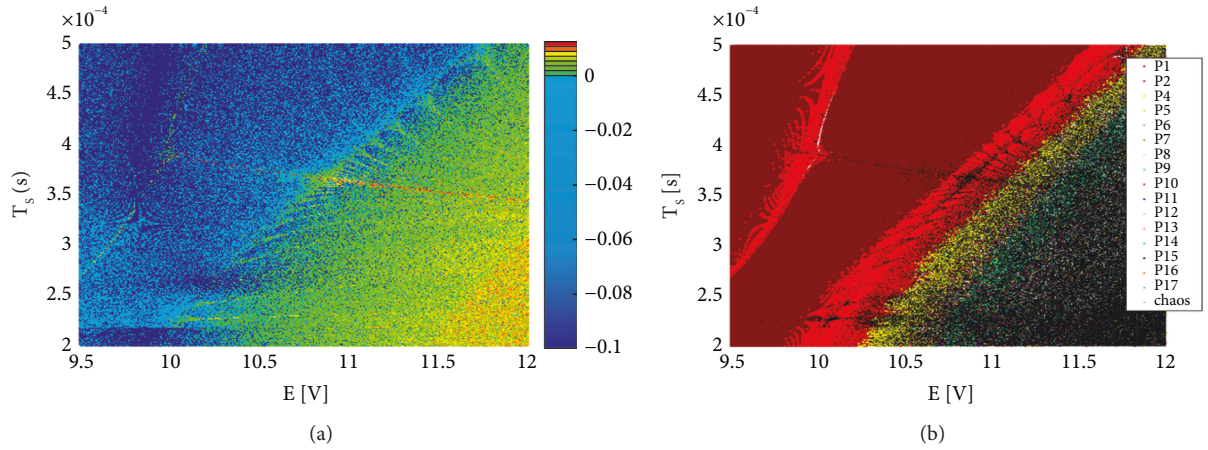

(a)   (b)

FIGURE 9: Dynamical domain shown in the two parameters space (T_s, E) is the boundary regions of each dynamical feature in the Buck converter. (a) Periodic oscillations are revealed by red region, while chaotic oscillations are manifested by a continuously changing black region bifurcation diagram and (b) the corresponding two diagram Lyapunov exponents. E versus parameter T_s.

There are two states for the continuous mode which are linked. Figure 5 presents the dynamical change of the current i_L in continuous current mode (CCM).

4. Equilibrium Points and their Stability

Generally, there are equilibrium points in most of the physical systems and it is necessary to investigate the equilibrium points since they affect the system dynamics to a great extent. For equations (5) and (6), we can calculate their equilibrium points by solving the following equation:

$$\left(\frac{di_L}{dt} \ \frac{dv_c}{dt} \ \frac{d\varphi}{dt} \right) = \left(0 \ \ 0 \ \ 0 \right). \tag{8}$$

By solving (8), the general equilibrium point is given by

$$O_u \left(\left(\frac{mr}{n} E(1-u) - p \right) E(1-u), E(1-u), \frac{m}{n} E(1-u) \right). \tag{9}$$

The Jacobian matrices are

(a)

(b)

(c)

(d)

(e)

(f)

FIGURE 10: MATLAB numerical simulation: the time-domain waveforms and phase portraits of dc/dc single-stage current-mode-controlled buck converter. (a) inductor current with chaotic orbit for $E = 12$ V; (b) capacitor voltages with chaotic orbit; (c) phase portrait with period-1 orbit for $E = 9$ V; (d) phase portrait with period-2 orbit for $E = 9.67$ V; (e) phase portrait with period-4 orbit for $E = 10.67$ V; (f) phase portrait with chaotic orbit corresponding to (a) and (b).
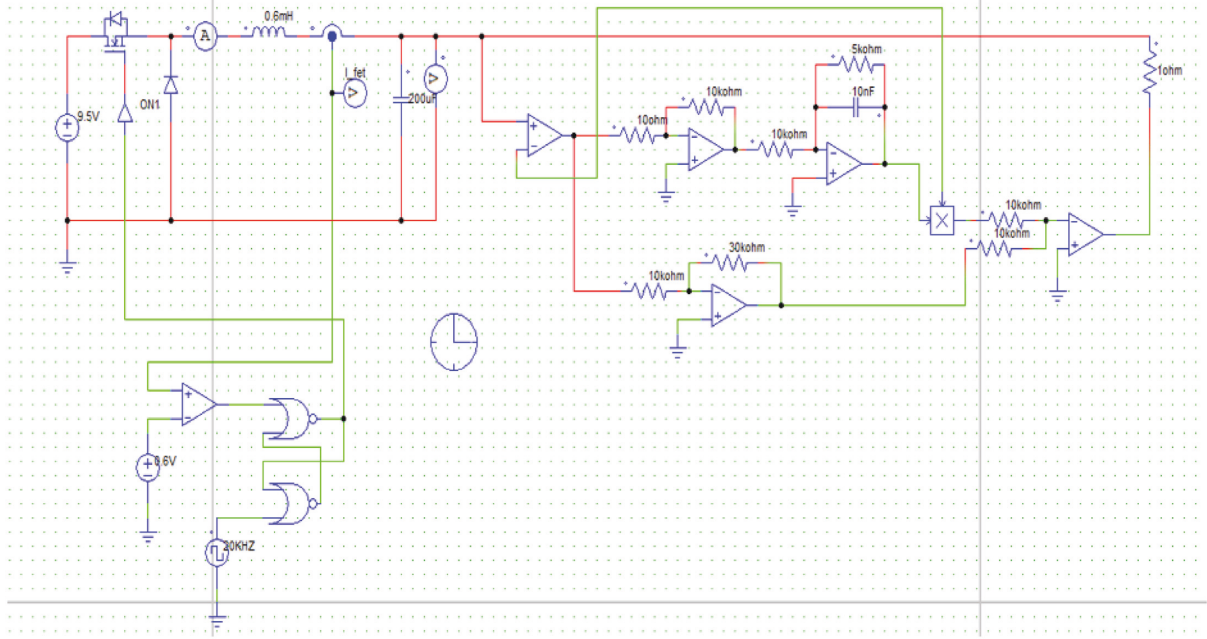
FIGURE 11: Screenshot of PSIM simulation model of the buck converter with memristive load.

$$J_{O_u} = \begin{pmatrix} 0 & -a_1 & 0 \\ a_2 & a_2 p - a_2 r \dfrac{m}{n} E(1-u) & -a_2 r E(1-u) \\ 0 & \alpha m & -\alpha n \end{pmatrix},$$

with $a_1 = \dfrac{1}{C} et \ a_2 = \dfrac{1}{L}.$

$$(10)$$

The eigenvalues are obtained at equilibrium point by solving the expression

$$\det(J_O - \lambda I_3) = 0. \tag{11}$$

The characteristic equation is given by

$$\lambda^3 + \left(\alpha n + a_2 r \frac{m}{n} E(1-u) - a_2 p\right)\lambda^2$$

$$+ (a_1 a_2 + 2\alpha m a_2 r E(1-u) - \alpha n a_2 p)\lambda \tag{12}$$

$$+ \alpha n a_1 a_2 = 0.$$

Obviously, equation (12) represents the characteristic equation that can be used to analyze the stability of the system around its equilibrium points. However, the non-trivial fixed points can be found by exploiting numerical methods, in particular, by using the Newton Raphson method. As already pointed out, it can be found that there exists two equilibrium points on the (x, y, z) plane, that is, for $u = 0$, the equilibrium point is, $O_0(((mr/n)E - p)E, E, (m/n)E)$, and $O_1(0, 0, 0)$ for $u = 1$. Table 3 shows the roots of the characteristic equation computed for various values of E. It clearly appears from Table 3 that the system is unstable for some values of E and the graphical representations are

provided in Figure 6. As the system presents instability, it is necessary to study the dynamic behavior of the system. Note that for a smooth chaotic circuit system with a memristor, the local activity, i.e., the negative resistance region of a memristor is essential for generating chaos, while for a switched chaotic system with a memristor, it might be unnecessary for generating chaos. Figure 7 shows the eigenvalue locus in the complex plan $(\text{Re}(\lambda), \text{Im}(\lambda))$ with the following parameter values: $n = 2; m = 1; p = 2; r = 1; \alpha = 10000; L = 0.6$ mH. The intersection of the curve with imaginary axis shows the presence of the Hopf bifurcation in the system.

5. Numerical Investigations

5.1. Bifurcation and Lyapunov Exponent Analysis based on Computer Simulations. The bifurcation and Lyapunov exponent diagrams are powerful graphical nonlinear analysis tools to locate promising parameter windows that provide a detailed knowledge of the system behavior. There exist several numerical techniques to differentiate these motions, and the bifurcation diagram is one of the most important ones. A bifurcation diagram can be used to exhibit the qualitative changes in features under the variation of one or more parameters on which the system depends. Generally, there exist one or more bifurcation parameters in a chaotic system. To this end, equations (4) and (5) were integrated systematically over grids of equally spaced parameters using a standard Runge–Kutta fourth-order algorithm with a fixed time step $h = 10^{-6}$. In order to provide a better performance, Fortran software is exploited to perform this high-resolution computation which is quite demanding. The following initial conditions are considered for the simulations $x = 1, y = 0, z = 0, t = 0$. We recall that for a chaotic system, for special parameters, the buck converter may have distinct motions
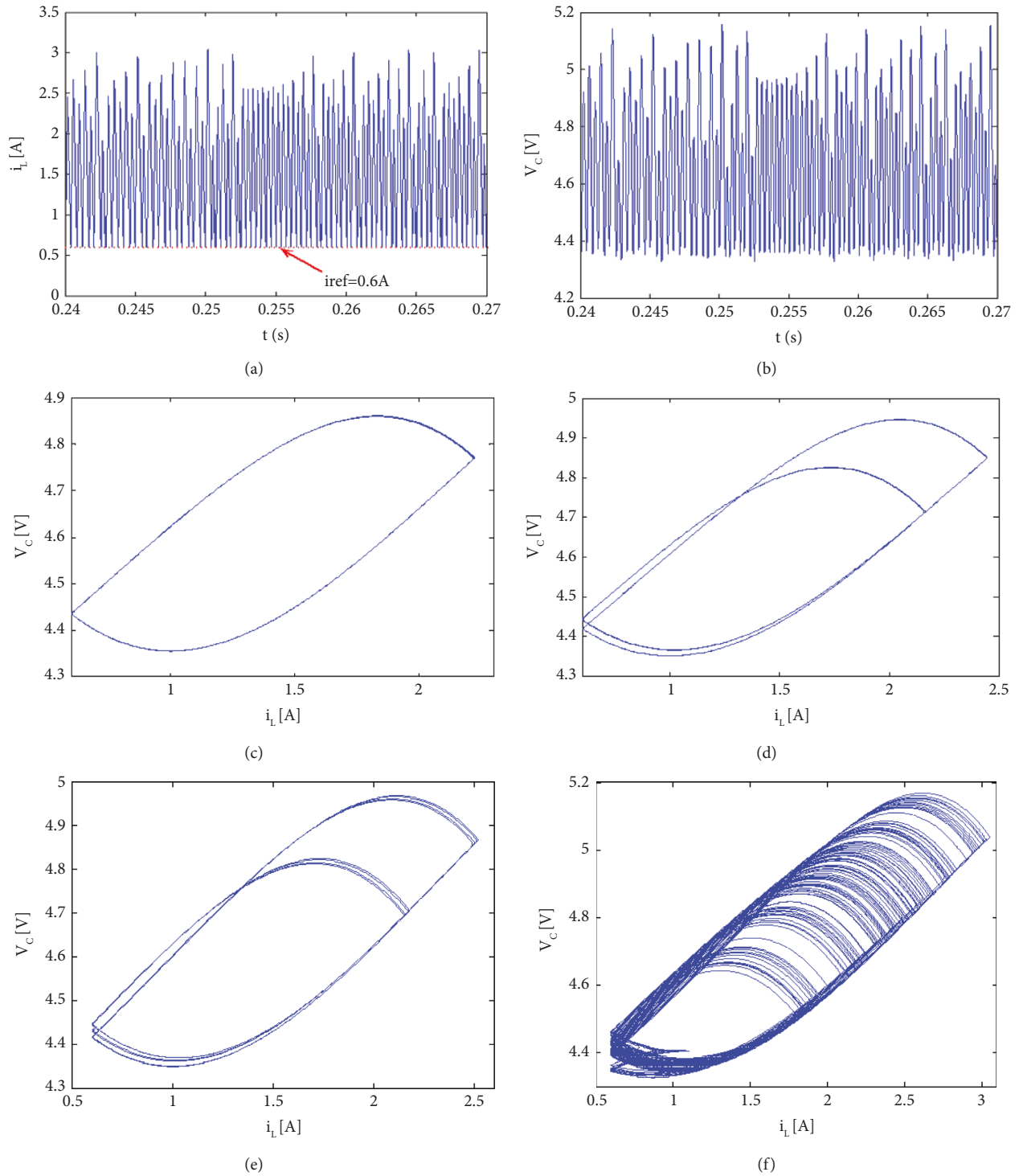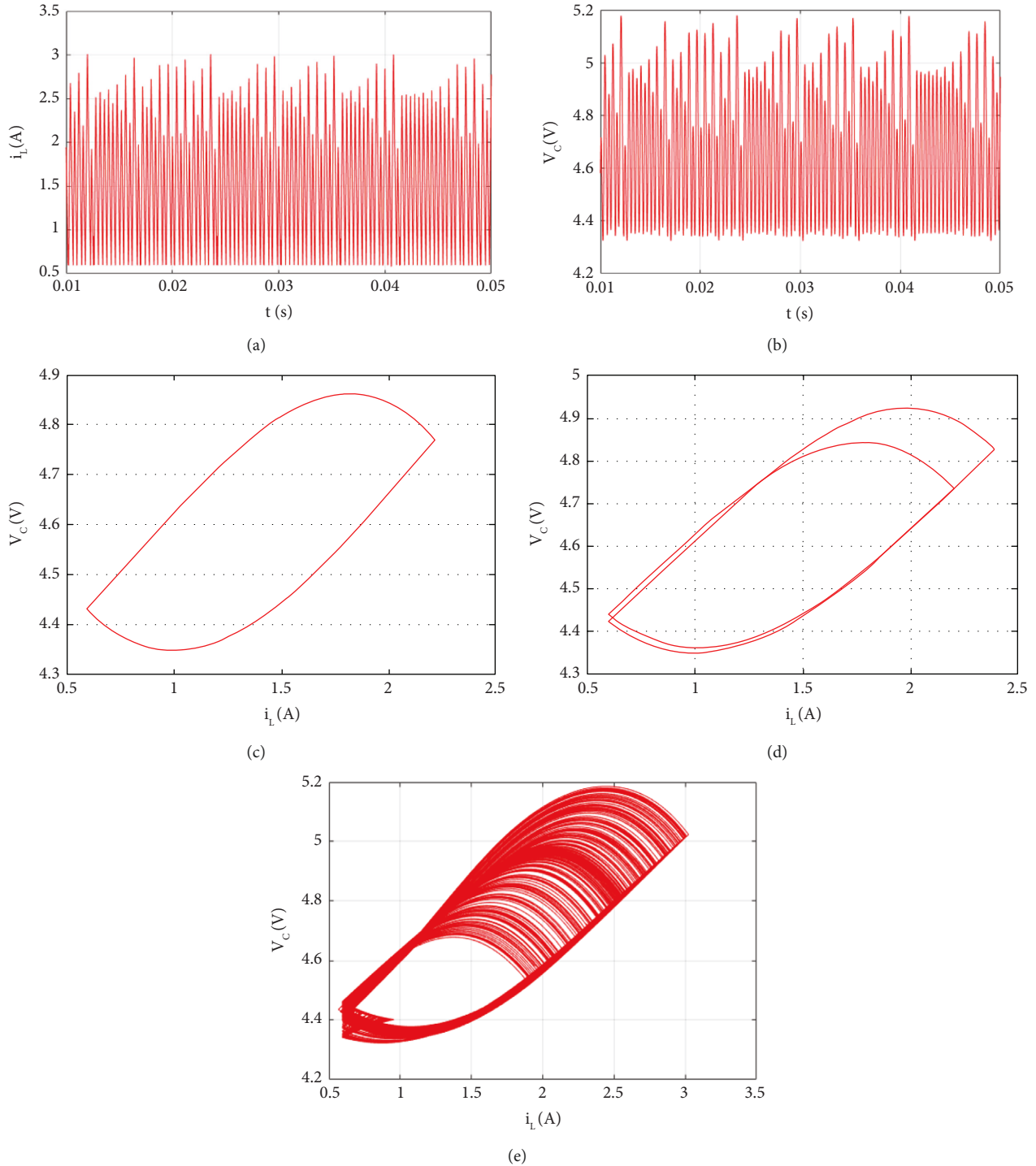
(a)

(b)

(c)

(d)

(e)

FIGURE 12: Analog simulation PSIM: the time-domain waveforms and phase portraits of dc/dc single-stage current-mode-controlled buck converter. (a) inductor current with chaotic orbit for $E = 12$ V; (b) capacitor voltages with chaotic orbit; (c) phase portrait with period-1 orbit for $E = 9$ V; (d) phase portrait with period-2 orbit for $E = 9.67$ V; (e) phase portrait with chaotic orbit corresponding to (a) versus (b).

such as periodic motion, quasiperiodic motion, subharmonic, chaos, and hyper-chaos. Figure 8 presents in two complementary ways (described below) bifurcation diagrams and Lyapunov exponent characterizing the far-reaching regular organization induced by the set of stable and unstable oscillations of the circuit. These panels' bifurcation and their corresponding Lyapunov exponent are plotted for the values of parameters set as follows:

$$T_S = 200\,\mu\text{s}; m = 1; n = 2; r = 1; p = 2; i_{\text{ref}} = 0.6\,\text{mA}; L$$
$$= 0.6\,\text{mH}; C = 200\,\mu\text{F},$$
$$E = 12\,\text{V}; m = 1; n = 2; r = 1; p = 2; i_{\text{ref}} = 0.6\,\text{mA}; L$$
$$= 0.6\,\text{mH}; C = 200\,\mu\text{F}.$$

$$(13)$$

Figures 8(a) and 8(b) show the bifurcation diagrams of the current-mode-controlled buck converter by taking input voltage E and the T_s parameter as bifurcation parameters, respectively. From these, we clearly observe that the first period-doubling bifurcations occur at $E = 10\,\text{V}$ and $T_s = 5.8 \times 10^{-4}$, respectively. As the parameter E increases, forward bifurcation routes with period-doubling and border collision to chaos suddenly appear in the buck converter and globally characterize the routes toward chaos. When parameter T_s increases, reversed bifurcation routes with period-doubling and chaos appear in the buck converter topology under investigation.

With the aim to have a perfect and complete knowledge of the total dynamics of the system, the standard Lyapunov stability diagrams are plotted to give the zones of chaotic and periodic oscillations according to two parameters of the system. Figures 9(a) and 9(b) represent the bifurcation diagrams with the corresponding Lyapunov exponents when the voltage E and period T_s are monitored. One can see that the negative exponents correspond to the periodicity zones of the diagram of bifurcation and the positive exponents correspond to chaos. Figure 9(a) shows a two parameters sweep, obtained by plotting the aforementioned fine parameter grid, the nonzero Lyapunov exponent which stands as a familiar indicator allowing one to discriminate unambiguous chaos (positive exponents) from periodic oscillations (negative exponents). Indeed, the values below zero are the negative values (indicated on the legend by the color blue) of Lyapunov exponent and those above are positive values (on the legend indicated by the color green, red, and yellow) of Lyapunov exponent. A very distinct and complementary representation of the same parameter of bifurcation $[E, T_S]$ is presented in Figure 9(b), in the form of a bifurcation diagram namely, a diagram obtained by plotting local maxima according to the control parameters. This diagram was drawn using 18 colors; the first 17 colors represent the zones of periodicity (represented by rainbow color) and the last color (black) represents chaos.

The results previously obtained can be proven by the time-domain waveforms and the phase portraits which are particularly important for observing nonlinear phenomena. The current-mode-controlled buck converter can be obtained using Runge–Kutta algorithm via constructing piecewise smooth switching models obtained from Fortran simulation (the time-domain waveforms and the phase portraits of the inductor current versus output voltage). Taking the variation of input voltage E into consideration, the time-domain inductor current and output voltage waveforms are obtained for $E = 12\,\text{V}$. Figures 10(a) and 10(b) present the time evolution of the states (i_L and V_c) and the phase portraits are shown in Figures 10(c)–10(f) which

correspond to period-1 orbit, period-2 orbit, period-4 orbit, and chaotic orbit, respectively.

6. PSIM Simulation Results

6.1. Schematic Circuit. In this section, the dc/dc converter circuit with a memristance load in PSIM is built to demonstrate the presence of complex phenomena in the system under investigation. Based on Figure 1, the schematic circuit is shown in Figure 11. The schematic circuit consists of the buck circuit (on the left) of the memristor emulator (on the right) and the controlled current source. The experimental values considered are recorded in Table 2. The current sensor ISEN7, which can transform the current signal into a voltage signal, is used to collect the current i through the inductor L. The collected voltage signal as the input of comparator U can be used to compare the reference current I_{ref}. Note that the input signal of the comparator U is in fact a voltage signal; therefore, $V_2 = 0.6\,\text{V}$ can be regarded as $I_{\text{ref}} \equiv 0.6A$.

6.2. Validation by Circuit Simulations. PSIM (Power Simulation) software is a useful simulation tool, which can be used to simulate the time sequences and phase portraits of the memristive buck converter. With PSIM Version 9.0 software, the circuit simulation model is built with a relevant frequency and duty cycle of the square-wave voltage source to have these different behaviors. We note that their default values are 5000 Hz and 0.5, respectively. However, we plot the current i_M at the terminal of the inductor and the voltage v_m at the terminal of the memristor. The results are reported in Figure 12. Note that the time series, periodic, and chaotic portraits are captured by the virtual oscilloscope in PSIM. With reference to the pictures in Figure 12, it can be seen that the buck converter under consideration experiences the same bifurcation scenarios as predicted in the previous section.

7. Conclusion

The nonlinear behavior of current-mode-controlled buck converter memristive load is investigated in this paper. The study of stability allowed us to observe that the system has rich dynamic behavior when some system parameters change. Different tools such as bifurcation diagrams, Lyapunov exponent, phase portraits, and two parameters Lyapunov diagram are considered to provide a systematic total dynamics of the dc/dc buck converter. Peak current-mode controlled single-stage buck converter system with a memristance load goes to chaos via period-doubling and border collision routes. Moreover, it was found that the analog results in PSIM are similar to the numerical results in Fortran. Especially, peak current controlled buck converter exhibits inverse nonlinear behaviors compared with a current-mode-controlled buck converter. More interestingly, one of the key contributions is the finding of various regions in the parameters' space in which the buck converter experiences the unusual phenomenon of competing attractors which is not yet reported in the literature. It should be noted that we only focused on the investigation

of dynamical behaviors with respect to the frequency and the voltage, and it will be necessary to further study the dc/dc converters with a memristance load by considering the system parameters and topological structures in future research studies. It is worth noting here that we have worked with a continuous memristor model on a discrete converter topology, and some recent works present in detail analyzes the discrete memristor model [42, 43]. This issue should be considered in our future directions with the same converter topology with the aim to point out some technical specifications.

Data Availability

The research data used to support the findings of this study is described and included in the article. Furthermore, some of the data used in the study are also supported by providing references as described in the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

References

[1] M. A. Sakka, J. Van Mierlo, and H. Gualous, *Electric Vehicles Modelling and Simulations*, InTech, Rijeka, Croatia, 2011.

[2] N. Dan, L. Dan, P. Viorel, and I. Corina, "Bifurcation and Chaotic Aspects in Peak Current Controlled Buck-Boost Converters," *WSEAS Transactions on Circuits and Systems*, vol. 7, 2008.

[3] G. H. Zhou, B. C. Bao, J. P. Xu, and Y. Y. Jin, "Dynamical Analysis and Experimental Verification of valley Current Controlled Buck Converter," *Chinese Physics B*, vol. 19, 2010.

[4] D. Giaouris, S. Banerjee, B. Zahawi, and V. Pickert, "Stability Analysis of the Continuous-Conduction-Mode Buck Converter Via Filippov's Method," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 4, pp. 1084–1096, 2008.

[5] L. Q. Zheng and Y. Peng, "Chaos control of voltage mode controlled buck-boost converter," *Acta Physica Sinica*, vol. 65, no. 22, 2016.

[6] M. di Bernardo, F. Garefalo, L. Glielmo, and F. Vasca, "Switchings, bifurcations, and chaos in DC/DC converters," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 45, no. 2, pp. 133–141, 1998.

[7] H. Li, Z. Li, B. Zhang, Q. Zheng, and W. Halang, "The stability of a chaotic PWM boost converter," *International Journal of Circuit Theory and Applications*, vol. 39, no. 5, pp. 451–460, 2011.

[8] J. D. Morcillo, D. Burbano, and F. Angulo, "Adaptive Ramp Technique for Controlling Chaos and Subharmonic Oscillations in DC-DC Power Converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5330–5343, 2016.

[9] H. Zhang, W. Li, H. Ding, P. Luo, X. Wan, and W. Hu, "Nonlinear Modal Analysis of Transient Behavior in Cascade DC-DC Boost Converters," *International Journal of Bifurcation and Chaos*, vol. 27, no. 9, p. 1750140, 2017.

[10] L. Corradini, E. Orietti, P. Mattavelli, and S. Saggini, "Digital Hysteretic Voltage-Mode Control for DC-DC Converters Based on Asynchronous Sampling," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 201–211, 2009.

[11] R. Gavagsaz-Ghoachani, M. Phattanasak, M. Zandi et al., "Estimation of the bifurcation point of a modulated-hysteresis current-controlled DC-DC boost converter: stability analysis and experimental verification," *IET Power Electronics*, vol. 8, no. 11, pp. 2195–2203, 2015.

[12] N. Zamani, M. Ataei, and M. Niroomand, "Analysis and control of chaotic behavior in boost converter by ramp compensation based on Lyapunov exponents assignment: theoretical and experimental investigation," *Chaos, Solitons & Fractals*, vol. 81, pp. 20–29, 2015.

[13] W. Hu, B. Zhang, R. Yang, and D. Qiu, "Dynamic behaviours of constant on-time one-cycle controlled boost converter," *IET Power Electronics*, vol. 11, no. 1, pp. 160–167, 2018.

[14] P. Karamanakos, T. Geyer, and S. Manias, "Direct Voltage Control of DC-DC Boost Converters Using Enumeration-Based Model Predictive Control," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 968–978, 2014.

[15] B. Wang, V. R. K. Kanamarlapudi, L. Xian, X. Peng, K. T. Tan, and P. L. So, "Model Predictive Voltage Control for Single-Inductor Multiple-Output DC-DC Converter With Reduced Cross Regulation," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4187–4197, 2016.

[16] Q. Wei, B. Wu, D. Xu, and N. R. Zargari, "Model Predictive Control of Capacitor Voltage Balancing for Cascaded Modular DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 752–761, 2017.

[17] N. Katayama, S. Tosaka, T. Yamanaka, M. Hayase, K. Dowaki, and S. Kogoshi, "New topology for DC-DC converters used in fuel cell-electric double layer capacitor hybrid power source systems for mobile devices," *IEEE Transactions on Industry Applications*, vol. 52, no. 1, pp. 313–321, 2016.

[18] B. C. Bao, G. H. Zhou, J. P. Xu, and Z. Liu, "Unified classification of operation-state regions for switching converters with ramp compensation," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1968–1975, 2011.

[19] M. Zhioua, A. El Aroudi, S. Belghith et al., "Modeling, dynamics, bifurcation behavior and stability analysis of a DC-DC boost converter in photovoltaic systems," *International Journal of Bifurcation and Chaos*, vol. 26, no. 10, p. 1650166, 2016.

[20] S. Banerjee and K. C. Chakrabarty, "Nonlinear modeling and bifurcations in the boost converter," *IEEE Transactions on Power Electronics*, vol. 13, no. 2, pp. 252–260, 1998.

[21] E. El Aroudi, L. Benadero, E. Toribio, and S. Machiche, "Quasiperiodicity and chaos in the DC-DC buck-boost converter," *International Journal of Bifurcation and Chaos*, vol. 10, no. 02, pp. 359–371, 2000.

[22] J. P. Wang, B. C. Bao, J. P. Xu, G. H. Zhou, and W. Hu, "Dynamical effects of equivalent series resistance of output capacitor in constant on-time controlled buck converter," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 5, pp. 1759–1768, 2013.

[23] Y. Wang, R. Yang, B. Zhang, and W. Hu, "Smale Horseshoes and Symbolic Dynamics in the Buck-Boost DC-DC Converter," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 800–809, 2018.

[24] G. H. Zhou, B. C. Bao, and J. P. Xu, "Complex dynamics and fast-slow scale instability in current-mode controlled buck

converter with constant current load," *International Journal of Bifurcation and Chaos*, vol. 23, no. 04, p. 1350062, 2013.

[25] C. C. Fang, "Saddle-node bifurcation in the buck converter with constant current load," *Nonlinear Dynamics*, vol. 69, no. 4, pp. 1739–1750, 2012.

[26] Y. F. Zhou, D. D. Jiang, J. C. Huang, and J. N. Chen, "Impedance characteristic of load in dc-dc converters and its effect on stability," *Proc CSEE*, vol. 30, pp. 15–21, 2010.

[27] A. El Aroudi, L. Benadero, E. Toribio, and G. Olivar, "Hopf bifurcation and chaos from torus breakdown in a PWM voltage-controlled DC-DC boost converter," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 46, no. 11, pp. 1374–1382, 1999.

[28] Y. Wang, R. Yang, B. Zhang, and W. Hu, "Smale Horseshoes and Symbolic Dynamics in the Buck-Boost DC-DC Converter," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 800–809, 2018.

[29] Z. T. Zhusubaliyev and E. Mosekilde, "Multistability and hidden attractors in a multilevel DC/DC converter," *Mathematics and Computers in Simulation*, vol. 109, pp. 32–45, 2015.

[30] D. W. Spier, G. G. Oggier, and S. A. O. da Silva, "Dynamic modeling and analysis of the bidirectional DC-DC boost-buck converter for renewable energy applications," *Sustainable Energy Technologies and Assessments*, vol. 34, pp. 133–145, 2019.

[31] T. Kamal, U. Arifoğlu, and S. Z. Hassan, "Buck-boost Converter Small Signal Model: Dynamic Analysis under System Uncertainties," *Journal of Electrical Systems*, vol. 14, no. 2, 2018.

[32] A. Ghosh, N. Rana, and S. Banerjee, "Study of complex dynamics in DC-DC boost converter with dSPACE-based real time controller," *International Journal of Power Electronics*, vol. 11, no. 2, pp. 160–178, 2020.

[33] K. Mandal, S. Banerjee, and C. Chakraborty, "Complex Behavior of Load Resonant DC-DC Converters," in *Proceedings of the National Conference on Nonlinear Systems and Dynamics (NCNSD 2011)*, Tamil Nadu, India, January 2011.

[34] R. Zhang, A. Wu, S. Zhang, and S. Cang, "Dynamical Analysis and Circuit Implementation of a DC/DC Single-Stage Boost Converter with Memristance Load," *Nonlinear Dynamics*, vol. 93, no. 3, pp. 1741–1755, 2018.

[35] B. Bao, X. Zhang, H. Bao, P. Wu, Z. Wu, and M. Chen, "Dynamical Effects of Memristive Load on Peak Current Mode Buck-Boost Switching Converter," *Chaos, Solitons & Fractals*, vol. 122, pp. 69–79, 2019.

[36] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, 2008.

[37] L. O. Chua and S. M. Sung Mo Kang, "Memristive devices and systems," *Proceedings of the IEEE*, vol. 64, no. 2, pp. 209–223, 1976.

[38] L. Chua, "Memristor-the missing circuit element," *IEEE Transactions on Circuit Theory*, vol. 18, no. 5, pp. 507–519, 1971.

[39] B. C. Bao, N. Wang, Q. Xu, H. G. Wu, and Y. H. Hu, "A simple third-order memristive band pass filter chaotic circuit," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 8, pp. 977–981, 2017.

[40] H. Hyongsuk Kim, M. P. Sah, C. Changju Yang, S. Seongik Cho, and L. O. Chua, "Memristor emulator for memristor circuit applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 10, pp. 2422–2431, 2012.

[41] H. G. Wu, B. C. Bao, Z. Liu, Q. Xu, and P. Jiang, "Chaotic and periodic bursting phenomena in a memristive Wien-bridge oscillator," *Nonlinear Dynamics*, vol. 83, no. 1-2, pp. 893–903, 2015.

[42] K. Li, H. Bao, H. Li, J. Ma, Z. Hua, and B. C. Bao, "Memristive rulkov neuron model with magnetic induction effects," *IEEE Transactions on Industrial Informatics*, vol. 18, no. 3, pp. 1726–1736, 2022.

[43] H. Bao, Z. Hua, H. Li, M. Chen, and B. Bao, "Discrete memristor hyperchaotic maps," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 11, pp. 4534–4544, 2021.