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Research Article

Fully Integrated Chen Chaotic Oscillation System

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A fully integrated Chen chaotic oscillation system using operational amplifiers (OAs) and multipliers is designed and verified in this paper. Unlike the conventional breadboard-based Chen chaotic system using off-the-shelf discrete components, the fully integrated Chen chaotic oscillation circuit presented in this paper is realized using GlobalFoundries' 0.18 μm CMOS 1P6M process, and all the circuit components are integrated in a chip. The fully integrated Chen chaotic oscillation system is verified using Cadence IC Design Tools, and the post-layout simulation results indicate that the presented integrated Chen chaotic oscillation system only consumes 148 mW from ± 2.5 V supply voltage, and its chip area is 6.15 mm^2.

1. Introduction

With the development of nonlinear systems, the research on chaos and chaotic neural networks has grown rapidly in recent years [1–10]. However, the development of chaos and chaotic neural networks mainly focuses on their software algorithm improvement [11–18], the hardware implementation of chaos and chaotic neural networks has fallen far behind their software algorithm. Facing with this issue, the research on hardware circuits implementation of chaos and chaotic neural networks becomes increasing important. Chaos has been investigated widely in the last decades and they become increasing interest subjects because of their great potential applications in many fields such as chaotic signal radar [19], secure communications [20–24], chaos-based analog-to-information conversion and image encryption applications [25]. The double-scroll Chua system is the first physical circuit realization of chaos. Since then, other chaotic and hyperchaotic systems with complex chaotic attractors and nonlinear dynamical characteristics have been realized [26–31], and most of them are validated with commercial available discrete electronic components or digital signal processing (DSP) and field programmable gate array (FPGA) [32–42].

Most of the reported and physical implemented chaotic systems are realized using off-the-shelf electronic components with breadboards. The breadboard-based chaotic circuits are suitable for theoretically proving the existence and realizability of chaos, they are non-portable and unstable, and far from the practical application of chaos. Unlike the conventional breadboard-based chaotic circuits, the fully integrated chaotic systems are more stable and convenient than their breadboard-based counterparts. Chaotic systems fully integrated on a single chip should be the development direction of chaotic circuits, and the fully integrated chaotic circuits will greatly enhance the practicality of chaos. For example, two CMOS Chua's chaotic circuits were reported in Ref. [43], another 2 μm CMOS process integrated chaotic system with high speed operation was introduced Ref. [44], and an integrated multi-scroll chaotic oscillator generating 3- and 5-scroll attractors was reported in Ref. [45].

Because of its simple circuit structure and easy to be theoretically proven, the famous Chen chaotic system

[46–50] and its deformation circuits are deeply studied in the past decades. Several realization and implementation of Chen chaotic circuits are presented in Ref. [50], however, these circuits are also realized using commercial available discrete electronic components with breadboards. Based on the existing Chen chaotic circuits and systems, a low voltage low power fully integrated classic Chen chaotic oscillation system is realized in this paper. The post-layout simulation results verified that the fully integrated Chen chaotic oscillation system is feasible and achievable. In addition, the main contributions of this work can be summarized below.

1) An operational amplifiers (OA) and an analog multiplier with GlobalFoundries' 0.18 μm CMOS 1P6M process are designed in this work.
2) Unlike the conventional breadboard-based chaotic circuits, a fully integrated Chen chaotic oscillation system using the designed OA and multiplier is presented.
3) The fully integrated Chen chaotic system is verified with Cadence IC Tools. The post-layout simulation results demonstrate that the whole power consumption of the fully integrated Chen chaotic system is about 148 mW, its chip area is only 6.15 mm^2, and the fully integrated Chen chaotic circuit is a more suitable candidate for practical applications.

2. Fully Integrated Chen Chaotic Circuit

The design of fully integrated Chen chaotic circuit is presented in this section. The original Chen chaotic system and its fully integrated circuit is introduced in subsection 2.1, and the implementations of operational amplifier and analog multiplier are introduced in subsection 2.2 and 2.3, respectively.

2.1. Chen Chaotic System. The classic dimensionless state equations of the Chen system can be depicted as follow:

$$\begin{cases} \dfrac{dx}{dt} = a(y - x) \\ \dfrac{dy}{dt} = (c - a)x - xz + cy, \\ \dfrac{dz}{dt} = xy - bz \end{cases} \tag{1}$$

where *a, b* and *c* are all constants, and a = 35, b = 3, c = 28. When the initial condition is (0, 0, 0), the Matlab numerical simulation results of Chen system are presented in Fig 1, and the chaotic attractors are observed as shown in Fig. 1(a)-(c).

Because the supply voltage of the fully integrated Chen chaotic oscillation system are ±2.5 V, and the output ranges of state variables x, y and z in Fig 1 all exceed ±2.5 V, state variables compression are necessary. After evenly compressed 40 times of the state variables, the state equations of the Chen system could be expressed as:

$$\begin{cases} \dfrac{dx}{dt} = 35(y - x), \\ \dfrac{dy}{dt} = -7x - 40xz + 28y, \\ \dfrac{dz}{dt} = 40xy - 3z. \end{cases} \tag{2}$$

Let $\tau = \tau_o \times t$, and $\tau_o = 10000$, and the state equations of the Chen system could be rewritten as:

$$\begin{cases} \dfrac{dx}{dt} = 100000(3.5y - 3.5x), \\ \dfrac{dy}{dt} = 100000(-0.7x - 4xz + 2.8y), \\ \dfrac{dz}{dt} = 100000(4xy - 0.3z). \end{cases} \tag{3}$$

Based on the existing circuit realizations of Chen chaotic systems, a simplified Chen chaotic oscillation circuit suitable for integration is presented in Fig. 2.

Assuming the gains of the multipliers are all *k*, and the circuit equation of Fig. 2 could be expressed as:

$$\begin{cases} \dfrac{dx}{dt} = \dfrac{1}{R_4C_1}\left(-\dfrac{R_3R_6}{R_1R_5}x + \dfrac{R_3}{R_2}y\right), \\ \dfrac{dy}{dt} = \dfrac{1}{R_{11}C_2}\left(-\dfrac{R_6R_{10}}{R_5R_7}x - \dfrac{kR_6R_{10}}{R_5R_8}xz + \dfrac{R_{10}}{R_9}y\right), \\ \dfrac{dz}{dt} = \dfrac{1}{R_{15}C_3}\left(\dfrac{kR_{14}}{R_{12}}xy - \dfrac{R_{14}R_{17}}{R_{13}R_{16}}z\right). \end{cases} \tag{4}$$

2.2. Implementation of Operational Amplifier. The designed OA for the integrated Chen chaotic oscillation circuit is shown in Fig. 3. The designed operational amplifier is very simple, and its supply voltages are $V_{CC} = -V_{SS} = 2.5$ V, and it includes two amplification stages and one bias stage.

The transistors M_7-M_{11} consist of the differential amplification input stage; M_{13} is the second common source amplification stage, and M_{12} is the active load of M_{13}; the transistors M_1-M_6 consist of the bias stage of the OA, and the transistor M_{14} and capacitor *C* are used for frequency compensation.

The simulated voltage gain and phase frequency characteristics of the OA are shown in Fig. 4. From the mark M_0, we can know that the voltage gain of the OA is about 30dB; From the marks M_0 and M_1, we can calculate that the 3dB bandwidth of the OA is 218.5 kHz; From the marks M_2 and M_3, we can know that the phase margin of the OA is about 86.22°. The power consumption of the OA is about 5.85 mW.

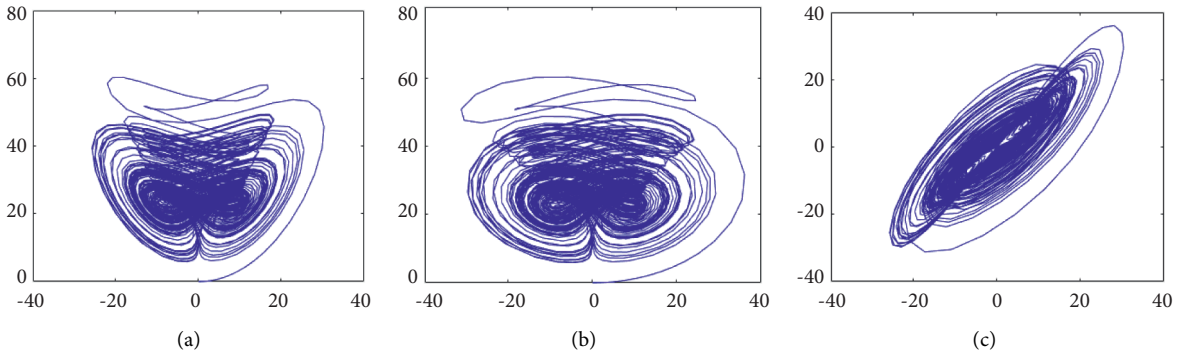

Figure 1: Numerically simulated phase portrait of Chen's attractors: (a) x-z plane, (b) z-y plane, and (c) y-x plane.

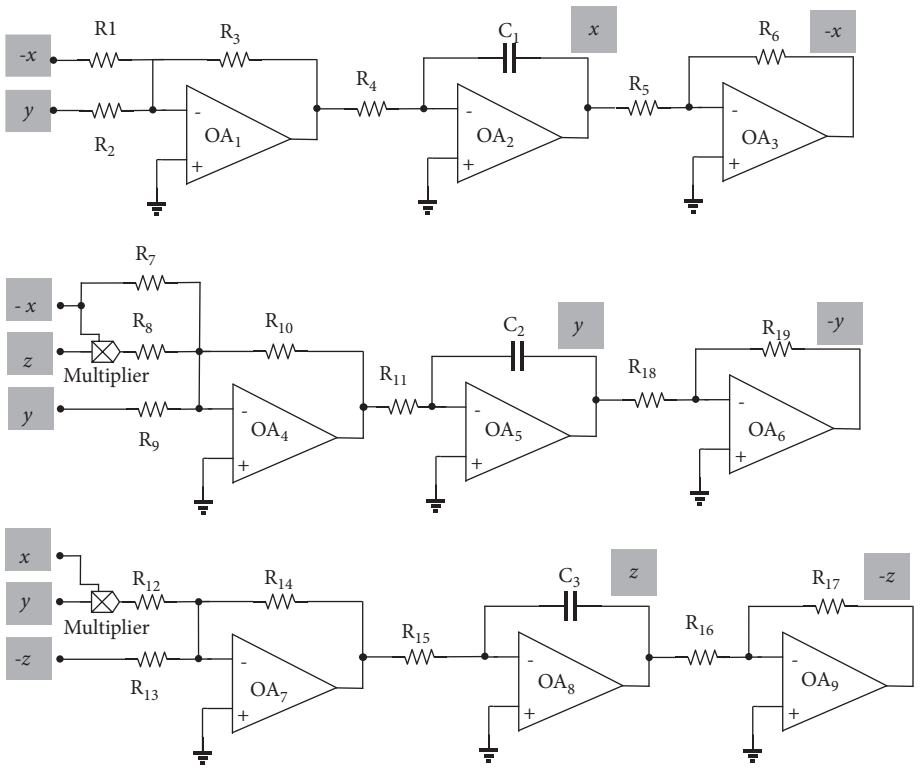

Figure 2: The fully integrated Chen chaotic oscillation circuit.

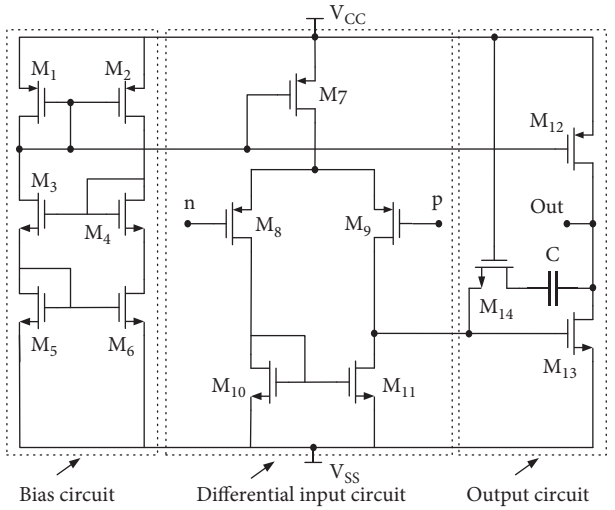

Figure 3: The designed OA.

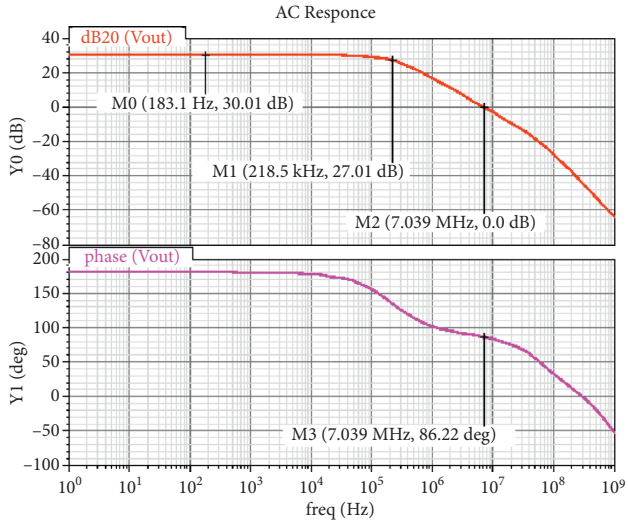

Figure 4: Voltage gain and frequency characteristics of the OA.

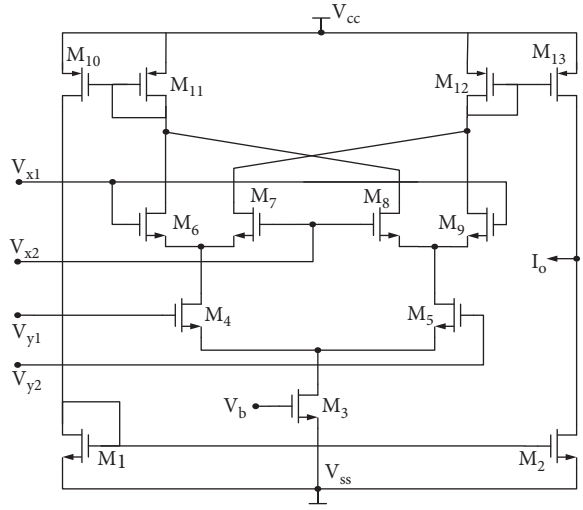

Figure 5: The designed analog multiplier.

2.3. Implementation of Analog Multiplier. The analog multiplier used in the integrated Chen chaotic oscillation circuit is shown in Fig. 5. The classic Gilbert structure is adopted, M_1 and M_2 consist of the current mirror, and they are the bias stage of the multiplier; M_3 works on its saturation region (also known as amplification region), which can be approximated as a current source to provide bias current for the transconductance stage (M_4 and M_5); M_4 and M_5 consist of the transconductance stage, M_6-M_9 consist of the Gilbert switch stage [51–53], and M_{10}-M_{13} consist of the load stage of the analog multiplier. The supply voltages of the multiplier are $V_{CC} = -V_{SS} = 2.5$ V, and its power consumption is about 47.7 mW.

The transient response of the designed analog multiplier is presented in Fig. 6. V_{i1} and V_{i2} are the two input voltages, their input powers are all -10 dBm, and their frequencies are 100 MHz and 10 MHz, respectively. V_{out} is the output voltage of the analog multiplier. From the above simulation results, it is clear that V_{i1} is the high frequency carrier, V_{i2} is the low frequency input signal, and the multiplication is realized in the output voltage V_{out}. From the marks M_0-M_3 in Fig. 6, peak voltages of V_{i1} and V_{i2} are all about 200 mV, and the peak voltage of V_{out} is about 4mV. According to $V_{out} = k \times V_{i1} \times V_{i2}$, it is clear that the parameter k in equation (4) is about 0.1.

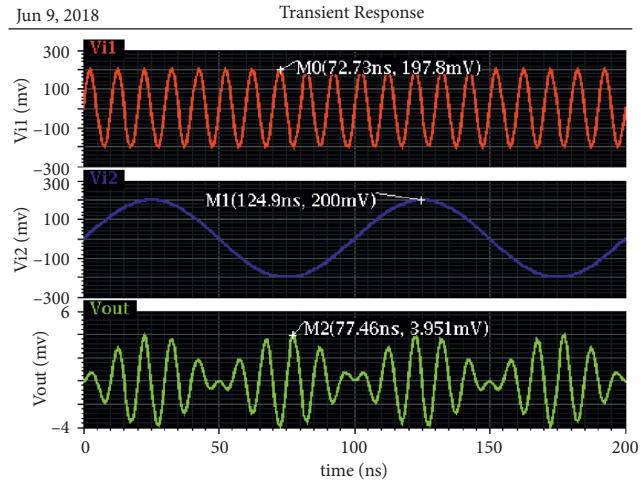

Figure 6: The transient response of the analog multiplier.

3. Post-Layout Simulation Results of the Integrated Chen Chaotic Oscillation Circuit

The presented fully integrated Chen chaotic oscillation circuit in Fig. 2 is simulated and verified using Cadence IC Tools with GlobalFoundries' 0.18 μm CMOS technology. The supply voltages of the fully integrated Chen chaotic circuit are ±2.5 V, and its whole static power consumption is about 148mW. Considering equations (3) and (4), the values of circuit elements are selected as $R_1 = R_2 = 2.85$ kΩ, $R_3 = R_5 = R_6 = R_{10} = R_{14} = R_{16} = R_{17} = R_{18} = R_{19} = 10$ kΩ, $R_4 = R_{11} = R_{15} = 200$ kΩ, $R_8 = R_{12} = 0.25$ kΩ, $R_7 = 14.28$ kΩ, $R_9 = 3.57$ kΩ, $R_{13} = 33.33$ kΩ, $C_1 = C_2 = C_3 = 50$ pF.

The chip layout diagram of the Chen Chaotic oscillation system is shown in Fig. 7, and its chip area is 6.15 mm^2 including all the testing pads.

The Mentor Calibre software is used for circuit verification and parasitic extraction. Based on the layout of the Chen chaotic oscillation circuit in Fig. 7, and connecting the extracted parasitics to the original circuit in Fig. 2, the post-layout simulation results of the integrated Chen chaotic oscillation circuit are presented in Figs. 8 and 9.

Fig. 8 is the transient response of the fully integrated Chen chaotic circuit, and various dynamical oscillations can be observed. From Fig.8, it is clear that the peak amplitudes of output voltages x, y and z are all less than 2 V. Fig. 9 is the phase portraits in x-z, z-y and y-x planes. By comparing Figs. 1 and Fig. 9, a good qualitative agreement between the post-layout chip circuit simulation and numerical simulation is observed.

There are nine operational amplifiers and two multipliers used in the Chen chaotic oscillation circuit. According to the data sheets of operational amplifier LF347 and multiplier AD633JN in Refs. [51–55], the supply voltage of LF347 is

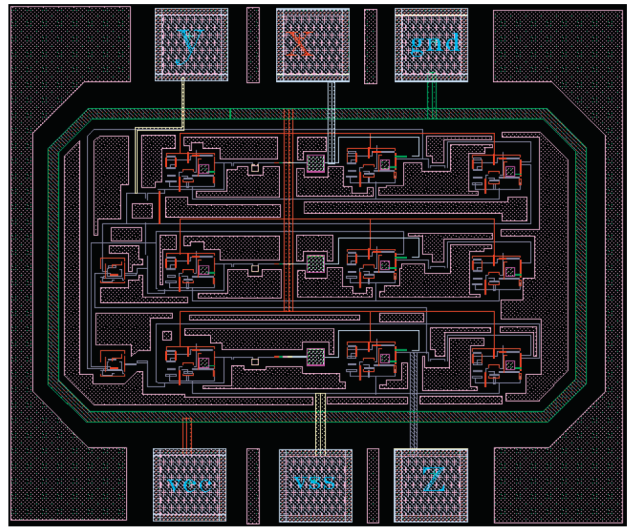

Figure 7: Chip layout diagram of the Chen chaotic oscillation circuit.

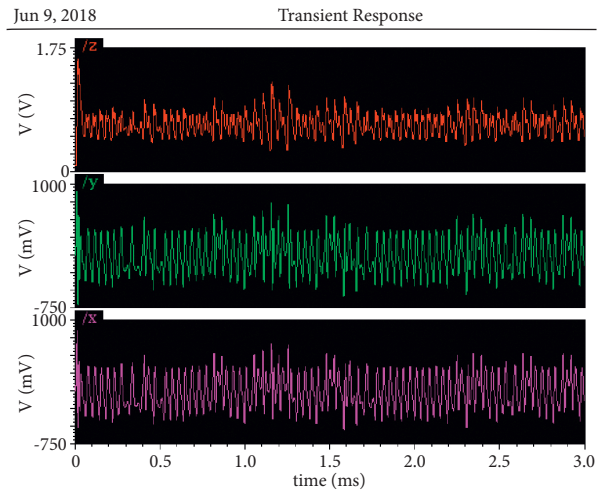

Figure 8: Transient response of the Chen chaotic circuit.

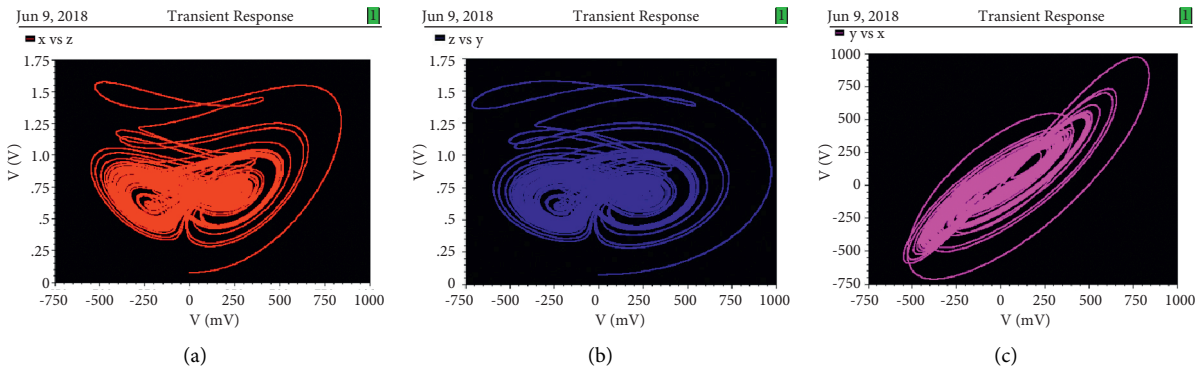

Figure 9: Phase portraits of the Chen's attractor in (a) x-z plane, (b) z-y plane, and (c) y-x plane.

±18 V, and its power consumption is about 500 mW; the the supply voltage of AD633JN is also ±18 V, and its power consumption is also about 500 mW. If the Chen chaotic circuit is realized using commercial available chips LF347 and AD633JN, the whole power consumption is about 5500 mW.

The supply voltage of the fully integrated Chen chaotic oscillation circuit is ±2.5 V, the whole power consumption is

about 148 mW, and its chip area is only 6.15 mm^2. Compared with the conventional realizations using commercial available discrete electronic components with breadboards, the fully integrated Chen chaotic oscillation circuit is a more suitable candidate for practical applications.

4. Conclusion

In this paper, a fully integrated Chen chaotic oscillation system using OAs and multipliers is designed and verified. Unlike the conventional realization using commercial available discrete electronic components with breadboards, the designed Chen chaotic oscillation system is integrated in a single chip. It has the advantages of smaller chip area, lower supply voltage and power consumption. Moreover, it has practical application prospects in demanding portable chaos systems. Besides, it should be further developed from the following objectives to improve the practicability of the fully integrated chaotic circuit. Firstly, other OA and transconductance operational amplifier (OTA) with simpler circuit structures and lower power consumption should be designed to further improve the performance of the fully integrated chaotic circuit. In addition, the realization of integrated chaotic circuits with complex chaotic attractors and nonlinear dynamical characteristics is also considered in our future works.

Data Availability

All data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest in this work.

Acknowledgments

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