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*Research Article*

# The Design and Process Reliability Analysis of Millimeter Wave CMOS Power Amplifier with a Cold Mode MOSFET Linearization

**N. A. Quadir**,[1] **Amit Jain**,[2] **S. Kashfi**,[1] **Lutfi Albasha**,[1] **and Nasser Qaddoumi**[1]

[1]*American University of Sharjah, Sharjah, UAE*
[2]*CMR Institute of Technology, Bengaluru, India*

Correspondence should be addressed to N. A. Quadir; nquadir@aus.edu

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A power amplifier design operating at 28 GHz for communication applications is presented in this paper. Analog predistorted technique is used to improve the linearity using a cold mode MOSFET linearizer. The paper reports +19.8 dBm of peak power at the output and power-added efficiency (PAE) of 17% is attained by the designed circuit. The 1-dB compression point linearity was +18.6 dBm. The adjacent channel power ratio (ACPR) simulations were performed for the different communication standards like 802_11n_40M, CDMA, IS-95, and 802_11n_20M. Design specification variations of the amplifier have been analyzed over five process corners and simulations were performed to validate compliance with standards and robustness of the designed circuit. Monte Carlo simulation were performed to assess the performance over statistical variability of PAE and power gain. It is believed that this linearization design and the verifications used are done for the first time on a 65-nm RFCMOS process.

## 1. Introduction

Bandwidth and modulation play significant roles in designing power amplifiers for high-speed communications. This helps in delivering faster and superior RF (radio frequency) performances. Several power amplifier designs are reported without a linearizer, examples include cascode [1–5], three stage common source [6], two stage current mirror [7], and triple stacked single stage transistors [8]. These designs allow for bigger bandwidth, higher gain, and better power handling capabilities. However, linearity is one of the key parameters in the design of power amplifier to overcome distortion of the transmitted signal. Several design techniques are reported in the literature to improve power amplifiers linearity [9–12]. Applications where operating frequency is less than 10 GHz, linearization techniques such as feed forward and cartesian feedback are mostly used [13]. However, these systems are complex and less suitable for handset integration. Predistortion techniques may offer a better and lower cost alternative with the linearizer employed in predistortion techniques models the inverse characteristic of the nonlinearities in the power amplifier to compensate for linearity and gain. In higher frequency bands, the circuits using digital predistortion technique consumes more power due to higher clock rates. Hence analog predistortion [14–16], which can be divided as active and passive, are seen as a better alternative. Passive analog predistortion is less complex compared to its active counterpart and does not obviously add any gain, however it does improve the linearity, and is considered as a better option for high-frequency applications [17–21].

A dual stage power amplifier integrated with analog linearizer circuit on a single substrate is presented in this paper. The performance of the designed circuit is presented across process, voltage and temperature variations with Monte Carlo simulations results to assess the long-term reliability of the proposed amplifier.

## 2. Proposed Design

Figure 1 depicts the schematic of the design that consists of biasing network, input and output impedance matching circuit and the integrated linearizer circuit with the power

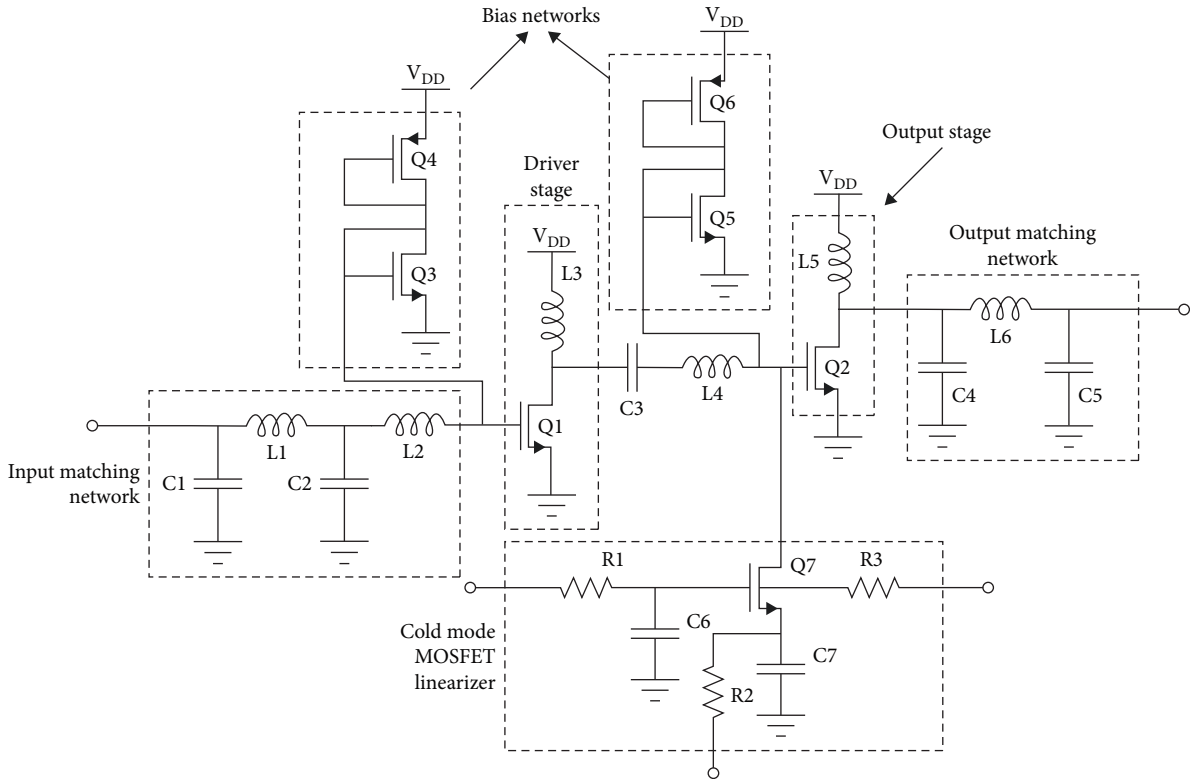


FIGURE 1: Proposed power amplifier.

amplifier. For the design of impedance matching of inter and input stage, small signal S-parameter analysis is used. Stability of the designed power amplifier is improved by using a resistor in the interstage impedance matching network. The resistor slightly reduces the gain and hence boosts the amplifier stability. Furthermore, all the component values are optimized in the matching network to achieve the desired result. Transistors Q3, Q4, and Q5, Q6 form the 1st and 2nd stage of the biasing circuit, respectively. The biasing circuits are basically simple voltage divider circuits. This helped to ensure lower power consumption and hence improving the efficiency of the amplifier. Proper care is taken in choosing the values of these biasing transistors, to avoid loading the previous stages with more parasitic capacitance. Table 1 provides the values of all the components used in the design.

In the design of a power amplifier following steps are taken:

(1) At first the output stage is designed, where maximum voltage swing allowed for the given technology is determined from the load line graphs, such that the drain voltage swings equally between $V_{\max}$ and $V_{\mathrm{DS,sat}}$ centered at power supply. Maximum voltage swing is governed by the breakdown for the given technology used and is given by

$$V_{\mathrm{out}} = V_{\max} - V_{\mathrm{DS,sat}}. \quad (1)$$

(2) Based on the output voltage swing and $P_{1\,\mathrm{dB}}$ requirements, biasing current of the transistor is set and from that aspect ratio of the transistors are obtained.

TABLE 1: Values of all the components.

| Component | Value |
|---|---|
| Q1 | 245 $\mu$m/90 nm |
| Q2 | 320 $\mu$m/120 nm |
| Q3 | 320 nm/60 nm |
| Q4 | 125 nm/70 nm |
| Q5 | 2 $\mu$m/60 nm |
| Q6 | 120 nm/85 nm |
| Q7 | 10 $\mu$m/90 nm |
| L1 | 225 pH |
| L2 | 225 pH |
| L3 | 225 pH |
| L4 | 225 pH |
| L5 | 225 pH |
| L6 | 225 pH |
| L7 | 225 pH |
| R1 | 2.4 K$\Omega$ |
| R2 | 2.4 K$\Omega$ |
| R3 | 2.4 K$\Omega$ |
| C1 | 550 fF |
| C2 | 100 fF |
| C3 | 100 fF |
| C4 | 205 fF |
| C5 | 70 fF |
| C6 | 9 pF |
| C7 | 75 fF |
| C8 | 75 fF |

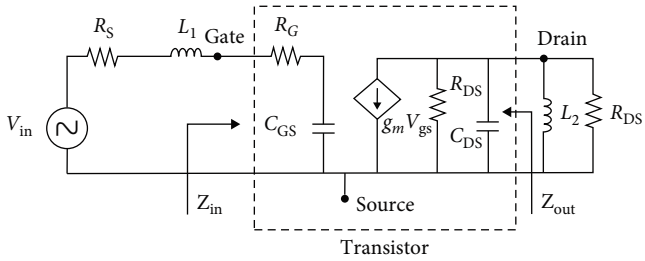


FIGURE 2: Small signal model of individual transistor.

Load-line theory is used to determine $P_{1\,\mathrm{dB}}$ and is given by

$$P_{1\,\mathrm{dB}} = \frac{\left(V_{\mathrm{DD}} - V_{\mathrm{DS,sat}}\right)}{4} \times I_{\mathrm{out}}. \tag{2}$$

For power gain based on the small signal model of the transistor as shown in Figure 2 is given by Equation (2) [22].

$$\mathrm{G} = \frac{\text{Output power}}{\text{Source power}} = \frac{g_m^2 R_{\mathrm{DS}}}{4\omega^2 R_G C_{\mathrm{gs}}^2}. \tag{3}$$

Transistor aspect ratio is designed as such as to maximize the power gain as given by Equation (3). The resistance at the gate must be reduced by implementing less number of finger in the length of the designed gate which is done in the proposed design. The gain of the power amplifier also tends to decrease with the increase in temperature. In order to have minimum effect of temperature on gain the transconductance of the amplifier is designed using the given equations.

$$g_m = \frac{\delta I_{\mathrm{D}}(\mathrm{sat})}{\delta V_{\mathrm{gs}}}, \tag{4}$$

$$= \mu_n(T_0)\left(\sqrt[-\frac{3}{2}]{\frac{T}{T_0}}\right)\frac{\mathrm{WC}_{\mathrm{ox}}}{L}\left(V_{\mathrm{gs}} - V_{\mathrm{t}}\right), \tag{5}$$

where $W$ is the width of the transistor, $\mu_n$ is the mobility of electrons in the NMOS transistor, gate oxide capacitance is given by $C_{\mathrm{ox}}$, length of the transistor is given by $L$, gate-source voltage is given by $V_{\mathrm{gs}}$, and threshold voltage is denoted by $V_{\mathrm{t}}$, $T_0$ is 300 K, and $T$ is the operating temperature.

(3) After that output matching network is designed for the last stage and for the preceding stages to maximize power transfer.
(4) Same steps are repeated for the design of the preceding stages.
(5) Input stage is then matched to $Z_{\mathrm{o}} = 50$.
(6) Cold-mode MOSFET technique to increase the linearity is then implemented.

A linearizer technique of cold-mode MOSFET [14–20] is implemented in the design. It not only improves the linearity of the design but also improves the gain at higher frequency bands. The linearizer circuit consists of MOSFET Q7, three resistors R1, R2, and R3 and two capacitors C6 and C7 as noticed from Figure 1. The resistors are being used as the bias feed for the respective bias circuits and capacitors are used as bypass capacitors. The designed linearizer circuit successfully implements the desired predistortion characteristics by using the difference in I–V characteristics slope between linear and saturation region. To achieve better linearity, gate voltage at the driver transistor must be equal to the source potential of the transistor used for linearization [21, 23, 24] Cold-mode linearizer's equivalent circuit [25–27] is shown in Figure 3, in which the circuit is represented as the combination of two parallel branches, where one consists of a variable resistor $R_{\mathrm{ds}}$ and the other is a series connection of resistor $R_{\mathrm{eq}}$ and capacitor $C_{\mathrm{eq}}$. $R_{\mathrm{ds}}$ represents the active device Q7 whose resistance is proportional to the power level of the input, which in turn results in the gain expansion characteristics. Considering the variations of $C_{\mathrm{eq}}$ and $R_{\mathrm{eq}}$ to be much smaller than the variation of $R_{\mathrm{ds}}$ the gain $S_{21}$ is expressed by Equation (6):

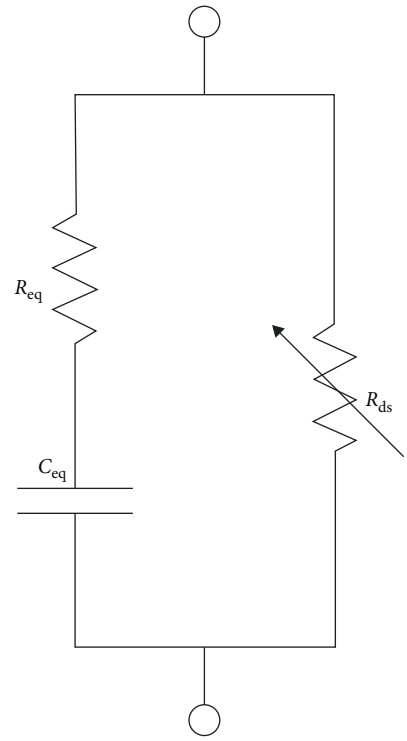


FIGURE 3: Cold mode linearizer's equivalent circuit.

$$S_{21} = \frac{2}{2 + Z_0\left(\frac{1}{R_{\mathrm{ds}}} + \frac{1}{\left(\frac{1}{j\omega C_{\mathrm{eq}}} + R_{\mathrm{eq}}\right)}\right)}, \tag{6}$$

where $50\,\Omega$ characteristics impedance is denoted by $Z_0$ and $R_{\mathrm{ds}}$ (drain to source resistor). Equation (7) shows that at low-input power, $R_{\mathrm{ds}}$ is almost constant due to linear region operation of the transistor and increase in $R_{\mathrm{ds}}$ happens near the saturation region (pinch-off voltage), when the

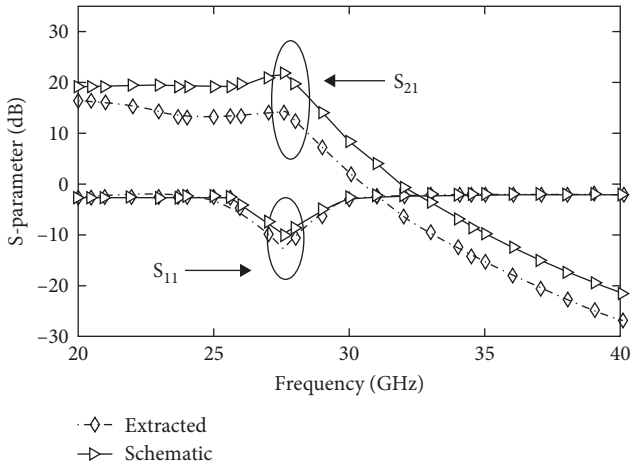


FIGURE 4: S-parameter plot of $S_{11}$ and $S_{21}$.

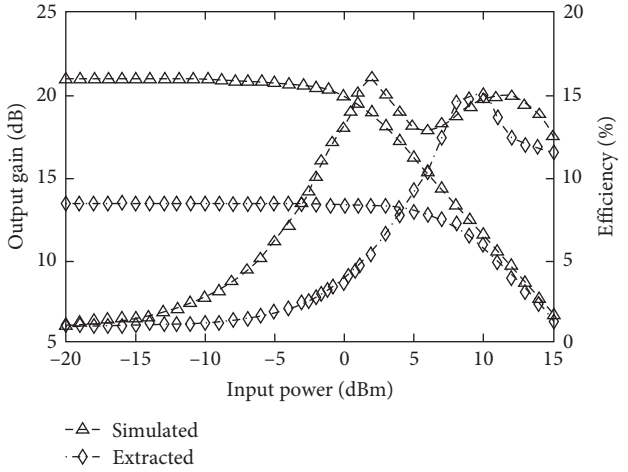


FIGURE 5: Power-added efficiency and output gain.

input power is high. It can be perceived that increased $R_{ds}$ results in gain expansion which is the most important parameter of linearizer and is expressed as follows:

$$R_{ds} = \frac{1}{\frac{\partial I_{ds}}{\partial V_{ds}}}. \tag{7}$$

## 3. Results

The proposed circuit has been designed in 65-nm CMOS technology with both simulated (without parasitic components) and extracted (with all the parasitic RC components) views compared for various important parameters of PA. S21 (gain) and S11 (input reflection coefficient) are depicted in Figure 4; S21 peak is achieved at 28 GHz after which it starts to gradually reduce. It can be observed from the figure that the simulation and extracted result for input reflection coefficient remains almost the same for the entire frequency range.

The overall power gain (Equation (8)) of the designed circuit is illustrated in Figure 5, for the input power ranging from −20 to 15 dBm.

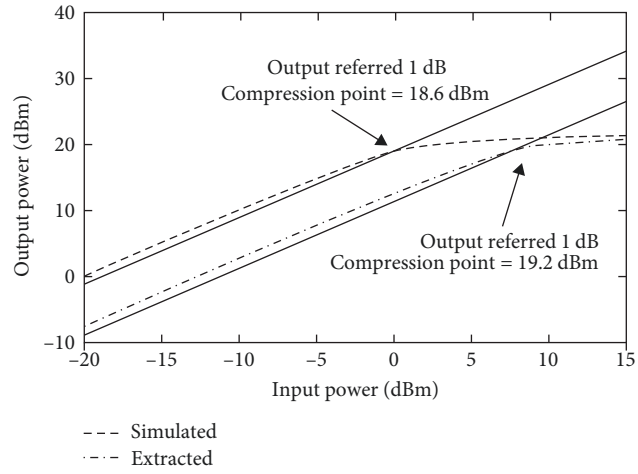


FIGURE 6: Linearity analysis using 1-dB compression point.

$$A = (\text{Output power})/(\text{Input power}) = P_{out}/P_{in}, \tag{8}$$

where overall power gain is expressed by $A$ and $P_{in}$ and $P_{out}$ are the input and output power levels, respectively.

The result shows the power gain of 21 dB whereas the extracted result is obtained as 14 dB. The difference in the achieved powers shows the effect of the additional parasitics the layout has generated based on the process PDK, and its impact on the output matching.

The power-added efficiency (PAE) (Equation (9)) for the designed circuit with linearizer is obtained as 17% as plotted in Figure 4.

$$\text{PAE} = (P_{out} - P_{in}/P_{DC} = (1 - 1/A)P_{out}/P_{DC} = (1 - 1/A)\eta. \tag{9}$$

The linearity of the designed circuit is assessed by plotting the 1-dB compression point versus the input power levels. As observed in Figure 6 the 1-dB compression point achieved was 19.2 and 18.6 dBm for simulated and extracted circuits, respectively.

The ACPR given by Equation (10) is an important metric used to quantify the nonlinear behavior displayed by the power amplifier that normally comes into picture when PAs are operated beyond their linear region at slightly compressed mode, to increase its efficiency.

$$\text{ACPR} = \frac{\text{Power in the adjacent channels}}{\text{RMS power in the channel.}} \tag{10}$$

ACPR with and without built-in linearizer is shown in Figures 7 and 8, respectively, showing clear improvement in linearity.

To obtain ACPR for various standards, the offset frequency and the channel bandwidth (main) is kept at 20 MHz [28]. It can be observed that the ACPR value reduces as the input power level reaches 1-dB compression point. Figure 9 demonstrates the ACPR values of the power amplifier with and without linearizer. It is evident from the plot

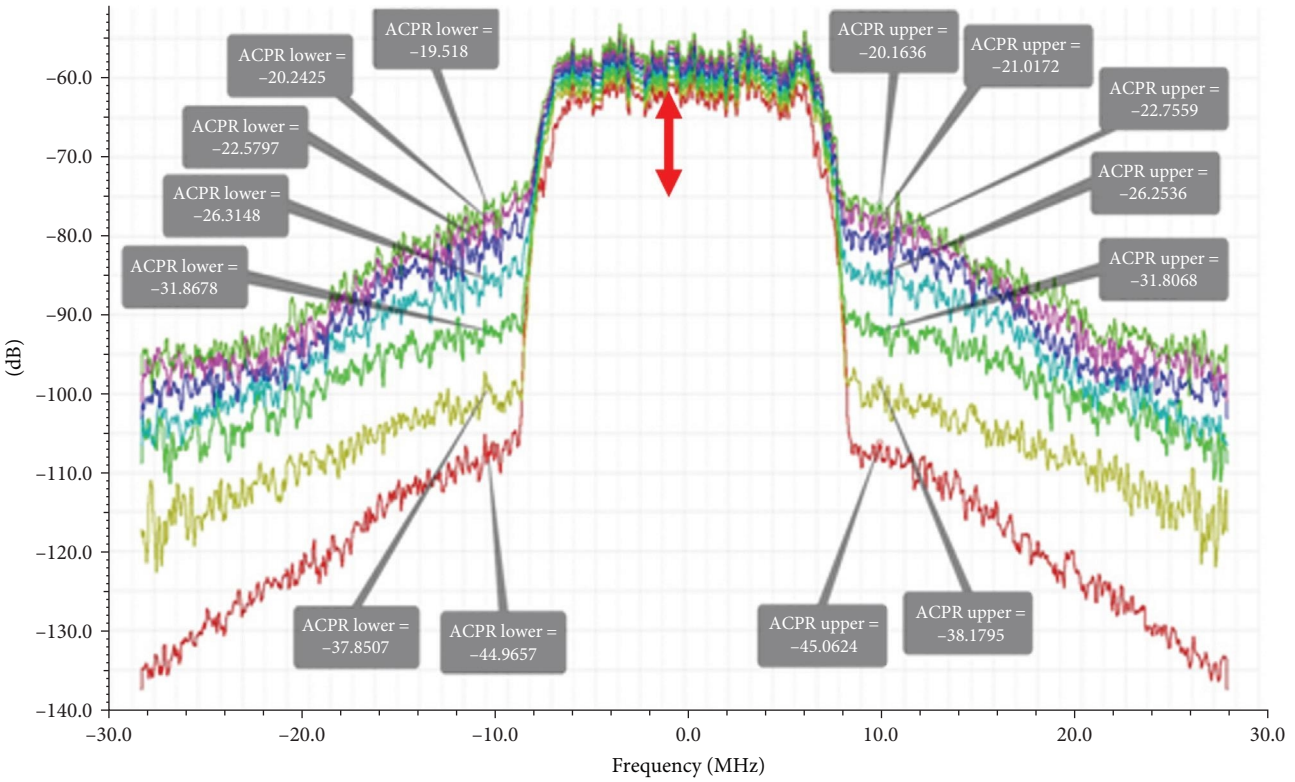


Figure 7: ACPR analysis for 20-MHz bandwidth with 802.11*n* wireless standard (without linearizer). Red arrow shows ACPR to be approximately 15 dBc.

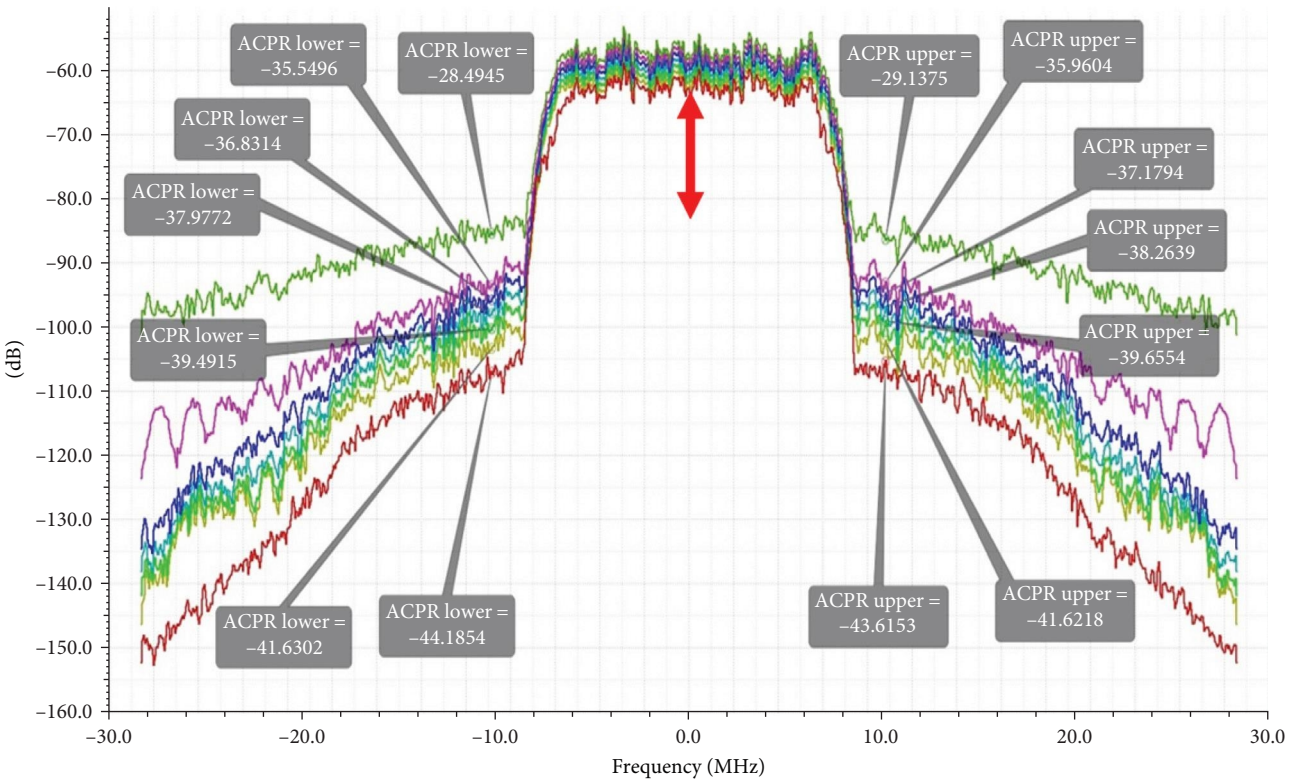


Figure 8: ACPR analysis for 20 MHz bandwidth with 802.11*n* wireless standard (with linearizer, showing better linearity). Red arrow shows ACPR to be approximately 25 dBc.

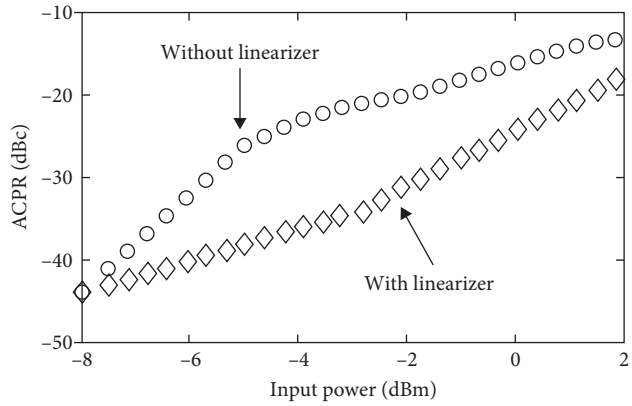


Figure 9: ACPR (with and without linearizer) for the designed circuit.

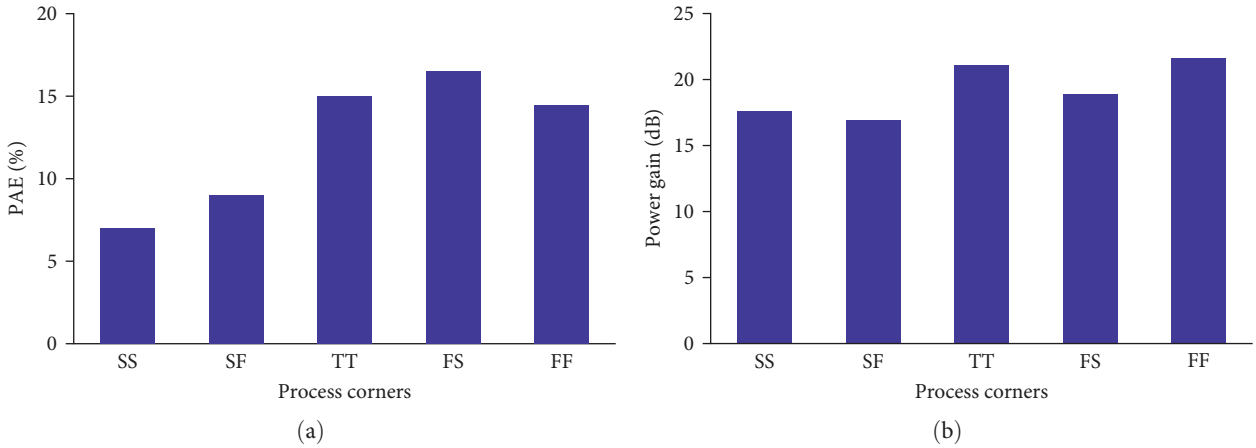


Figure 10: The effect of process corners on (a) PAE and (b) power gain.

that the ACPR values significantly improves till 1-dB compression point.

Emphasis on reliability and PVT (process, voltage, and temperature) variations were discussed in the recent works [29–33]. To evaluate the designed circuit for these corners, Monte Carlo simulations were performed across five corner simulations (SS, SF, TT, FS, and FF). Figure 10 illustrates the effect of process variations on PAE of the amplifier. As noticed from Figure 10(a) the maximum PAE is achieved in fast–slow (FS) corner and minimum PAE is obtained in slow–slow (SS) corner. The design circuit is also simulated for power gain under the process variation (Figure 10(b)). The simulation shows the maximum power gain is achieved as 21.5 dB considering fast–fast (FF) combination, whereas the minimum value of 16.9 dB is obtained for slow–fast (SF) case.

A change of 5 dB is seen across the temperature variation of −40 and 125°C similarly a difference of 5% is seen in PAE across the temperature variation as shown in Figure 11. The maximum PAE of 18.5% is obtained at −40°C, after which the performance degrades with temperature showing the minimum value as 13% at 125°C.

The variation of the power gain with respect to power supply variation is shown in Figure 12. The maximum and minimum values of power gain obtained were 20.3 and 18.5 dB, respectively. The PAE curve shows a parabolic behavior with the maximum value of 17.8%, whereas the minimum value was 15.3%. This is a reasonable amount of PAE given the process capabilities. PVT corner analysis has, hence, confirmed a very good performance of the designed power amplifier in compliance with related standards under variations of temperature, voltage supply and process.

Finally, the designed circuit has been assessed by Monte Carlo simulation (100 runs) to check its performance for various changes across the process. The standard deviation of PAE was measured to be 4.2% with mean value of 15.8% as appears in histogram in Figure 13(a). The reported mean of power gain is 20.5 dB and the standard deviation is 4.5 dB as illustrated in Figure 13(b). This is a particularly good result and is also done for the first time in this work for a linearized power amplifier.

To reduce the chip size and noise in the circuit, lumped elements were not integrated onto the chip [34]. However,

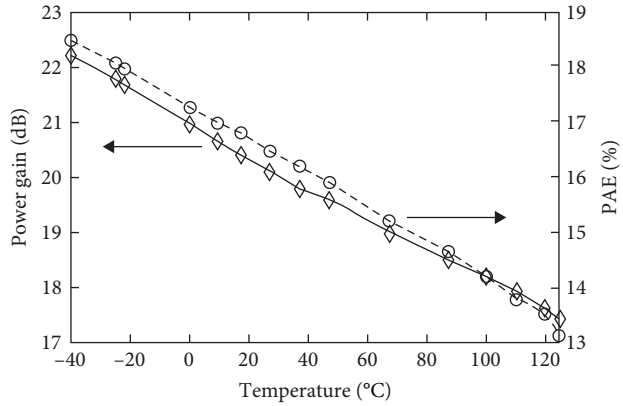


Figure 11: PAE and gain over change in temperature.

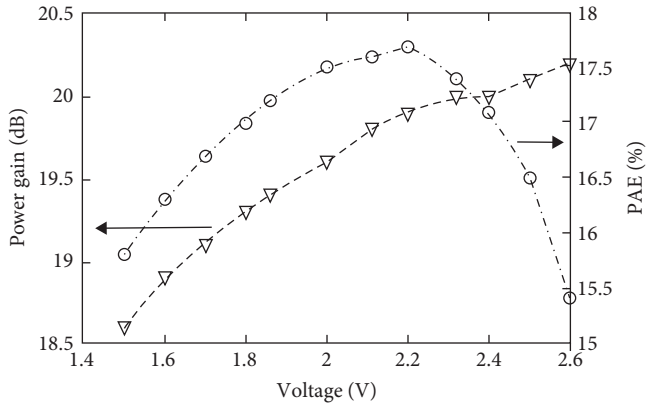


Figure 12: PAE and power gain across power supply variation.

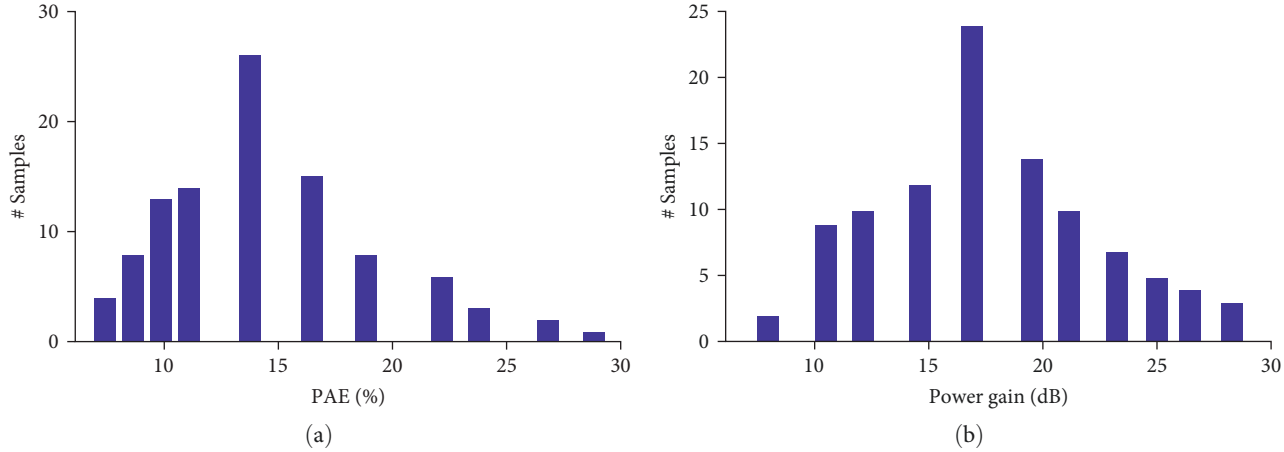


Figure 13: Monte Carlo simulation for (a) PAE and (b) power gain.

while designing these lumped elements the offchip impedances such as board capacitance, wire-bond inductance, and PCB (printed circuit board) line capacitances were taken care of. By keeping these elements offchip, it also enables the tuning ability of the matching network with an added advantage of small chip size and being economical. Layout of the chip is shown in Figure 14 and the size of the entire chip without the offchip components is $525 \times 450\,\mu m^2$.

Table 2 presents a comparison between published work and this design. Most of the work it has been compared to are power amplifiers without any built-in linearizers as most of the design with linearization techniques are operating around

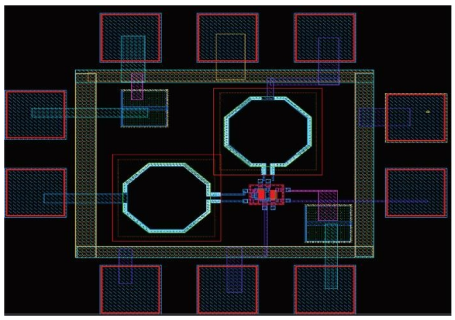

Figure 14: Layout of the chip.

Table 2: Comparison of key parameters with existing power amplifier designs.

| Ref. | Process node (nm) | Freq (GHz) | Gain (dB) | $OIP_{1\text{-}dB}$ (dBm) | PAE (%) | $P_{sat}$ (dBm) | Results |
|---|---|---|---|---|---|---|---|
| Khan and Wahab [1] | 130 | 24 | 6 | – | 30 | 12.5 | Simulated |
| Portela et al. [4] | 180 | 24 | 16.2 | 13.6 | 22.5 | 17.5 | Simulated |
| Jen et al. [5] | 180 | 27 | 14.5 | – | 13.2 | 14 | Measured |
| Chang et al. [8] | 130 | 24 | 12.2 | – | 20.5 | 17.5 | Simulated |
| Kuo et al. [9] | 180 | 22 | 11.9 | 14.3 | 10.7 | 16.8 | Measured |
| Tsai et al. [14] | 90 | 60 | 9.8 | 10.2 | 11.4 | 10.7 | Measured |
| Koo et al. [24] | 130 | 24 | 15.6 | 13.3 | 17.7 | 16 | Measured |
| Shang et al. [34] | 45 | 24 | 18.6 | – | 39.7 | 22.4 | Measured |
| Ciocoveanu et al. [35] | 150 GaAs | 33–37 | 18 | – | – | 26.7 | Simulated |
| This work | 65 | 28 | 21.1 | 18.6 | 17 | 22.4 | Extracted |

2–5 GHz, however the study of Kuo et al. [9] and Tsai et al. [14] are power amplifiers with linearization techniques operating at comparable speed or higher. Adaptive bias technique is used by Kuo et al. [9] to increase the efficiency and linearity, but the design consumes around 108 mW of power which is around 60% more than our design. The design by Tsai et al. [14] uses cold-mode MOSFET linearizer with body biasing technique operating at 60 GHz but the total power consumption of the design is around 102 mW which in comparison to our design is more than 60%. Values of most of the critical parameter achieved by our design is around 50% or more in comparison to the work (built-in linearizers) which have measured results. With reference to Table 2, this work reports the highest 1-dB compression point, with the value of gain, $p_{sat}$ (saturated power level) and PAE are also similar to the numbers which is obtained through other linearizers through the use of cold-mode MOSFET linearizer.

## 4. Conclusions

In this paper a new analog cold-mode linearized power amplifier was designed and evaluated using 65-nm RFCMOS process. An excellent PAE of 17.1% was obtained by the proposed design. A built-in linearizer was used to obtain the $OIP_{1\,dB}$ (output referred $P_{1\,dB)}$ of 18.6 dBm. The linearity in terms of compression point ($P_{1\,dB}$) is better in comparison to the other available work at such frequency. The design has shown at least 10 dB improvement in adjacent channel rejection ratio ACPR of the power amplifier with the linearizer implemented. Maximum small-signal gain of 21.1 dB has been achieved with this design. The result shows that the maximum value of the output power provided by the design is 22 dBm under process and temperature variations. This proves that the design is highly robust against physical and environmental variations. Monte Carlo simulations result, another novel contribution in this work, shows good performance against statistical variations. It confirms that using this analog predistorted technique can be an attractive solution for millimeter wave high-power applications which has been already proved by Tsai et al. [14], however this paper further delve into the process reliability analysis of the power amplifier by providing the PVT variations and Monte Carlo reliability simulation results on the key parameters of the design.

## Data Availability

All the design and results data are available, however due to university's policy we will not able to share it.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

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