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Research Article

A Process Optimization Method of the Mini-LOCOS Field Plate Profile for Improving Electrical Characteristics of LDMOS Device

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In this work, the effects of the mini-local oxidation of silicon (LOCOS) field plate's bottom physical profile on the devices' breakdown performance are analyzed through technology computer-aided design simulations. It is indicated that the "abrupt" bottom profile could certainly do with an optimization. This paper introduces an effective process improvement method by etching bias power adjustment and time reduction. The upgradation of the field plate physical profile has been proved by transmission electron microscope cross-section analysis. The angle for the bottom surface of mini-LOCOS field plate θ_2 is improved from 11.9° to 12.6°, and the thickness ratio of H_{up}/H_{bottom} (field plate oxide thickness for the upper and bottom, respectively) is increased from 71.8% to 76.6%. Finally, the optimized laterally diffused metal oxide semiconductor devices have been fabricated, and both figure of merit curves and safe operation area curves are measured. The specific on-resistance $R_{on,sp}$ could achieve as low as 11.3 mΩ mm^2, while breakdown voltage $BV_{ds,max}$ arrives at 37.4 V, which is nearly 19.3% improved.

1. Introduction

Recently, the semiconductor industry has been extending rapidly to artificial intelligence, the Internet of things, biology, and automotive fields over the current area. The laterally diffused metal oxide semiconductor (LDMOS) devices play increasingly implant roles in power management integrated circuits (PMICs). The PMICs fabricated with the bipolar-CMOS-DMOS (BCD) process own the advantages of high-power density, high speed, and easy integration [1, 2]. Many researches have been published about LDMOS performance enhancement [3, 4]. For example, Hebert et al. [4] majorly focus on specific on-resistance performance improvement, and Gavoshani and Orouji [3] can effectively improve device robustness, including both the self-heating effect and breakdown voltage through a novel triple oxide trench deep gate LDMOS structure.

There are also many research works about novel structures, including surrounded stress dielectric layer LDMOS [2], folded accumulation LDMOS [5], optimized high-temperature oxide field plate, and the decoupled plasma nitridation LDMOS [6], H-shape shallow-trench isolation (STI) field plate LDMOS [7], or even silicon-on-insulator LDMOS [8], and high breakdown voltage devices with new material Ga_2O_3 [9]. These papers provided certain innovative device structures with encouraged $R_{on,sp}$ or $BV_{ds,max}$ performance by simulation results or small amounts of electrical results. However, these structures will bring in a very complex fabrication process and high cost for production. Basically, these ideas are still in the early phase of production and have a long way to step into the large-scale production of integrated circuits.

Therefore, according to the advantages of simple process, low cost, good compatibility, and high reliability, the conventional LDMOS, with the mini-LOCOS field plate structure, is still the first choice for high-performance PMICs chips mass production [10, 11]. However, the mini-LOCOS field plate has a complex physical profile, such as an inherent "abrupt" bottom surface, which will lead to breakdown voltage degradation of the final LDMOS device. Therefore, it is of

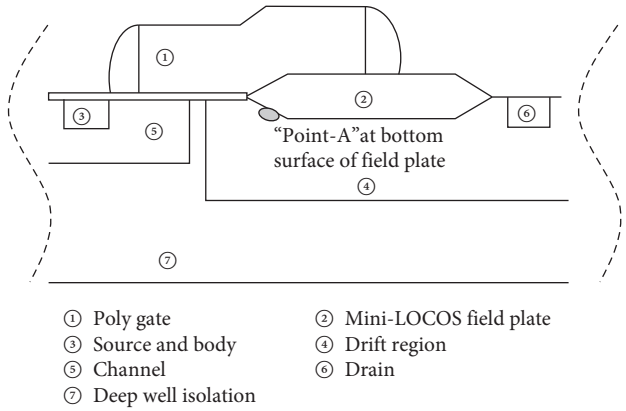


FIGURE 1: LDMOS schematic with mini-LOCOS field plate.

great practical significance for further study and optimization of existing mini-LOCOS field plate processes.

In this paper, an effective process method for mini-LOCOS field plate bottom surface optimization is proposed. The measurement results indicate that the structural profile of the mini-LOCOS field plate has been obviously improved, and the electrical performance, including the figure of merit (FOM) and safe operation area (SOA) curves, is improved accordingly. The principle of the mini-LOCOS field plate technology is shown in Section 2. The experiments and results are shown in Section 3. A conclusion is drawn in Section 4.

2. Studies on "Abrupt" Field Plate Profile

2.1. Process Observations. A brief schematic of the LDMOS [12] device with a mini-LOCOS field plate is shown in Figure 1. During the high-performance BCD platform development in 12-inch Can.-FAB to fabricate the mini-LOCOS field plate, a hard mask approach is applied for field plate photo and etching before high-temperature thermal oxidation. Under this process condition, an inherent defect, called an "abrupt" profile, is observed on the bottom surface of the mini-LOCOS field plate, as shown in Figure 2.

Specific description as follows: the oxide thickness of the mini-LOCOS field plate changes not so smoothly, and an "abrupt" physical profile occurs, which will cause additional charge accumulation Q_A at the bottom surface. Breakdown voltage degradation will be the side effect of Q_A at the "abrupt" location. The related analysis will be raised in Section 2.2.

It is a pity that physical profiles such as transmission electron microscope (TEM) or scanning electron microscope images about mini-LOCOS field plates are not sufficient from published papers. However, the authors still suspect the "abrupt" profile should be a common issue through related industry experiences and some undisclosed benchmark data from other LDMOS device vendors. Another supporting data are the electrical data enumerated in Sections 3.3 and 3.4, which indicate the device FOM performance from the reference vendors still needs to be improved. Thus, our work on process optimization can address the current BCD manufacturing industry with more process solutions.

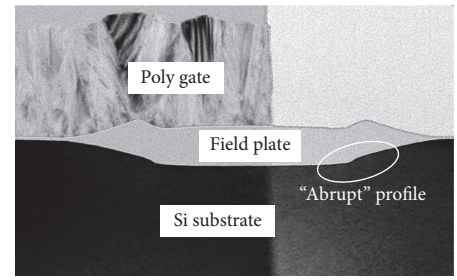


FIGURE 2: Inherent defect on the bottom surface of mini-LOCOS field.

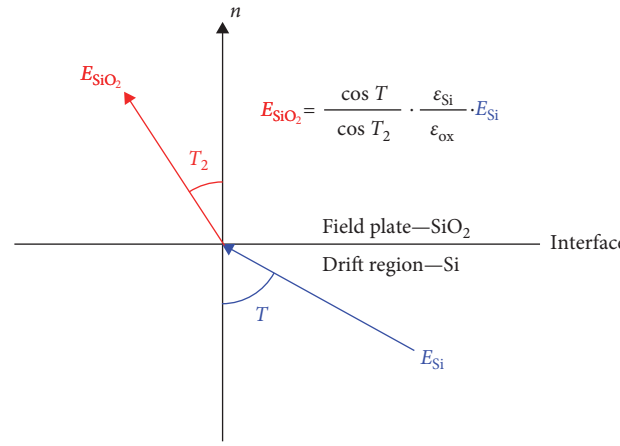


FIGURE 3: Electric field at silicon and oxide interface.

2.2. Theory Analysis. The source-drain breakdown voltage of this device in Figure 1 mainly depends on the electric field distribution of the drift region under the mini-LOCOS field plate [13].

For all types of LDMOS devices with oxide field plate, such as mini-LOCOS field plate, mini-STI field plate, and high-temperature oxide field plate, the source-drain breakdown voltage can be qualitatively expressed [14] as follows:

$$V_{ds} = 3\cos T \cdot E_{si} \cdot t_{ox} + V_{GS} + V_{FB} + V_A, \quad (1)$$

where V_{ds} is the source-drain breakdown voltage of the device, t_{ox} the oxide thickness of the mini-LOCOS field plate, E_{si} the electric field in the Si substrate when the PN junction breaks down, V_{FB} the flat band voltage of LDMOS, V_{GS} the gate bias, V_A the potential at the location A, which close to the bottom surface of the field plate, $\cos T$ the normal component of the potential shift-vector. As signified in Figure 3, take the dielectric constant of oxide $\varepsilon_{ox} = 3.9$, the dielectric constant of silicon $\varepsilon_{Si} = 11.5$, and minimum electric field E_{SiO_2} is acquired when $\cos T_2 = 1$, then we can get the relationship between E_{SiO_2} and E_{si} : $E_{Sio_2} = 3\cos T \cdot E_{si}$.

Further, V_A can be expressed approximately as follows:

$$V_A = \frac{Q_A}{C_{ox}} = Q_A \cdot \frac{\varepsilon_{ox}}{t_{ox}}, \quad (2)$$

where C_{ox} is the normalized capacitance. Considering the thickness t_{ox} variation of different locations of the mini-LOCOS field plate, an integral calculation needs to be carried

out along the bottom surface of the field plate, thus Equation (1) and can be extended as follows:

$$BV_{\mathrm{ds,max}} = \int_0^L \frac{V_{\mathrm{ds}} \cdot W \cdot t_{\mathrm{ox}}}{C_{\mathrm{ox}}}\, dL, \tag{3}$$

where L is the perimeter of the bottom surface of the mini-LOCOS field plate, W is the width of the mini-LOCOS field plate. Combine Equations (1) and (2) into Equation (3), the relation between maximum source-drain breakdown voltage $BV_{\mathrm{ds,max}}$ and the mini-LOCOS field plate oxide thickness t_{ox} and carrier accumulated Q_{A} can be expressed as follows:

$$BV_{\mathrm{ds,max}} \propto ({t_{\mathrm{ox}}}^2 + t_{\mathrm{ox}} + Q_A). \tag{4}$$

In other words, the source-drain breakdown voltage $BV_{\mathrm{ds,max}}$ does not only depend on the thickness t_{ox} of the oxide from the mini-LOCOS field plate but also depends on the charging accumulation Q_A at the bottom surface location and the negative charge accumulation induced by the "abrupt" profile should be eliminated.

2.3. Technology Computer-Aided Design (TCAD) Simulation. For further study on the effects of "abrupt" field plate bottom profile on device performance, TCAD simulation [11, 15] is carried out with the 2-D models of Sivaco software.

Figures 4(a) and 4(b) illustrate the doping profile at the "initial state." The "initial state" means no bias forced on the devices, $V_{\mathrm{g}} = V_{\mathrm{ds}} = 0$ V. At the "initial state," a flat doping profile is considered an ideal profile due to it means less charging accumulation. From Figure 4(c), the comparison results between the "abrupt" field plate and "smooth" field plate, it can be seen the "abrupt" field plate doping profile is not so flat from point "A" to point "B" along the X-axis. Therefore, the doping profile from an "abrupt" field plate could certainly be done with an optimization.

Figures 4(d) and 4(e) illustrate the electric fields at the "off-state," and the "off-state" means high voltage forced to the drain terminal, while the gate terminal and source/body terminal keep zero bias, $V_{\mathrm{gs}} = 0$ V, $V_{\mathrm{ds}} =$ breakdown voltage.

At the "off-state," a lower electric field peak is considered a good distribution due to the higher breakdown voltage that can be acquired. From Figure 4(f), the comparison results between the "abrupt" field plate and the "smooth" field plate, it can be seen the "abrupt" field plate owns a higher electric field at point B. Postoptimization, the electric field peak value from the "smooth" field plate decreases by around 6.3%. That is the reason why "smooth" profile yields higher breakdown voltage. What is more, as shown in Figure 4(d), at the silicon surface and the bottom corner of field plate, electric field spike is observed, which is also an indication for lower breakdown behaviors in "abrupt" field plate.

3. Experiments and Results

3.1. Experiments. Figure 5 is the brief 153 nm BCD process flow in Can.-FAB, which includes seven steps:

Step (1) Deep N-well isolation with an extra high-energy (higher than 3,000 keV) implant, followed by high temperature (higher than 1,100°C) and longtime (more than 4 hr) drive-in.

Step (2) STI formation for device isolation.

Step (3) Drift region implant. Normally, there is no call for additional thermal post this step implant. However, the thermal budget of the following oxidation process, including oxidation/rapid time anneal, etc., should be carefully considered for drift region design.

Step (4) Field plated process. Here, the conventional but low-cost, high-quality mini-LOCOS process is used.

Step (5) Poly gate and self-alignment channel implant (P-body implant).

Step (6) Light doping drain module, then oxide–Si_3N_4–oxide spacer, source/drain engineering process.

Step (7) Back end of the line connection with AlCu metal.

The process of the mini-LOCOS field plate is the most critical process [16, 17]. It can be divided into six steps:

Step (1) ~200 A pad oxide deposition.

Step (2) Silicon-nitride hard mask layer deposition.

Step (3) Lithography field plate region definition.

Step (4) Field plate pattern dry etching is shown in Figure 6(a).

Step (5) Photoresist removal by O_2 asher and $H_2SO_4 + H_2O_2$ wet strip.

Step (6) High-temperature growth (around 900°C, 2 hr, with H_2/O_2) for field plate oxide is shown in Figure 6(b).

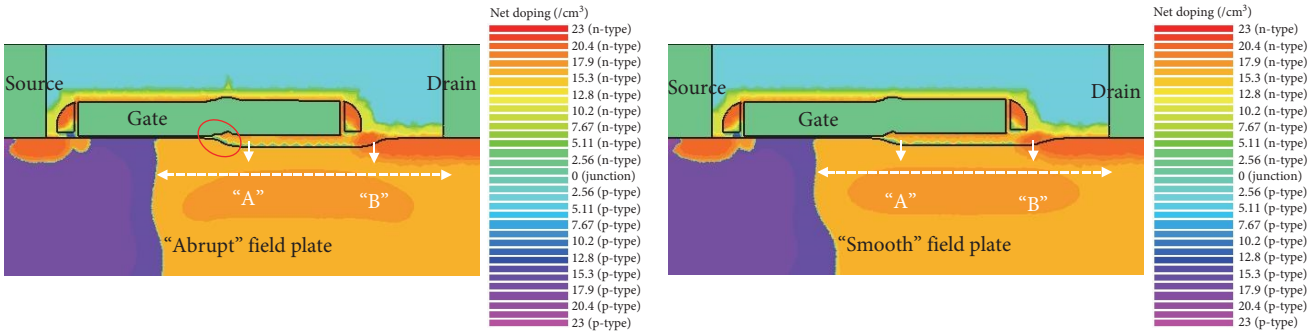
During these process steps, Step (4), dry etching, is the key process. This process has a great impact on the final field plate bottom surface. The reason is that the silicon surface can be easily damaged by the plasma process during dry etching, and then the following oxide growth behavior will be changed accordingly.

Thus, design of experiments (DOE) about silicon loss is designed as shown in Table 1:

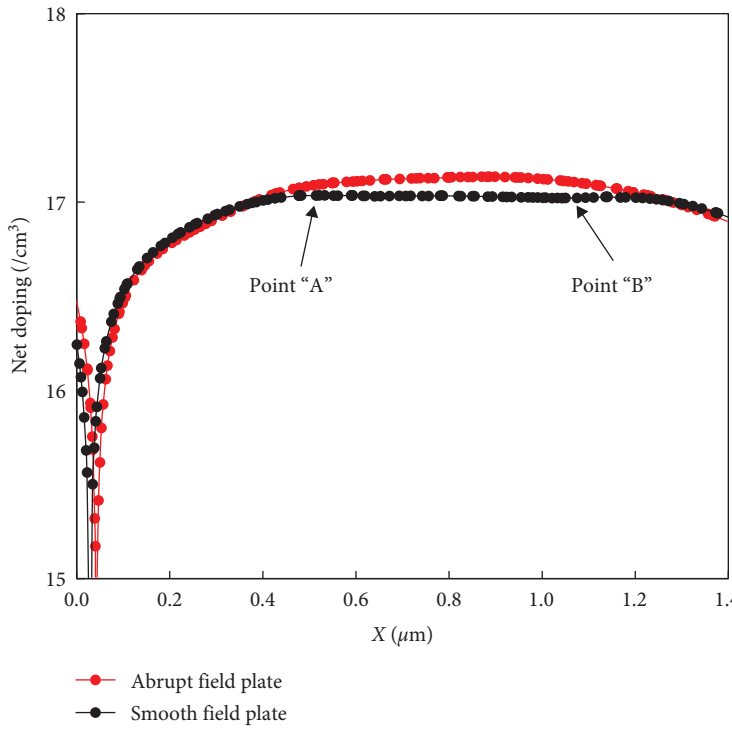
(1) Group 1 is the control group with baseline production process conditions, and the silicon loss is around 200 A;

(2) Group 2 is the bias power reduction group. 12-inch TEL SCCM SE + tool is selected for our experiments. Oxide and nitride etch rates are considered the two critical factors. For reducing the oxide etching amount, bias power is reduced by about 4.2% from hundreds of watts. As a result, the oxide etch rate is reduced to around 15% from more than 400 A/min, while the nitride etch rate keeps less than 10 A/min. Finally, silicon loss is around 100 A in this group.

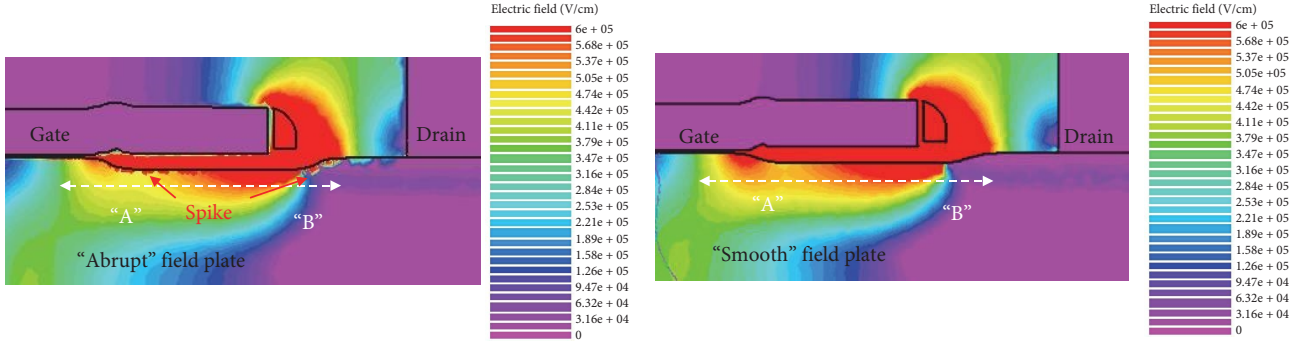
(3) Group 3 is the etching time reduction group, and etching time is reduced by about 12%. As a result, silicon loss is nearly 0 in this group.



(a) (b)

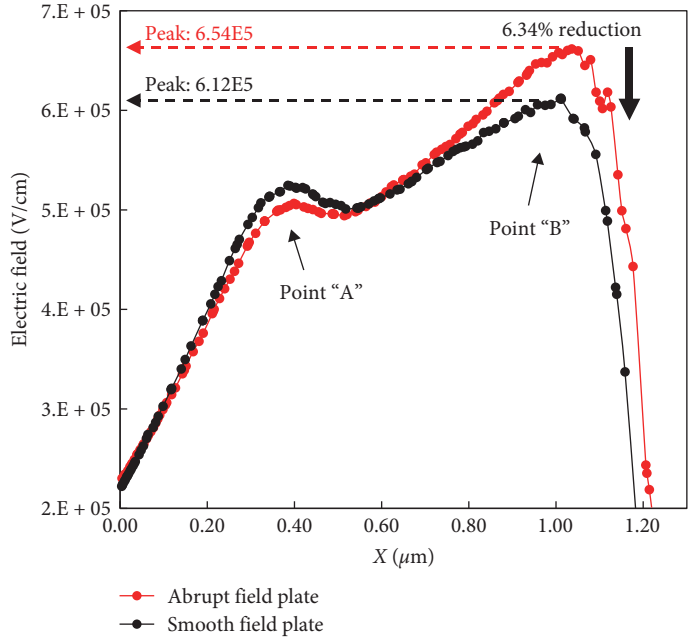


(c)



(d) (e)

FIGURE 4: Continued.



(f)

FIGURE 4: TCAD simulation results of different field plate profiles: (a) net doping simulation of the "abrupt" field plate; (b) net doping simulation of the "smooth" field plate; (c) net doping profile from point A to B; (d) electric field of the "abrupt" field plate; (e) electric field of the "smooth" field plate; (f) electric field from point A to B.

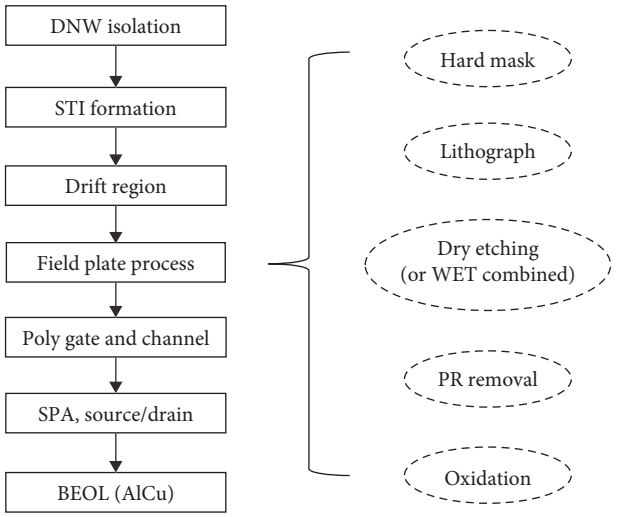


FIGURE 5: 153 nm high-power BCD platform process flow Can.-FAB.

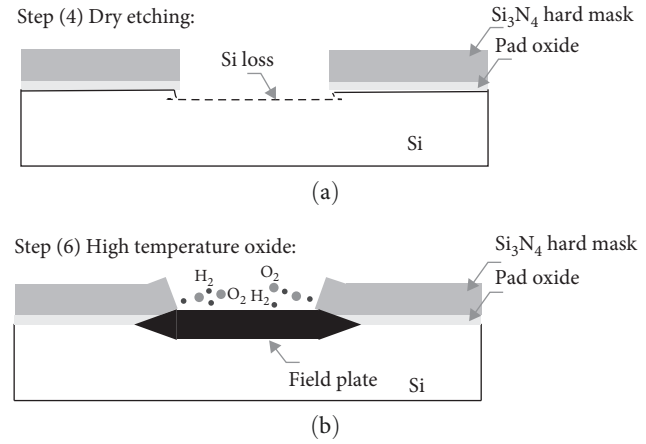


FIGURE 6: Key process schematic for mini-LOCOS field plate: (a) Step (4); (b) Step (6).

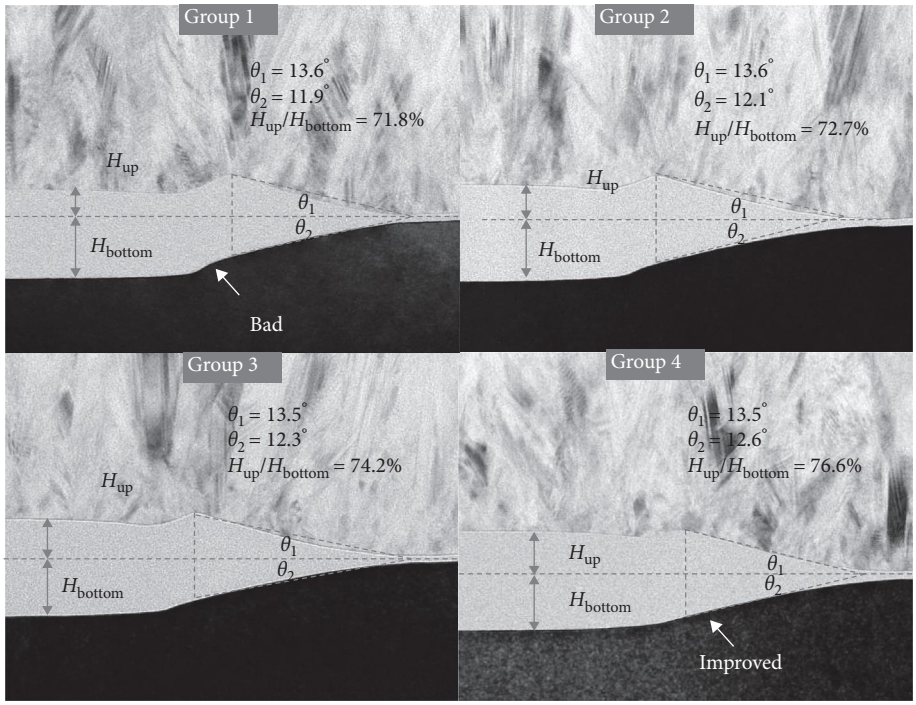
(4) Group 4 is the final optimized group. Bias power is reduced by about 4.2%, and etching time is reduced ~by about 12% at the same time. As a result, there is no silicon loss, and ~100 A oxide remains post-dry etching. It is worth mentioning that an additional wet process with HF is required in this group.

3.2. Physical Results. Taking the silicon substrate boundary as the reference plane, as described in Figure 7(a), the upper angle of the field plate is defined as θ_1, and the angle of the bottom surface is defined as θ_2. The thickness of the upper field plate and bottom field plate are defined as H_{up} and H_{bottom}, respectively. The oxide thickness ratio H_{up}/H_{bottom} and the bottom surface θ_2 are calculated as the factors for field plate bottom profile characterizations. Obviously, a higher ratio of H_{up}/H_{bottom} and higher angle θ_1 stands for a smoother bottom surface profile.

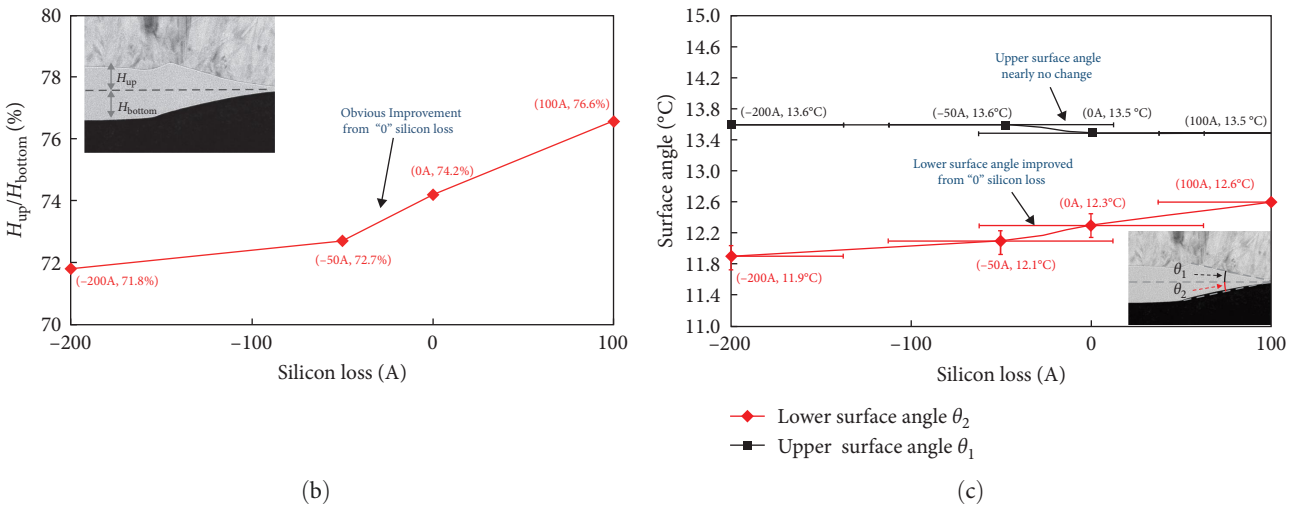
Figure 7(a) illustrates the physical results from four DOE groups; it can be seen Group 4 owns the best field plate structure. Compared with the baseline result of Group 1, the angle of the bottom surface θ_2 is improved from 11.9° to 12.6°, while the angle of the upper surface θ_1 nearly no change. Meanwhile, the oxide thickness ratio H_{up}/H_{bottom} increases from 71.8% to 76.6%. An "abrupt free" field plate has been produced successfully.

Table 1: Experiments design for field plate profile optimization.

Silicon loss	Group 1 ~200 A	Group 2 ~50 A	Group 3 ~0 A	Group 4 ~−100 A (oxide remains)
Bias power	Baseline	−4.2%	Baseline	−4.2%
Etching time	Baseline	Baseline	−12%	−12%
Extra HF	–	–	~15 A	~150 A
TEM cut (Figure 6)	√	√	√	√
TEM cut (Figure 7)	√	○	○	√



(a)



(b) (c)

Figure 7: Effects analysis of the field plate profile: (a) TEM result of mini-LOCOS field plate profile; (b) effects of silicon loss on field plate lower profile through H_{up}/H_{bottom}; (c) effects of silicon loss on field plate lower profile through θ_1 and θ_2.

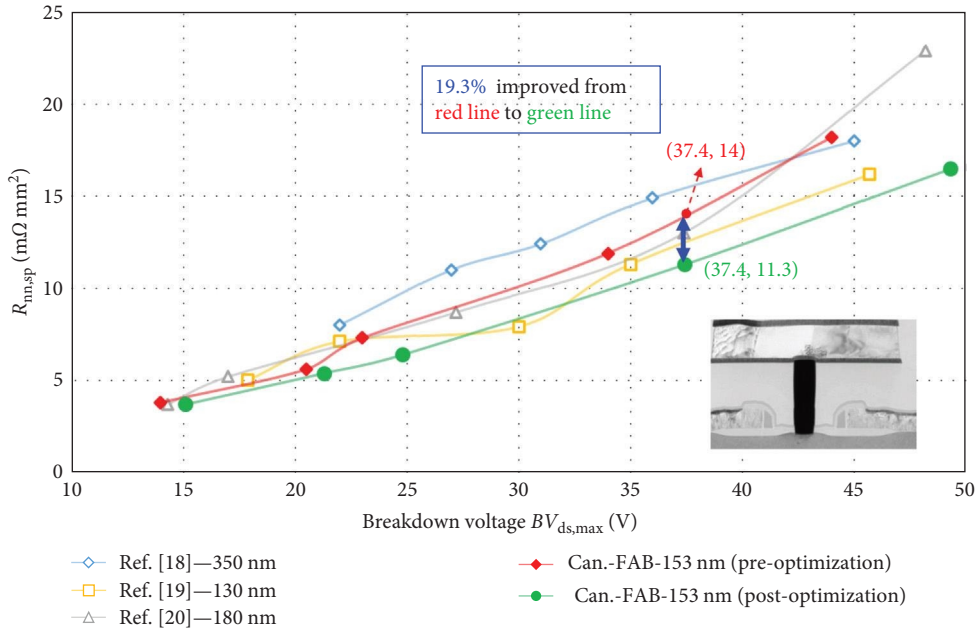


Figure 8: FOM curve from LDMOS with mini-LOCOS field plate.

Table 2: Electrical parameter for 130–350 nm LDMOS devices with mini-LOCOS field plate.

Ref. [18]—350 nm "abrupt" (suspicion)		Ref. [19]—130 nm "abrupt"(suspicion)		Ref. [20]—180 nm "abrupt" (suspicion)		Can.-FAB -153 nm "abrupt" (TEM)		Can.-FAB -153 nm "smooth"(TEM)	
$R_{on,sp}$ mΩ · mm^2	$BV_{ds,max}$ V	$R_{on,sp}$ mΩ · mm^2	$BV_{ds,max}$ V	$R_{on,sp}$ mΩ · mm^2	$BV_{ds,max}$ V	$R_{on,sp}$ mΩ · mm^2	$BV_{ds,max}$ V	$R_{on,sp}$ mΩ · mm^2	$BV_{ds,max}$ V
8	22	5	17.9	3.7	14.3	3.8	14	3.7	15.1
11	27	7.1	22	5.2	17	5.1	20.5	5.4	21.3
12.4	31	7.9	30	8.7	27.2	7.3	23	6.9	24.8
14.9	36	11.3	35	13	37.4	11.9	34	11.3	37.4
18	45	16.2	45.7	22.9	48.2	18.2	44	16.5	49.3

Figures 7(b) and 7(c) illustrate the silicon loss effects on H_{up}/H_{bottom} and θ_1: from the "0" silicon loss point, both H_{up}/H_{bottom} and θ_1 begin to increase obviously. The possible reason is that "0" silicon loss means no plasma damage on the silicon surface, and then the diffusion of H_2 and O_2 to the silicon surface under Si_3N_4 film becomes easier and smoother. Thus, "0" silicon loss is a fundamental requirement for the "abrupt free" field plate profile.

3.3. Electrical Results. Wafer-level electrical data is collected with Agilent B1500 tools. For comparison, five different devices are measured, including [18] FAB-350 nm, [19] FAB-130 nm, [20] FAB-180 nm, and Can.-FAB-153 nm fabricated with process conditions from Group 1 and Group 4, respectively.

Figure 8 illustrates the FOM curves of N-type LDMOS, and the data are listed in Table 2. It can be seen that the process-optimized devices achieve much better electrical performance, even better than that of 130 nm devices [18]. Take the same production line (red line and green line); the specific on-resistance $R_{on,sp}$ can be improved by about 19.3% (at the same breakdown voltage of 37.4 V). With no doubt, the field plate bottom physical optimization contributes to the electrical enhancement.

Furthermore, Figure 9 illustrates the SOA results of a typical 24 V device. The SOA curves are measured under a transmission line pulse (TLP) environment, and the test condition is that the pulse width of the TLP V_{ds} is 100 ns with an external capacitance $C_{gs} = 10$ nF. The drain current I_{ds} are measured under a variable V_{gs} from 0 V to 1.1 × V_{dd}.

From the comparison with Kim et al. [6], it can be seen that our device owns a better (or called larger) SOA region, which is also an indication of the robustness of the optimized process condition.

4. Conclusions and Discussion

Though mini-LOCOS LDMOS is popular, researches on this type of device is still on track, and optimization works on the inherent defect, "abrupt" bottom field plate surface, is with great significance. The impact of the field plate physical profile on LDMOS electrical performance, especially for $BV_{ds,max}$, is theoretically analyzed and simulated in this paper. An

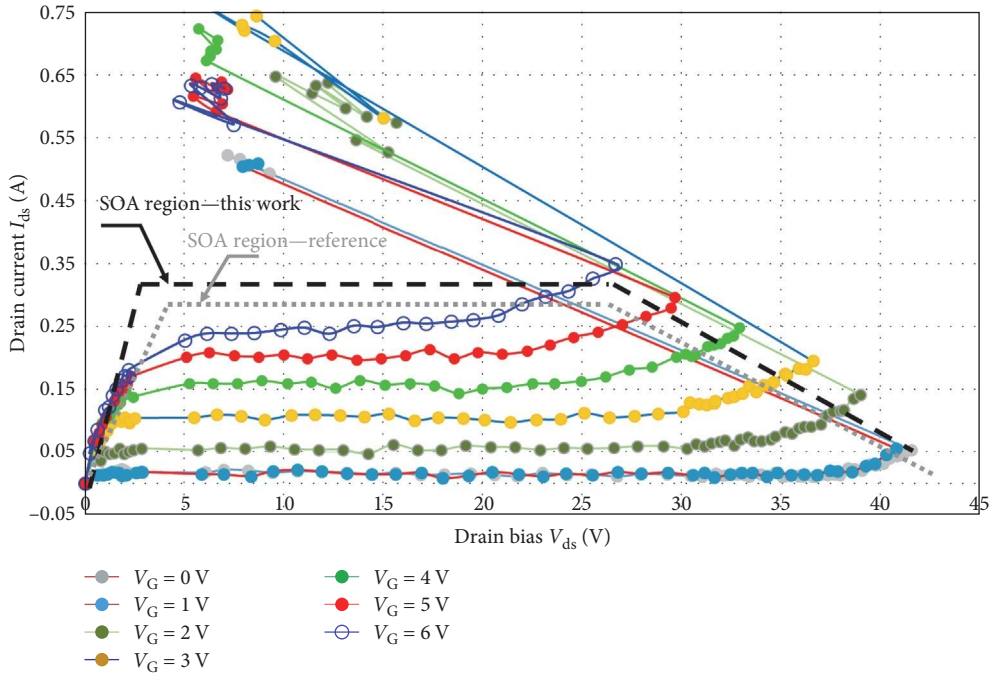


FIGURE 9: SOA of 24 V LDMOS with optimized min-LOCOS field plate.

effective optimization process by etching bias power and time reduction is proposed, and it is proved by TEM cut samples through the analysis of thickness ratio H_{up}/H_{bottom} and bottom surface angle θ_2. Finally, the optimization condition has been implemented in our real BCD circuit production line, series of LDMOS are measured, and $R_{on,sp}$ of typical 24 V N-type device achieves as low as 11.3 $m\Omega\,mm^2$ while $BV_{ds,max}$ arrives at 37.4 V. From the FOM curves analysis, specific on-resistance $R_{on,sp}$ performance is improved around 19.3%. From the I–V curves measurement under the TLP environment, a larger SOA window is acquired as well.

Beyond this work, there are still other studies that need to be carried out for future production improvement, including how to eliminate the "convex" upper profile on the field plate and how to integrate the mini-LOCOS field plate with the mini-STI field plate together. These works call for great industry line efforts, but they can bring us promising industry easily.

Data Availability

The data that support the findings of this study are available from the first author upon reasonable request (E-mail: 202111090937@mail.scut.edu.cn).

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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