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Research Article

An Approach to Increase Power-Added Efficiency in a 5 GHz Class E Power Amplifier in 0.18 μm CMOS Technology

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A new approach to increasing the power-added efficiency (PAE) of a class E power amplifier (PA) is proposed in this paper. The PA operates at a 5 GHz frequency and a reactance compensation technique is utilized to maximize the bandwidth at the operating frequency. The driver stage creates either a half-wave rectified sine wave or a half-wave rectified sawtooth wave. By applying each one of the waves, the performance of the PA is examined and PAE = 70% and PAE = 50% is achieved. Plus, the output power of the PA is about 26 dBm when the DC voltage supply is 1.8 V. Advanced design system and TSMC 0.18 μm CMOS process are utilized to carry on the simulation.

1. Introduction

Generally, a transceiver system is comprised of low-noise amplifiers, image reject filters, surface acoustic wave filters, voltage control oscillators, low-pass filters, band-pass filters, duplexers, and power amplifiers (PAs). Nevertheless, different transceivers might have more or less blocks in their systems. One of the major components of every radio frequency communication system is its PA. The block has to fulfill the required criteria such as low power consumption, low cost, appropriate integration, linearity, high output power, and high power-added efficiency (PAE). Owing to CMOS technology, PAs can be implemented with low cost and suitable integration. Plus, other criteria are to be achieved by the topology used for the PA, the class of the PA, the linearization technique, biasing, appropriate design and calculation of the matching network, and the CMOS size.

The performance of a PA fundamentally alters according to the class of the PA. In fact, PAs are categorized into different classes, including class A, B, AB, C, D, E, and F. The CMOS transistor in a PA might be considered as either a switch or a current source. Class A, B, AB, and C have their transistor as a current source, and other classes have their CMOS transistor as a switch. In addition, class A, B, and AB are linear and class C, D, E, and F are nonlinear [1]. Each class has its own merits and demerits. For instance, class A has a higher gain and linearity in comparison with class AB with higher PAE and higher output power [2, 3]. Furthermore, because of being ON just for half of the period of the input signal, class B dissipates less power, thus obtaining better PAE [2, 3]. On one hand, Class C does not have an appropriate performance for noise effects. On the other hand, it has suitable efficiency [4]. When it comes to having the best theoretical efficiency, class E has better results than class D and class F [5, 6].

Two different and crucial problems, oxide breakdown and hot electron effect, have brought about less reliability. To rectify the problem, cascode configuration has been utilized in order to enhance reliability and isolate the output from input, resulting in more stability [7–11]. Self-biased technique and capacitive crosscoupling technique have been utilized so as to decline power consumption, reduce the area of implementation, and improve reverse isolation [12, 13]. Common mode noise, time delay, and inductor loss have been solved by using differential cascode topology and capacitive crosscoupling neutralization technique [14–19]. Ultimately, the output power can be considerably increased by utilizing the power combining technique [20, 21].

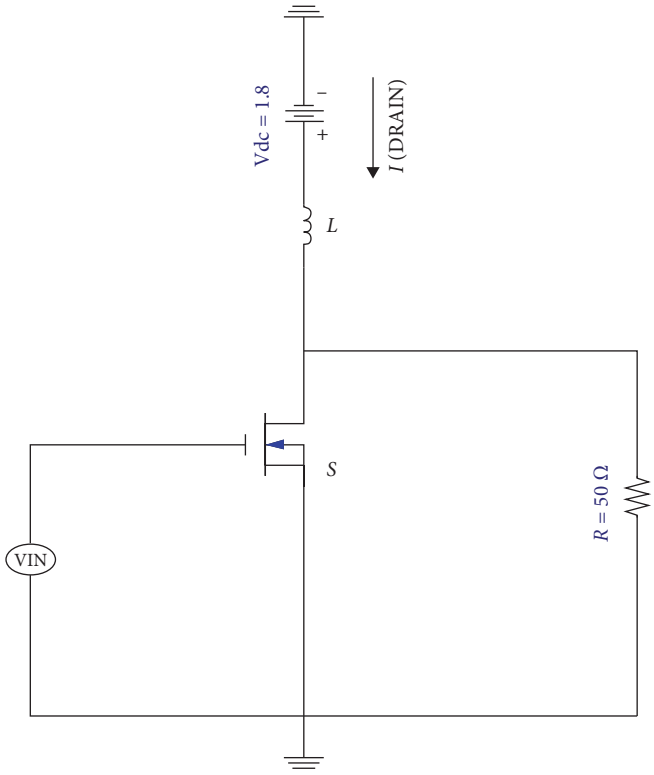

FIGURE 1: The circuit triggered by five different waves.

2. Appropriate Wave for Power Dissipation Reduction

PAE of PAs is calculated by:

$$\text{PAE} = \frac{P_{\text{OUT}} - P_{\text{in}}}{P_{\text{Vdc}}}. \quad (1)$$

In order to increase PAE, the power consumed by the DC voltage supply (P_{Vdc}) should be reduced. One of the most important advantages of a class E PA is that the efficiency of the circuit is considerably higher because the CMOS transistor, the switch, is ON just during half of the period. In other words, the Vdc consumes less power because the current crossing through the drain of the CMOS is very low during half of the period. Hence, if the time during which the CMOS is ON is brought down, the power consumption of the voltage supply is diminished. In order to evaluate the experience, the circuit demonstrated in Figure 1 is simulated so as to measure the power consumed by Vdc and input power when the circuit is triggered by five different waves, depicted in Figure 2. The power is calculated from:

$$P_{\text{Vdc}} = \left[\frac{1}{a2 - a1}\int_{a1}^{a2} I(\text{DRAIN})dt\right] \times \text{Vdc}. \quad (2)$$

The threshold voltage of the CMOS is 0.511 volts and the values of other elements and the performance of the circuit are shown in Tables 1 and 2. Plus, CMOS is biased to operate in weak inversion.

Traditionally, a class E PA is triggered by a pulse generated by a driver circuit. The pulse makes CMOS turn on during half of the period of the pulse. Nevertheless, in comparison with other waves, the pulse has the worst Vdc power dissipation according to Table 2. Notwithstanding, half-wave rectified sine wave, half-wave rectified sawtooth wave, and sawtooth wave have the best performance. The reason is that unlike, the pulse wave, other waves make CMOS turn on less than half of the period of the wave. Therefore, the current passing through the drain of the CMOS is very low more than half of the period, thus bringing down the power consumed by Vdc. Consequently, it can be deduced that the power consumption of Vdc can be reduced provided that the PA is triggered by half-wave rectified sine wave or sawtooth wave instead of a pulse. As a result, if the power consumption of Vdc is reduced, PAE will be increased. For that reason, the driver circuit should generate either half-wave rectified sine wave or sawtooth wave.

3. The Proposed PA

The proposed PA, illustrated in Figure 3, is comprised of two main parts, including the driver stage and the main PA. According to what mentioned in the previous section, the least power consumption of the Vdc occurs when the input wave is either half-wave rectified sine wave or half-wave rectified sawtooth wave. Hence, the major objective of using the driver stage is to generate the appropriate wave. By utilizing $C1$, $L1$, $L2$, $L3$, and $M1$, the suitable wave can be created so as to trigger the main PA. The main intention of using traditional drivers is that the transistor and two tanks, resonating at the first and the third harmonic, are supposed to generate pulse wave. Unlike the traditional driver stage, the proposed stage eliminates both parts. Consequently, the implementation will be more straightforward and the power dissipation in the tanks will be eliminated, thus reducing the power consumption of the PA. Another advantage is that each wave can be created just by adapting the width of $M1$, demonstrated in Table 3.

4. Results and Discussion

The created waves are demonstrated in Figure 4. In fact, the waves are generated to be applied to the gate of $M2$, $VG2$, for triggering the main PA.

The main PA consists of $C0$, $L0$, $L4$, $M2$, and output matching. In fact, $C0$ and $L0$ are calculated to resonate at the main frequency (5 GHz). The output matching network is designed to create the optimal impedance at the drain of $M2$. Triggered by each wave, $M2$ generates the drain voltage and current depicted in Figure 5.

Both voltages and currents are appropriate for a PA because in both circumstances, whenever the current of the drain is maximum the drain voltage is minimum and vice versa. Therefore, the power consumed by Vdc and $M2$ is reduced.

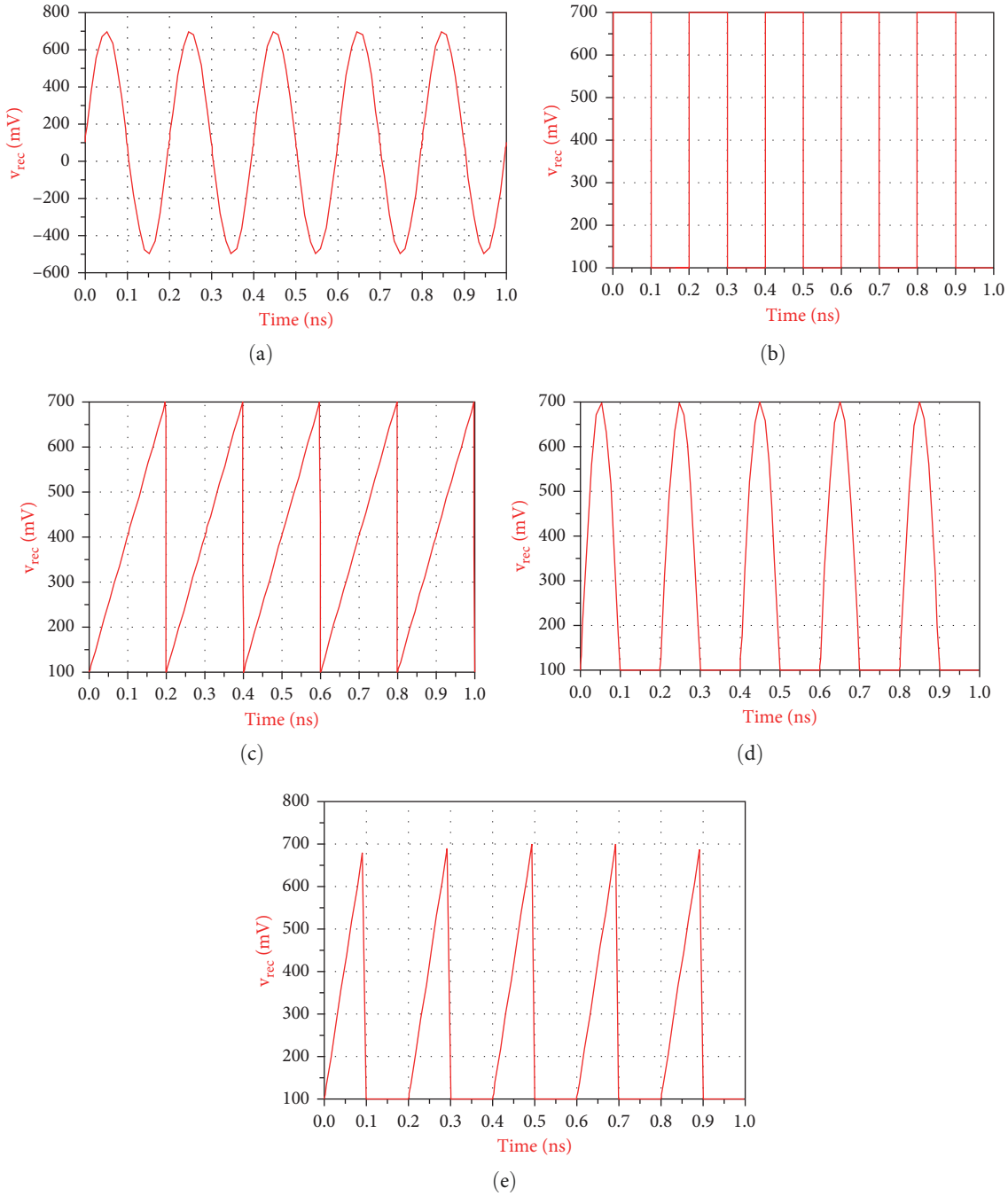

FIGURE 2: (a) Sine wave, (b) pulse wave, (c) sawtooth wave, (d) half-wave rectified sine wave, and (e) half-wave rectified sawtooth wave.

TABLE 1: The values of the elements in Figure 1.

$M = 50$	$W = 100\,\mu$m	$L = 2.8$ nH	Frequency of input voltage = 5 GHz	Amplitude of input voltage = 0.6 V

The reactance compensation technique is a method by which the alteration of the real part and the imaginary part of the input impedance of the output circuit is minimized. Consequently, the output power around the operating frequency has the least fluctuation.

The concept of the reactance compensation technique can be realized from Figure 6. The real and imaginary part of the input impedance of the output network is approximately constant around the operating frequency (5 GHz), demonstrated in Figure 6(a). As a result, the alteration of

Table 2: Performance of the circuit in Figure 1.

	Vdc power dissipation (W)	Input power (W)
Half-wave rectified sine wave	0.159	0.016
Half-wave rectified sawtooth wave	0.11	0.011
Sawtooth wave	0.145	0.132
Pulse wave	0.3	1.118
Sine wave	0.161	0.022

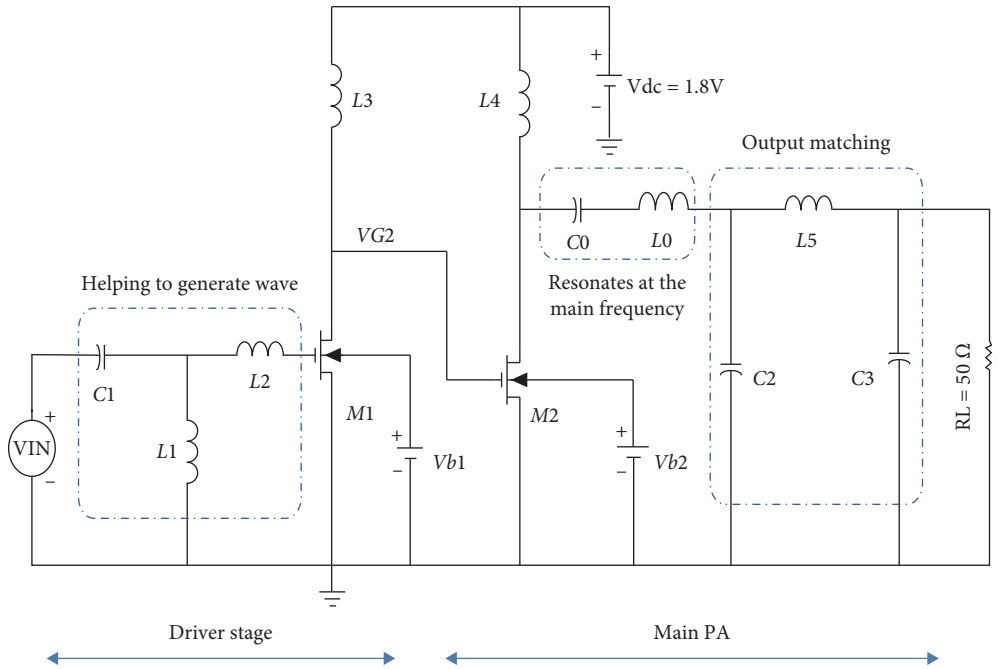

Figure 3: The proposed PA.

Table 3: Elements' values to create each wave.

Half-wave rectified sine wave	$M1$: $W = 5\,\mu$m, $M = 7$	$C1 = 10$ pF	$L1 = 0.1$ nH	$L2 = 2.5$ nH	$L3 = 0.441$ nH
Half-wave rectified sawtooth wave	$M1$: $W = 100\,\mu$m, $M = 7$	$C1 = 10$ pF	$L1 = 0.1$ nH	$L2 = 2.5$ nH	$L3 = 0.441$ nH

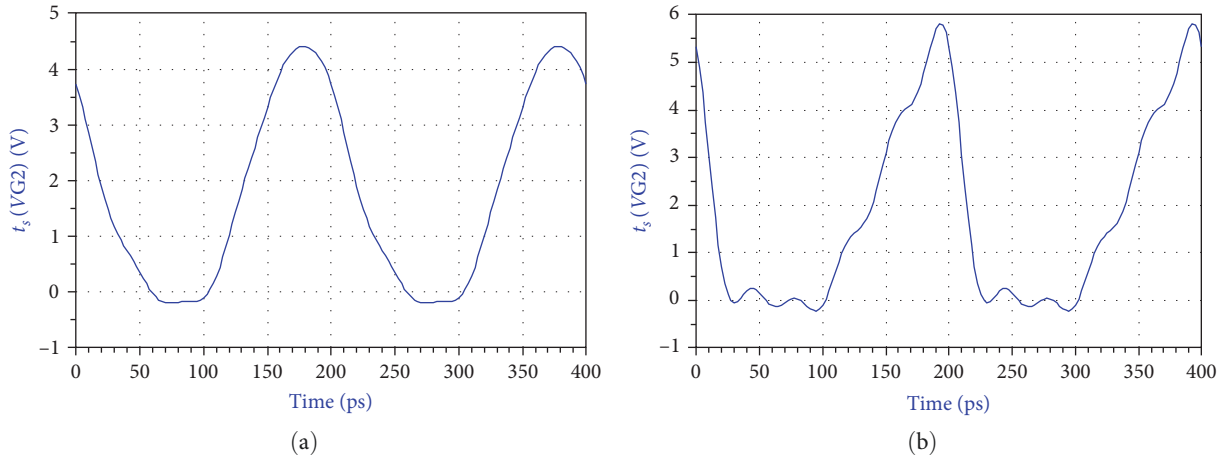

Figure 4: The output of the driver stage ($VG2$). (a) Half-wave rectified sine wave and (b) half-wave rectified sawtooth wave.

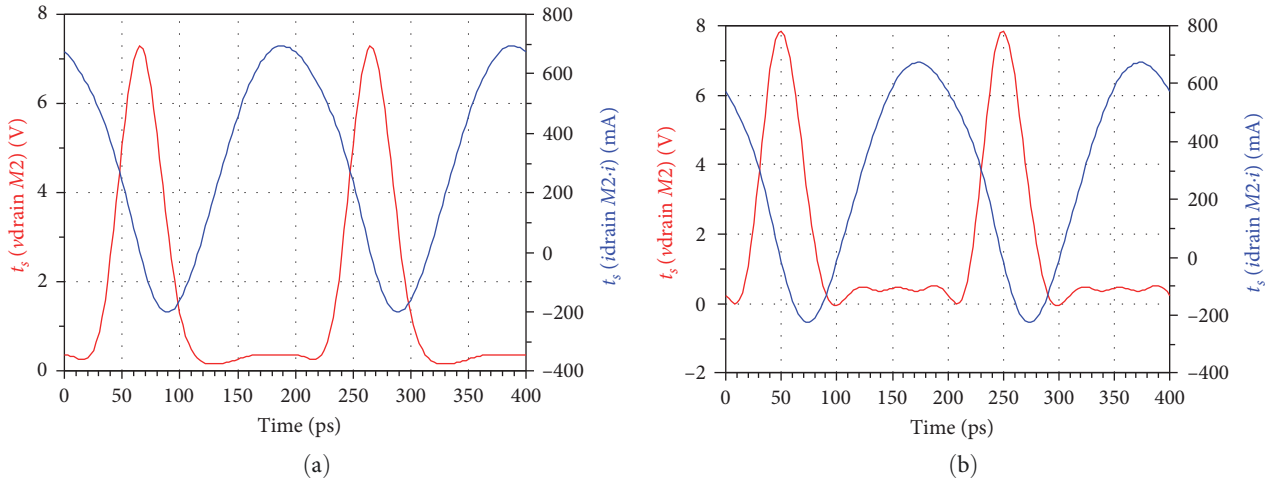

FIGURE 5: The drain voltage and current of $M2$. (a) By applying half-wave rectified sine wave in Figure 4 and (b) by applying half-wave rectified sawtooth wave in Figure 4.

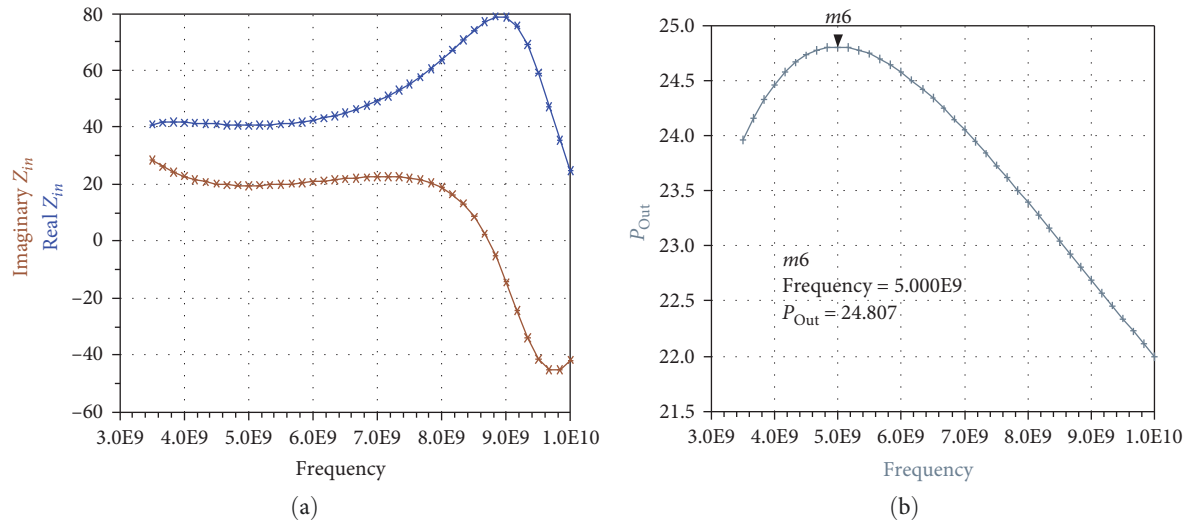

FIGURE 6: The reactance compensation technique. (a) The real and imaginary part of the impedance and (b) the output power after using the technique.

the output power is about zero around the frequency, depicted in Figure 6(b).

The final part of the PA is the output circuit, shown in Figure 7. In order to calculate the elements' values existing in the output circuit, the admittance of the circuit is calculated by:

$$Y_{in} = \frac{1}{Ron} + \frac{1}{j\omega L4} + j\,\omega\,Cds + \frac{1}{Z1 + P1}. \tag{3}$$

In which:

$$Z1 = \frac{1 - L0C0\omega^2}{C0\omega j} \text{ when: } L0 = \frac{1}{\omega^2 C0} \text{ then: } Z1 = 0, \tag{4}$$

$$P1 = \frac{-L5\omega + (RL - C3L5RL\omega^2)j}{C2C3L5RL\omega^3 - (C2RL + C3RL)\omega + (1 - C2L5\omega^2)j}, \tag{5}$$

$$Y_{in} = \frac{1}{Ron} + \frac{1}{j\omega L4} + j\,\omega\,Cds + \frac{C2C3L5RL\omega^3 - (C2RL + C3RL)\omega + (1 - C2L5\omega^2)j}{-L5\omega + (RL - C3L5RL\omega^2)j}, \tag{6}$$

Cds does not exist in the output circuit and it is considered as the capacitor seen from the drain of $M2$.

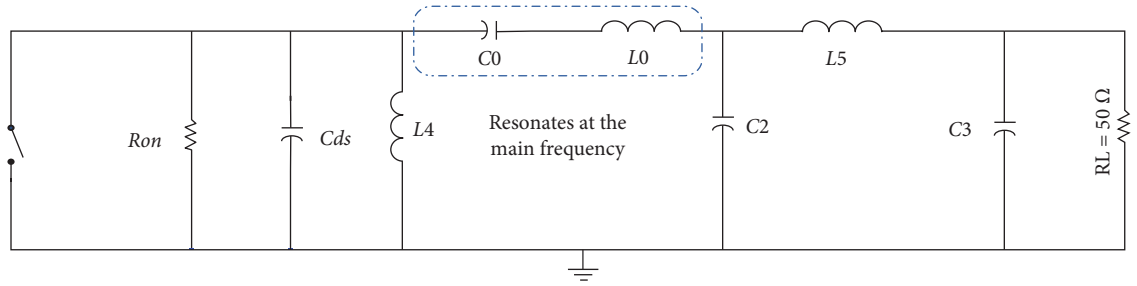

FIGURE 7: The output circuit.

TABLE 4: Elements' values for the main PA.

L4 (H)	C0 (F)	L0 (H)	C2 (F)	L5 (H)	C3 (F)
1.8e-9	1e-12	1.0132e-9	3.1e-11	0.1e-9	1.42e-11

The imaginary part of the admittance is calculated by:

$$\mathrm{im}(Y_{in}) = \frac{-1}{\omega L4} + \omega\, Cds + \frac{C2C3^2L5^2RL^2\omega^5 + (C2L5^2 - C3^2L5RL^2 - 2C2C3L5RL^2)\omega^3 + (C3RL^2 - L5 + C2RL^2)\omega}{C3^2L5^2RL^2\omega^4 + (L5^2 - 2C3L5RL^2)\omega^2 + RL^2}. \tag{7}$$

The first and the second derivatives of the imaginary part should be zero to maximize the bandwidth at the operating frequency [22].

$$\frac{d(\mathrm{im}Y_{in}(\omega))}{d\omega} = \frac{1}{L4\omega^2} + Cds + T1. \tag{8}$$

In which:

$$\begin{aligned} T1 &= \frac{\mathrm{num1}}{\mathrm{den1}} \\ \mathrm{num1} &= (C2C3^4L5^4RL^4)\omega^8 + (C3^4L5^3RL^4 - 4C2C3^3L5^3RL^4 + 2C2C3^2L5^4RL^2)\omega^6 \\ &\quad + (2C3^2L5^3RL^2 - C3^3L5^2RL^4 + 6C2C3^2L5^2RL^4 - 4C2C3L5^3RL^2 + C2L5^4)\omega^4 \\ &\quad + (2C2L5^2RL^2 - C3^2L5RL^4 - 3C3L5^2RL^2 - 4C2C3L5RL^4 + L5^3)\omega^2 + (C3RL^4 - L5RL^2 + C2RL^4) \\ \mathrm{den1} &= (C3^2L5^2RL^2\omega^4 + (L5^2 - 2C3L5RL^2)\omega^2 + RL^2)^2, \end{aligned} \tag{9}$$

$$\frac{d^2(\mathrm{im}Y_{in}(\omega))}{d\omega^2} = \frac{-2}{(L4\omega^3)} + T2. \tag{10}$$

In which:

$$\begin{aligned} T2 &= \frac{\mathrm{num2}}{\mathrm{den2}} \\ \mathrm{num2} &= (-2C3^6L5^5RL^6)\omega^9 - (6C3^4L5^5RL^4)\omega^7 + (12C3^4L5^3RL^6 - 6C3^2L5^5RL^2 + 18C3^3L5^4RL^4)\omega^5 \\ &\quad + (6C3^2L5^3RL^4 - 16C3^3L5^2RL^6 + 10C3L5^4RL^2 - 2L5^5)\omega^3 + (6C3^2L5RL^6 - 18C3L5^2RL^4 + 6L5^3RL^2)\omega \\ \mathrm{den2} &= (C3^2L5^2RL^2\omega^4 + (L5^2 - 2C3L5RL^2)\omega^2 + RL^2)^3. \end{aligned} \tag{11}$$

By using the formulas, all the calculated values are mentioned in Table 4.

The output voltage, the output power, and the PAE of the PA are shown in Figures 8–10, respectively. Because the amplitudes of the output voltage in both circumstances are approximately the same, the output power is nearly the same and about 26 dBm. It is anticipated that the PAE of the PA is considerably enhanced because of the current and voltage of $M2$ and appropriate waves created by the driver stage.

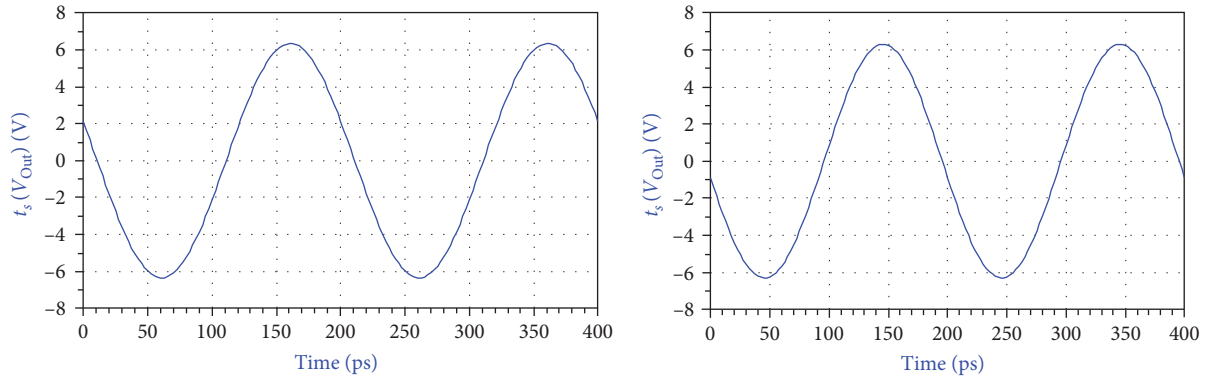

FIGURE 8: Output voltage of the PA. (a) By applying half-wave rectified sine wave in Figure 4 and (b) by applying half-wave rectified sawtooth wave in Figure 4.

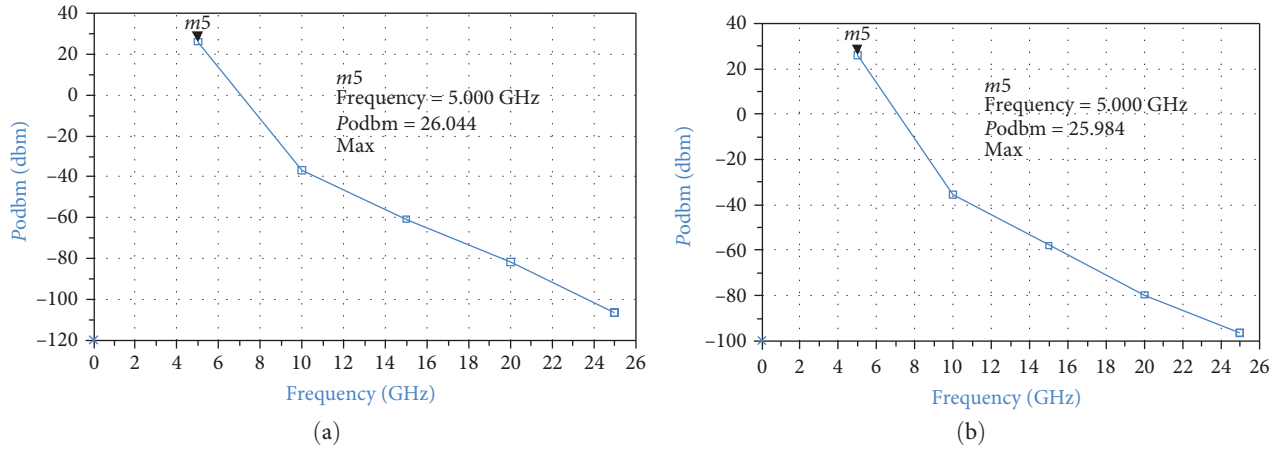

FIGURE 9: Output power of the PA. (a) By applying half-wave rectified sine wave in Figure 4 and (b) by applying half-wave rectified sawtooth wave in Figure 4.

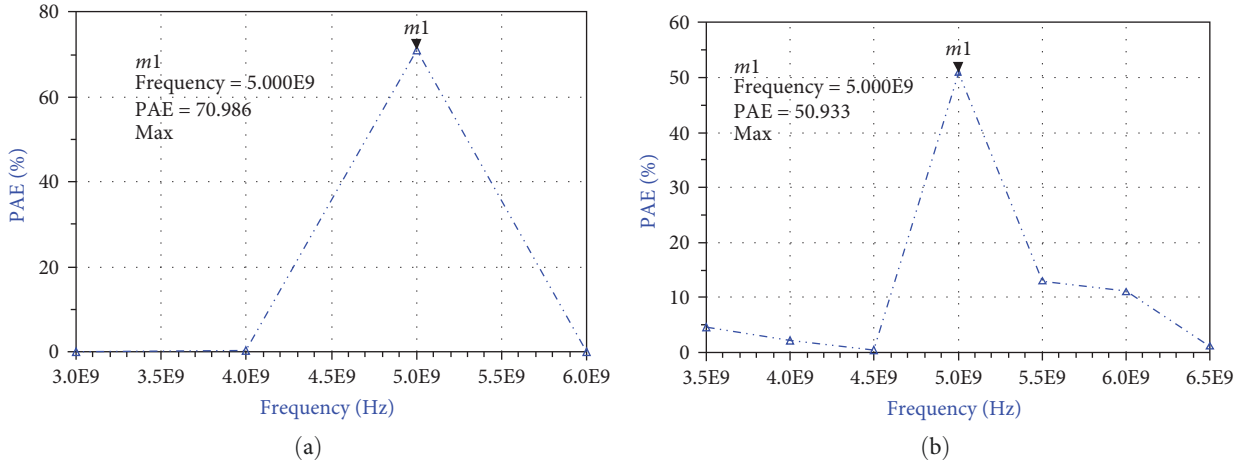

FIGURE 10: PAE of the PA measured at the main frequency (5 GHz). (a) By applying half-wave rectified sine wave in Figure 4 and (b) by applying half-wave rectified sawtooth wave in Figure 4.

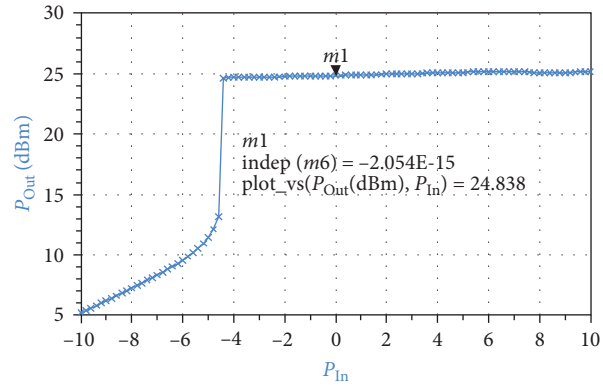

Figure 11: Output power versus input power.

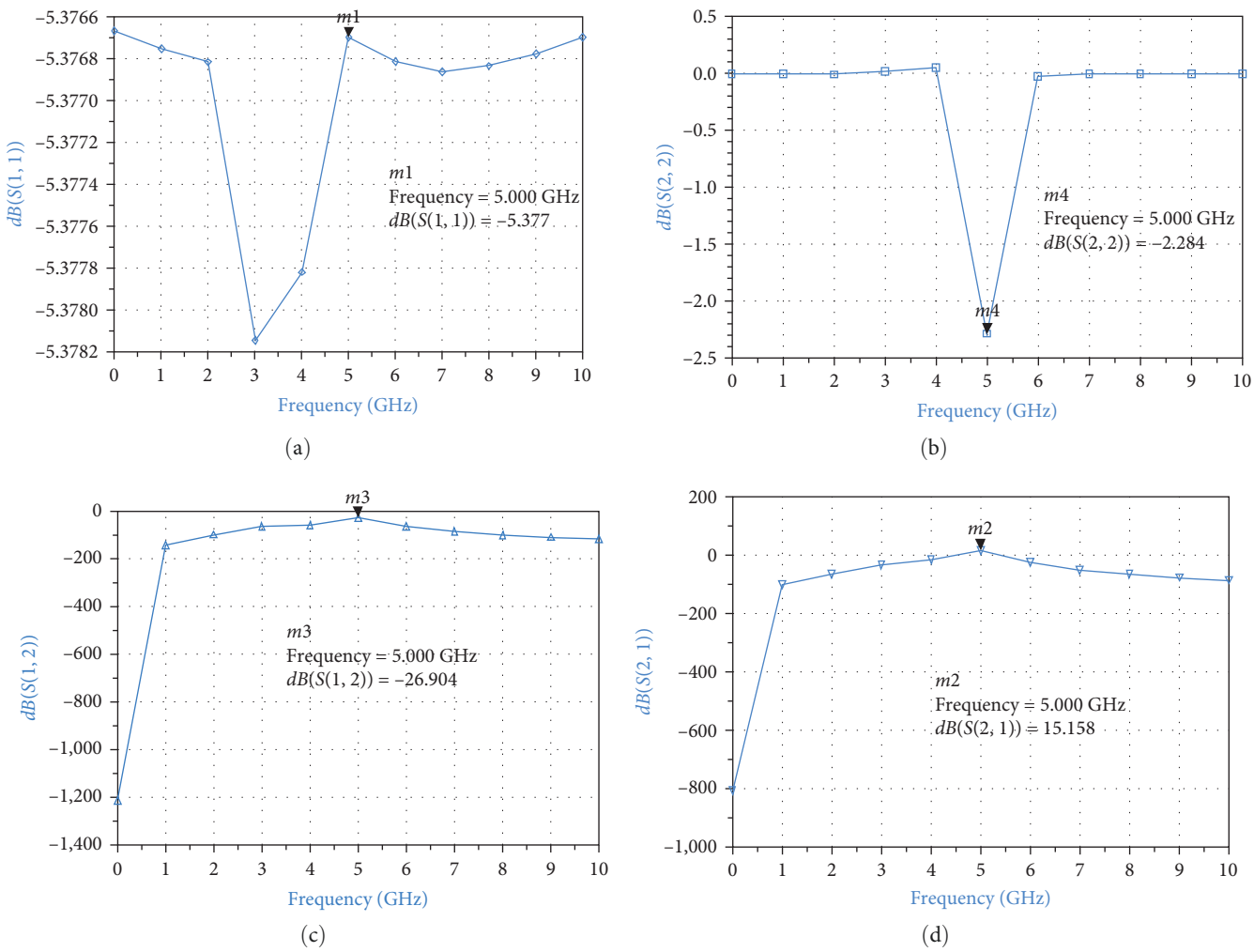

Figure 12: Scattering parameters of the PA. (a) $S11$, (b) $S22$, (c) $S12$, and (d) $S21$.

The PAE of the circuit is appropriate in both situations shown in Figure 10. In fact, the performance of the PA is better when the trigger wave is half-wave rectified sine wave, with PAE = 70.986%. Notwithstanding, the PAE of the PA is acceptable when the PA is triggered by half-wave rectified sawtooth wave with PAE = 50.933%.

The behavior of the output power versus the input power is shown in Figure 11. In addition, the extracted scattering parameters of the PA are demonstrated in Figure 12. The scattering parameters can guarantee that the circuit is stable at the operating frequency.

The performance of the PA is compared with other works in Table 5. The PA is designed to operate at 5 GHz frequency in 0.18 μm CMOS technology. The PAE of the PA is considerably enhanced in comparison with other works, which is the main purpose. The output power in some works

Table 5: Performance summary and comparison with other state-of-the-art.

Reference	CMOS technology (μm)	Frequency (GHz)	Supply voltage (V)	Classes	PAE (%)	Output power (dBm)
This work (half-wave rectified sine)	0.18	5	1.8	E	70	26
This work (half-wave rectified sawtooth)	0.18	5	1.8	E	50	25.9
[1]	0.18	2.4	2.5	AB	31	26.8
[2]	0.18	2.4	2.4	F	34.6	27.6
[5]	0.18	2.4	1.8	D	50	15
[7]	0.18	2.4	2.4	–	49	24.5
[9]	0.18	2.4	1.6	E	35	18
[10]	0.13	2.4	2	E	57	19
[11]	0.13	2.4	2.5	–	44.7	20
[13]	0.18	2.4	3.3	A	34.3	25.2
[23]	0.18	2.4	3.3	E	44.5	23
[24]	0.18	2.4	3.3	E	40	21.3
[15]	0.35	2.4	1	E	33	18
[16]	0.18	2.4	3.3	–	34.9	23.3
[20]	0.18	2.4	3.3	AB	27	31
[25]	0.18	2.4	3.3	AB	29	30.7
[26]	0.13	2.4	2.5	AB	40	30
[27]	0.065	2.4	3.3	–	40.3	26.9
[28]	0.18	2.4	3.3	–	23.5	21.28
[29]	0.13	2.4	1	E	69	18.58

is better than this work with sacrificing for utilizing higher Vdc. In other words, the better output power has been gained only with Vdc higher than 1.8 V. In fact, PAE, lifetime of the circuit, and the power consumption of the circuit will be reduced by using higher Vdc. Plus, the proposed PA operates at a higher frequency, 5 GHz. The reason why the PAE is improved can be attributed to the waveforms utilized. In fact, both waveforms are zero more than half of the period. Unlike pulse, both waves do not turn on the CMOS immediately and they gradually turn on the switch. Therefore, the CMOS is off more than half of the period. Consequently, the power dissipated via CMOS and the Vdc is reduced considerably. By decreasing the power consumed by Vdc, the PAE is increased noticeably.

5. Conclusions

In this paper, a class E PA is proposed with the intention of improving the PAE of the PA. A new technique is proposed to achieve the main objective by utilizing different waves to trigger the main PA. Owing to using the proposed driver stage, the implementation of the PA and the power consumption of the Vdc are enhanced. The performance of the circuit is noticeable when the main PA is triggered by a half-wave rectified sine wave instead of a pulse. The reactance compensation technique is used to broaden the bandwidth at the main frequency. The PAE = 70% and PAE = 50% are obtained by applying half-wave rectified sine wave and half-wave rectified sawtooth wave, respectively. The output power in both circumstances is about 26 dBm. The experience demonstrates that by utilizing waves during which the CMOS is turned on less than half of the duty cycle of the input wave, the PAE of the PA can be reduced significantly. Because the DC voltage utilized in this paper is 1.8 V, the 0.18 μm CMOS technology with an appropriate model for CMOS in the voltage is used. By generating a appropriate waveform for the main PA, the voltage existing on the drain of the CMOS is minimum when the current passing through the drain of the transistor is maximum, thus making PAE bigger. Ultimately, the PA can be improved so as to operate for ultra-wideband purposes. Plus, by decreasing DC voltage in technologies like 0.13 or 0.09 μm, the PAE and the size of the PA might be improved.

Data Availability

In case of any requirements, all supporting data can be requested from the author "Hemad Heidari Jobaneh" via his email: emehhj@gmail.com.

Conflicts of Interest

The author declares that there is no conflicts of interest.

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