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Research Article

Design of Binary and Ternary Logic Inverters Based on Silicon Feedback FETs Using TCAD Simulator

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A feedback field effect transistor (FBFET) with p-n-p-n structure benefits from a positive feedback mechanism. In this structure, the accumulated charges in its potential well and limitation of carrier flow by its internal potential barrier lead to superior electrical properties such as lower subthreshold swing (SS) and higher I_{ON}/I_{OFF} ratio in comparison with FinFET. Thus, FBFET is a promising alternative for digital applications such as logic inverters. In this paper, binary and ternary logic inverters are designed by using FBFETs with 40 nm channel length. The doping profile in the device plays an essential role and specifies the binary or ternary operation of the inverter. The inverter is analyzed by using a TCAD mixed-mode simulator. The results indicate the high value of 10^{10} for I_{ON}/I_{OFF} ratio with an extremely low SS (1 mV/decade). The voltage transfer characteristics of the inverter and its dependence on doping levels have been investigated. Also, the electrical properties of this inverter are compared with previous inverter counterparts.

1. Introduction

Power consumption is the most significant challenge to continue MOSFET scaling because of physical limitations to scale subthreshold swing (SS) below 60 mV/decade at 300 K [1–3]. Even with FinFET [4–7] or double-gate MOSFETs, SS is larger than 60 mV/decade. To overcome this limit, many super steep switching devices have been proposed, such as negative capacitance field effect transistors (FETs) [8], nanoelectromechanical [9] switches with the mechanical operation of the channel, phase FET [10, 11], and tunnel FETs [12, 13]. Out of all these structures, feedback FET (FBFET) has attracted a lot of interest due to low operating voltage, super steep switching characteristics, and high I_{ON}/I_{OFF} ratio [14, 15]. FBFET takes advantage of the S-shaped energy band of channel region, and the feedback loop creates the reciprocal interaction between the potential barriers and charge carriers that allow extremely low SS (<1 mV/decade). It was observed that the ON current of FBFET devices is slightly less compared to conventional devices though it has a much better OFF current [14, 15]. Thus, FBFET is a low-power device and a superior candidate to replace the conventional MOSFET in logic circuits for low-power applications [16].

In the paper, the binary and ternary logic inverters are designed based on FBFET instead of conventional devices, and effective parameters on their voltage characteristics have been investigated. Ternary logic (three-valued logic) has attracted much attention due to its potential advantages over binary logic for designing digital systems [16, 17].

By ternary logic, more simplicity and energy efficiency can be achieved since the logic reduces the complexity of interconnects and chip areas. Indeed, the main advantage of ternary logic circuits is the high density of logic elements. In ternary logic, it only takes $n \times \log 32$ bits to represent an n-bit binary number. Also, ternary logic reduces 37% area of the microprocessor for the same function [16, 17].

Overall, in comparison with binary design, a ternary logic implementation requires fewer operations, fewer gates, and signal lines for the same functions. Therefore ternary logic is expected to improve the power, performance, and area characteristics. The simulation results indicate that both binary and ternary inverters can be implemented by using FBFETs. Also, it is found that the impurity level and profile have strong effects on FBFET current–voltage characteristics. The organization of the paper is as follows. After the

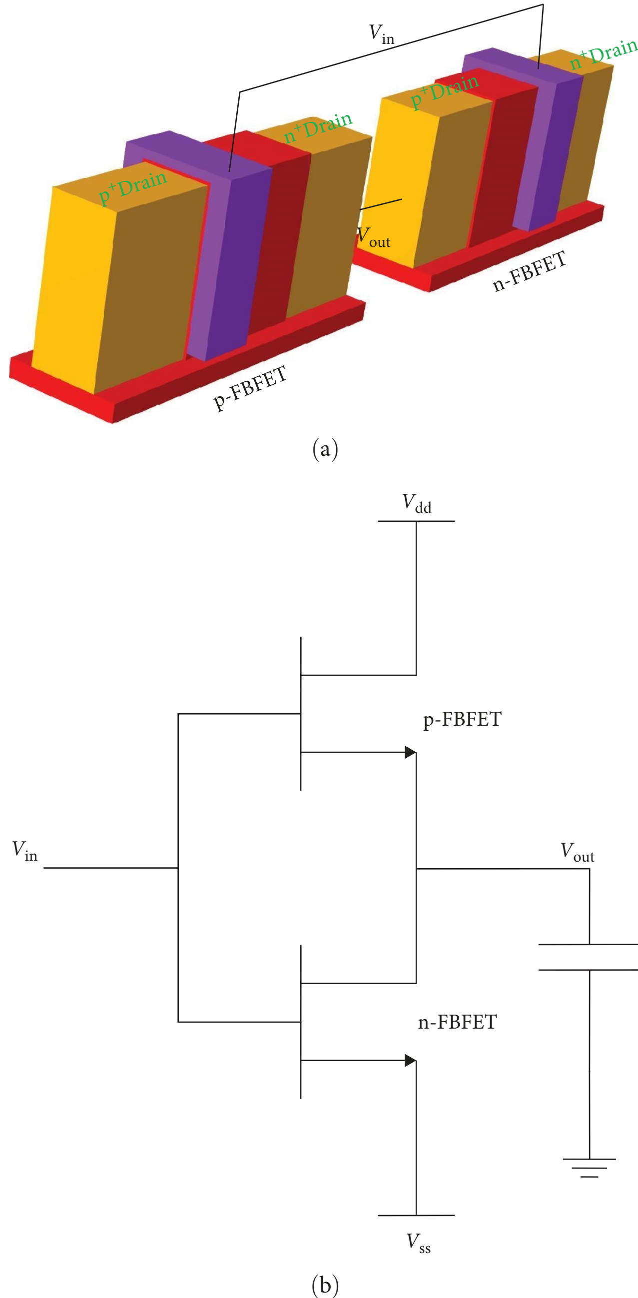


FIGURE 1: (a) The inverter device structure consists of n-FBFET and p-FBFET. The gate oxide is indicated by the red color. (b) The inverter circuit with series connection of p-FBFET and n-FBFET.

introduction section, the transistor structure and inverter circuit are presented in Section 2. Simulation results and the current–voltage characteristics are explained in Section 3. Finally, conclusions are discussed in Section 4.

2. Device Structure and Methods

Figure 1 shows the inverter circuit that uses the n-type and p-type FBFETs. The gate of n-FBFET and p-FBFET are connected to each other and also to the input voltage. The output voltage is measured from the point that the source of p-FBFET and drain of n-FBFET have been connected to each other. Each FBFET consists of four regions, i.e., drain, channel 1, channel 2, and source. The drain and channel 2 regions are p-type, but the source and channel 1 regions are n-type. While the gate oxide covers two sides of the channel regions, the metal gate just formed on one of the channel regions. The position of the gate on the channel specifies the p-type or n-type operation of the transistor. For n-FBFET, the metal gate is formed on channel 2, while for p-FBFET, the metal gate is formed on channel 1. Table 1 indicates the values for selected device design parameters. In the conventional inverter, the p-type metal oxide semiconductor source is connected to V_{DD}, and its drain is connected to the output voltage. But in the new structure, the drain of p-FBFET is connected to V_{DD} while the source contact is connected to the output voltage. Also, the only difference between n-FBFET and p-FBFET is the position of the gate, as it can be found in Figure 1, and is different from conventional FETs. Technology computer-aided design (TCAD) mixed mode simulator has been used to analyze the device performance. Shockley–Read–Hall (SRH) model is used to consider recombination and generation mechanisms in the semiconductor. In addition to the SRH model, the Auger model is used to consider the recombination events in heavily doped silicon devices [18]. Also, Fermi–Dirac calculation, field-dependent mobility model, bandgap narrowing model, and concentration-dependent mobility model are implemented in this simulation.

TABLE 1: Inverter device parameters.

Parameters	Value (unit)
Total length of channel	40 nm
Oxide thickness	0.7 nm
Length of metal	20 nm
Work function of metal	4 eV
Channel 1 doping density	$10^{20}/cm^3$
Channel 2 doping density	$10^{20}/cm^3$

3. Results

To explain the performance of the FBFET, in Figure 2 the energy band diagrams are shown in the OFF state ($V_{GS} = 0$ and $V_{DS} = 1.5V$), and in the ON state ($V_{GS} = 1.5V$ and $V_{DS} = 1.5V$). The S-shaped energy barrier in this device is formed by doping using p-n-p-n structures. Under equilibrium (Figure 2(a)), the electrons from the source to drain encounter a potential barrier at channel 2 (p-type) and a potential well at channel 1 (n-type). Similarly, holes encounter a potential barrier at channel 1, and a potential well at channel 2, preventing any flow of carrier between source and drain regions. By applying drain voltage, the energy level across the drain region decreases (Figure 2(b)). However, due to the potential barrier and the potential well, carriers still cannot flow into the channel. By applying positive gate voltage to n-FBFET or negative gate voltage to p-FBFET, the energy barrier collapsed suddenly. The green line in Figure 2(b) shows the sudden collapse of the energy barrier under $V_{GS} = 1.5V$.

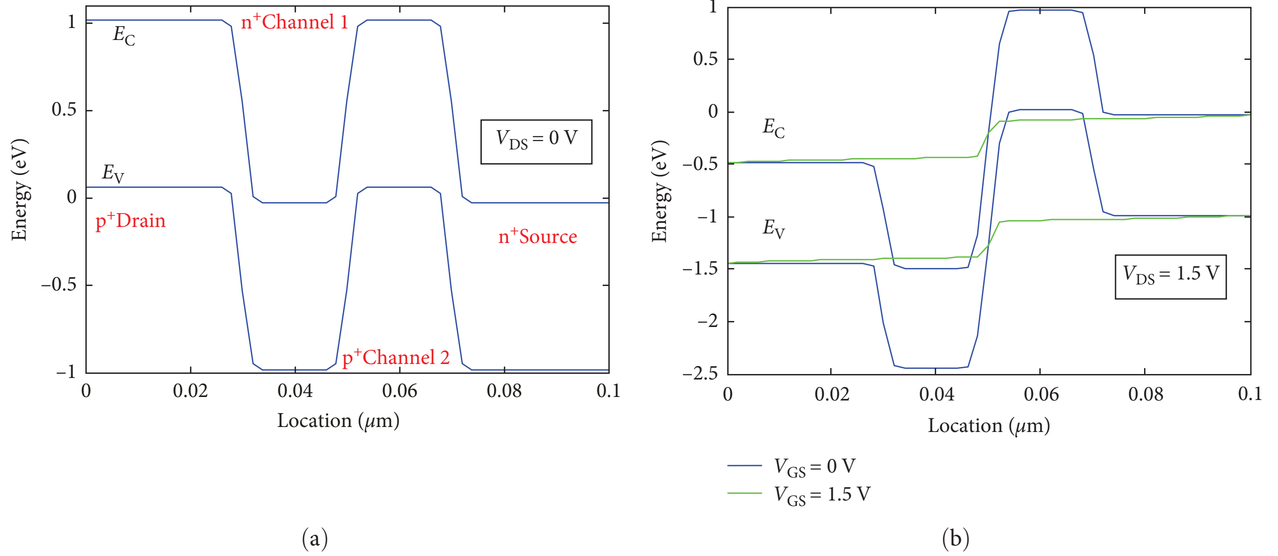


FIGURE 2: Conduction and valence band diagram of n-FBFET under (a) $V_{DS} = 0V$ and $V_{GS} = 0V$. In (b), the energy barrier is collapsed by positive gate voltage $V_{GS} = 1.5V$ at $V_{DS} = 1.5V$.

This collapse is due to a positive feedback mechanism [14, 15]. Indeed, by applying a positive gate voltage, the potential barrier at channel 2 decreases, and electrons from the source can drift toward the drain and accumulate in the well present at channel 1. This accumulation of electrons acts as a forward bias for the PN junction present at the drain end, reducing the barrier height for holes present at channel 1, and thus a few holes drift from the drain end to the source end and accumulate at channel 2. The accumulation of holes at channel 2 acts as a forward bias for the PN junction present at the source end. Thus there is a slight reduction of barrier at channel 1, which further enhances the flow of electrons from the source end to the drain and sets up a positive feedback loop in the device. At a particular gate bias, called the threshold voltage, the accumulated carriers are sufficient to remove the barrier completely, resulting in the steep switching ON of the device.

Figure 3 shows the current versus gate voltage in the case of $V_{DS} = 1V$. From the figure, the important characteristics such as I_{ON}/I_{OFF} ratio and SS are extracted. I_{ON}/I_{OFF} ratio represents the ratio of drain current at ON state ($V_{GS} = V_{OFF} + V_{DD}$ and $V_{DS} = |V_{DD}|$) to the current at the OFF state ($V_{GS} = V_{off}$ and $V_{DS} = |V_{DD}|$). V_{off} indicates the gate-source voltage (V_{GS}) at the OFF state. From the figure, the I_{ON}/I_{OFF} current ratio of 10^{10} can be observed. Also, we can find that the threshold voltage for n-FBFET is about +0.5 V, while the threshold voltage for p-FBFET is about −0.5 V.

The minimum value of the SS is one of the important parameters defined as follows [13]:

$$SS_{min} = \frac{dV_G}{d(\log(I_D))}. \quad (1)$$

In Figure 3, the sharp variation in the current curve versus gate voltage can be observed, and a very low SS (1 mV/decade) has been calculated from the figure. From the figure, it can be found that for both p-FBFET and n-FBFET, the positive current flows from the drain region to the source region. This is unlike conventional FETs.

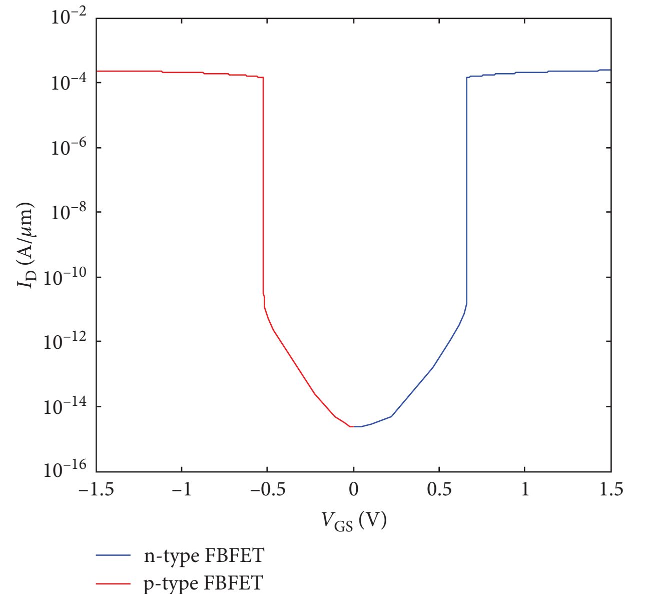
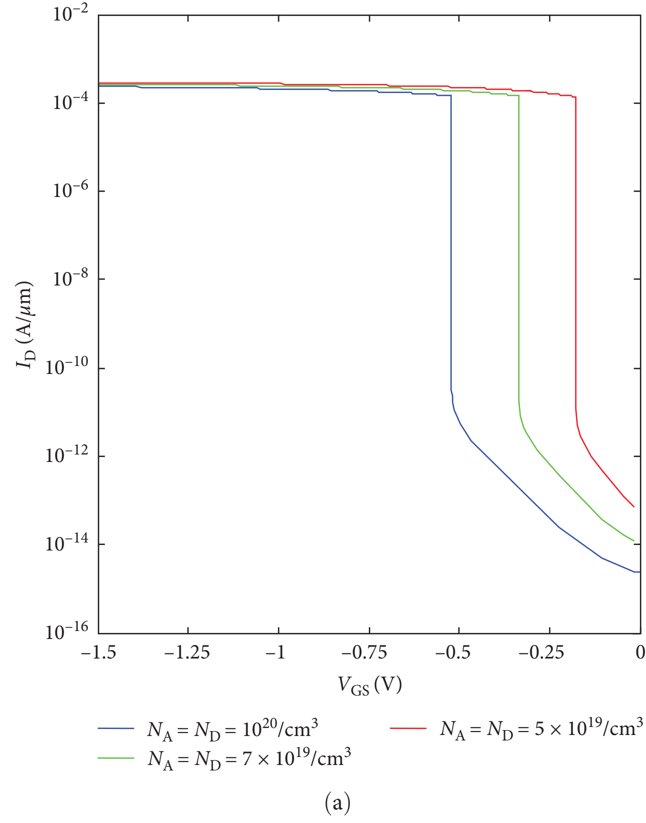
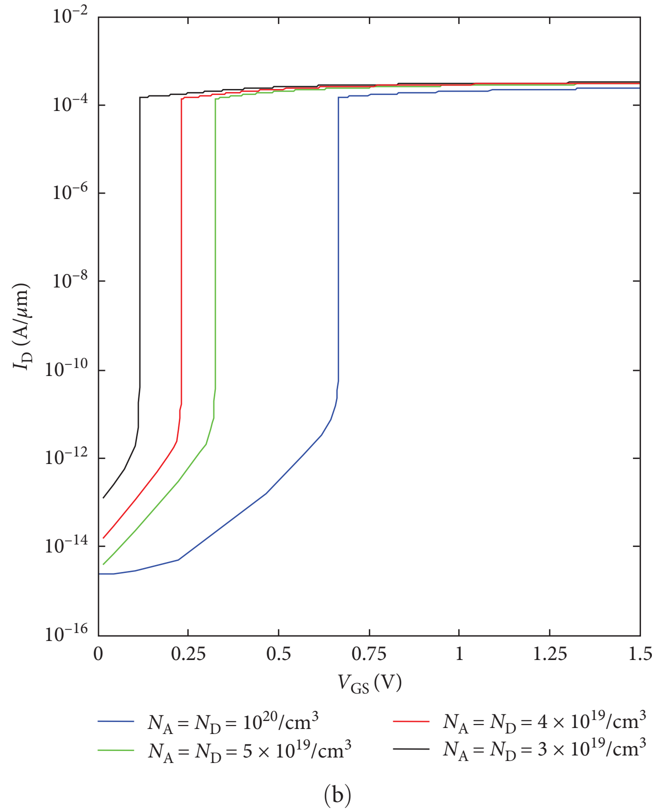


FIGURE 3: Simulated drain current as a function of gate voltage for n-FBFET (blue color) and p-FBFET (red color).

Figure 4 shows the impact of doping levels on the current–voltage characteristics of n-FBFET and p-FBFET structures. From the figure, it can be found that by increasing the doping level, the threshold voltage increases. For n-FBFET and p-FBFET with the doping value of $5\times 10^{19}/cm^3$, the threshold voltages are +0.3 and −0.1 V, respectively. Although the doping level has strong effects on threshold voltage and OFF current, it has a low effect on ON current, according to Figure 4. These threshold voltages play an important role in the inverter characteristics.



(a)



(b)

Figure 4: Simulated drain current as a function of gate voltage for different doping levels for (a) p-FBFET. The blue, green, red curves present the I–V_G curve with doping level of $10^{20}/\text{cm}^3$, $7 \times 10^{19}/\text{cm}^3$, and $5 \times 10^{19}/\text{cm}^3$, respectively. (b) I–V_G for n-FBFET. The blue, green, red, and black curves present the I–V_G curve with a doping level of $10^{20}/\text{cm}^3$, $5 \times 10^{19}/\text{cm}^3$, $4 \times 10^{19}/\text{cm}^3$, and $3 \times 10^{19}/\text{cm}^3$, respectively.

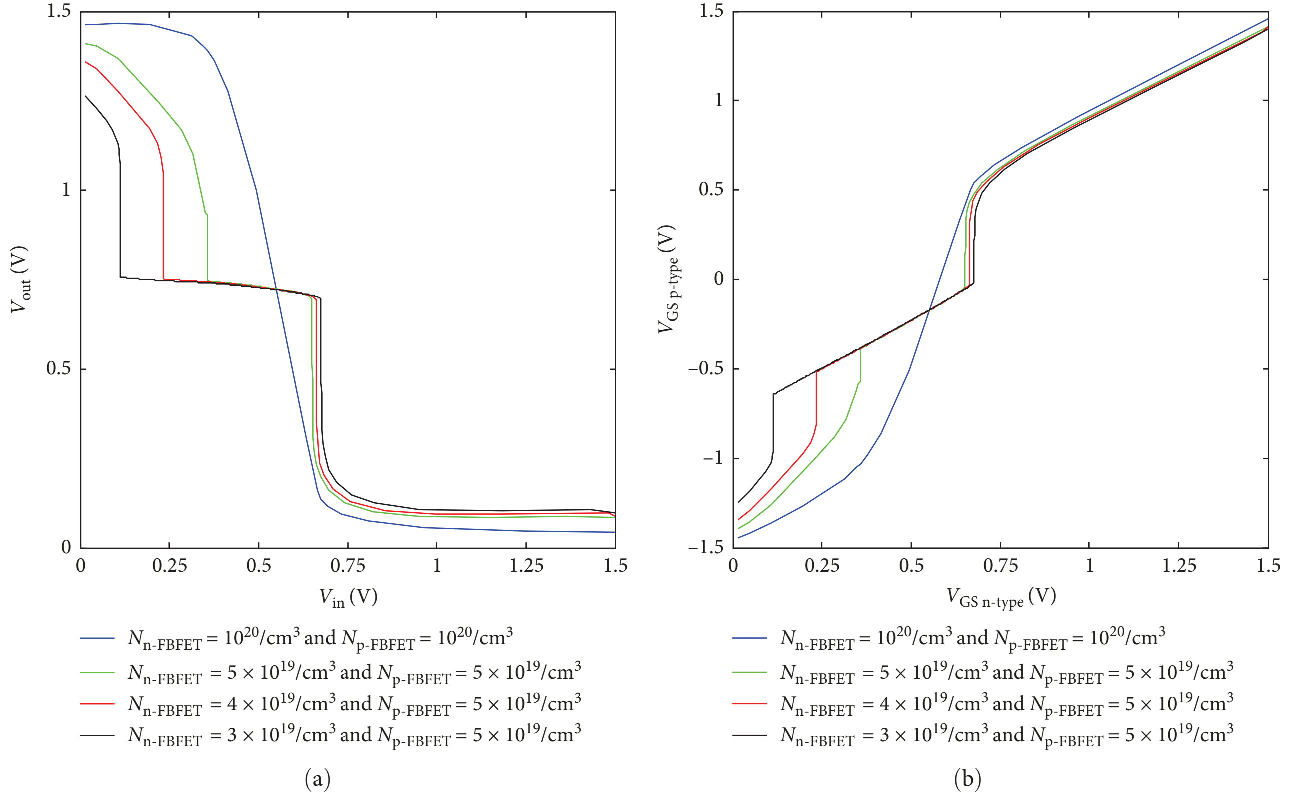


Figure 5: (a) Voltage transfer characteristics of two FBFET-based complementary inverters. (b) Gate-source voltage of p-FBFET versus gate-source of n-FBFET. The blue curve corresponds to doping level of $10^{20}/cm^3$ for n-FBFET and $10^{20}/cm^3$ for p-FBFET. The green curve corresponds to doping level of $5 \times 10^{19}/cm^3$ for n-FBFET and $5 \times 10^{19}/cm^3$ for p-FBFET. The red curve corresponds to doping level of $4 \times 10^{19}/cm^3$ for n-FBFET and $5 \times 10^{19}/cm^3$ for p-FBFET. The black curve corresponds to doping level of $3 \times 10^{19}/cm^3$ for n-FBFET and $5 \times 10^{19}/cm^3$ for p-FBFET.

The voltage transfer characteristics of the designed inverter are shown in Figure 5. The inverter circuit consists of n-FBFET and p-FBFET, as shown in Figure 1. The effect of doping level on the inverter characteristics is shown in Figure 5. From the figure, it can be found that by engineering the doping level, the binary and ternary inverters can be achieved. In Figure 5, the blue curve indicates the binary inverter, while the other colors show the ternary inverter. When the doping level of both n-type and p-type is $10^{20}/cm^3$, the threshold voltage for n-FBFET is 0.64 V, while threshold voltage for p-FBFET is −0.5 V. According to Figure 5(b), when the gate-source of n-FBFET V_{GSn} becomes higher than 0.64 V, the n-FBFET is in ON-state. But the gate-source voltage for p-FBFET, in this case, is higher than −0.5 V (that is, p-FBFET threshold voltage). Thus, when the doping level is $10^{20}/cm^3$, both transistors can not turn on simultaneously. In this case, the voltage transfer curves indicate a binary inverter, as shown in a blue curve. In other case, according to Figure 4, if the doping level for both transistors is $5 \times 10^{19}/cm^3$, the threshold voltage for n-FBFET and p-FBFET is 0.3 and −0.1 V, respectively. Figure 5(b) indicates that for V_{GSn} voltage between 0.3 and 0.6 V, both transistors are in ON state, and in this voltage range, the inverter output is roughly constant. Thus for this level of doping, the behavior of the ternary inverter can be observed.

Propagation delay is one of the most important figures of merits (FOM) for logic inverters. To investigate it, the transient response of ternary and binary inverters are shown in Figures 6(a) and 6(b), respectively. The 50% transition between input and output is defined as propagation delay. The ideal input voltage of the inverter is shown in Figure 6 in blue color, while the output voltage is indicated in green color. Figure 6(a) corresponds to the ternary inverter and has three input/output voltage levels, while Figure 6(b) corresponds to binary inverter and has two input/output voltage levels. The numerical values for ternary inverter indicate that the propagation delays for $0 \rightarrow 2$ and $2 \rightarrow 0$ (6.9 ps) are higher than those for $0 \rightarrow 1$, $1 \rightarrow 2$, $2 \rightarrow 1$, and $1 \rightarrow 0$ transitions (3.4 ps).

Also, the propagation delay for a binary inverter is 10 ps that is higher than a ternary inverter. This is due to higher current for ternary inverters in comparison with binary ones, according to Figure 4. There are two types of power dissipations, i.e., static and dynamic. Static power dissipation corresponds to the leakage between supply and ground, and dynamic one is the power dissipation between switching of the devices. Table 2 compares the electrical characteristics of the FBFET-based inverter with previous devices such as FinFet-based and MOSFET-based inverters. These characteristics include SS, ON/OFF switching ratio, propagation delay,

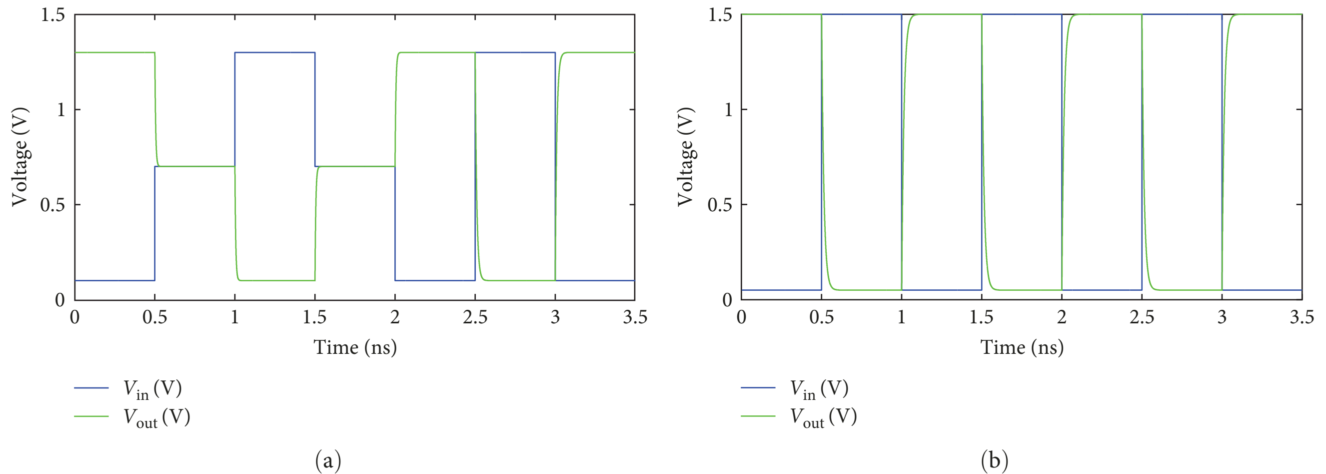


Figure 6: Switching response of the (a) ternary and (b) binary inverter for a load capacitor of 1 pF. The ideal input voltage of the inverter is shown in this figure by blue color, while the output voltage is indicated by green color.

Table 2: Comparison of electrical properties and performance of various inverters.

Inverter structure	SS (mV/decade)	ON/OFF ratio	Propagation delay	Average dissipated power P_{av} (μW)	Power-delay-product (PDP)	Reference
Bulk-MOSFET inverter	121	10^5	5.3 μs	11.3	59.89 pJ	[19]
Bulk-FinFET inverter	72	10^7	1.14 μs	0.83	0.946 pJ	[20]
SOI-FinFET inverter	121	10^5	1.3 ps	3.78	0.0049 fJ	[21]
FBFET inverter	1	10^{10}	3.4 ps	0.12	0.0004 fJ	This work

power consumption, and power-delay-product (PDP). From the table, it can be found that the lowest SS and highest ON/OFF switching ratio belong to FBFET. This is because of positive feedback explained in detail before. The lowest propagation delay time belongs to the SOI-FinFet-based inverter, the reason for which is the large ON current compared to other devices. The large ON current reduces the charge and discharge time of the load capacitor. Although it has a low propagation delay, the power dissipation of the SOI-FinFet-based inverter is high because of false switching current pulses in the off state due to the floating body of SOI [21]. Although the power dissipation in Bulk-Inverter is low due to lower OFF current, it has a higher propagation delay time. Among these devices, FBFET-based inverter has less OFF current, which leads to less power consumption. Therefore, it can be used in low-power applications. One of the important FOM is the PDP. The table shows that the PDP for FBFET-based inverters is less than other devices.

4. Conclusion

A study has been made on FBFET-based inverters, and important figures of merits such as SS, ON/OFF switching ratio, power consumption, propagation delay, and PDP were extracted. The inverter was implemented using a series connection of p-FBFET and n-FBFET. TCAD mixed-mode simulator was used to investigate the electrical characteristics of the designed inverter. The results indicate that by engineering the doping level in the channel, both ternary and binary inverters can be achieved. We observed the low power consumption in the FBFET inverter compared to FinFet one. This low power consumption (0.12 mW) is due to a very low OFF current and very low SS. Also, it can be found that I_{ON}/I_{OFF} ratio of 10^{10} can be observed from the electrical characteristics of the device. The results show that although the propagation delay of FBFET-based inverter is higher than SOI-FinFet-based inverter, the PDP of FBFET is lower compared to all of the devices. Thus, It has been found that for low-power digital applications, FBFET is the preferable option.

Data Availability

Data supporting this research article are available from the corresponding author or first author upon reasonable request.

Conflicts of Interest

The author declares that he has no conflict of interest.

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