Hindawi
International Journal of RF and Microwave Computer-Aided Engineering
Volume 2023, Article ID 1130129, 8 pages
https://doi.org/10.1155/2023/1130129

*Research Article*

# Differential-to-Common-Mode Noise Conversion Suppression on Right-Angle-Bent Differential Transmission Lines Using 3D-Printed Dielectric Materials

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Received 9 November 2022; Revised 4 September 2023; Accepted 5 September 2023; Published 20 September 2023

Academic Editor: Arpan Desai



A method using 3D-printed dielectric materials is proposed to suppress differential-to-common-mode noise conversion in right-angle-bent differential transmission lines. The permittivity of the 3D-printed dielectric material decreases the phase velocity of the shorter inner line of the differential transmission lines. Decreasing the phase velocity of the inner line enables the transmission line phase difference to approach 180°, suppressing differential-to-common-mode noise conversion. Simulation shows that increasing the length of the dielectric material causes a decrease in the phase velocity of the transmission line, suppressing differential-to-common-mode noise. The measured results agree with the simulation, indicating suppression in Scd21. The eye height of the eye diagram improved by 19.63%, improving the system signal integrity.

## 1. Introduction

Modern high-speed signaling uses differential signaling techniques to satisfy the demand for higher data rates. With higher data rates, the importance of signal integrity increased as signals were more prone to external noise [1]. As single-ended signaling is noisy with low signal integrity, differential signaling techniques have been studied because they are highly resilient to noise and electromagnetic interference (EMI) [2]. High resiliency to noise and EMI allowed differential signaling to improve the timing and quality of high data rate signals, thereby improving the signal integrity. Such advantages have led to a wide adaption of differential signaling in printed circuit board (PCB) interconnections. However, an imbalance in the differential signals can lead to EMI and common-mode noise. Because differential signaling transmits signals with a 180° phase difference through two transmission lines, it is crucial to maintain the phase difference for good signal integrity.

With space and layout limitations in PCBs, it became difficult to maintain symmetrical differential transmission lines [3]. An example where the differential signals are asymmetric is right-angle-bent differential transmission lines (DTLs) [4]. Due to the asymmetry in the transmission line lengths of right-angle-bent differential transmission lines, the phase difference diverges from 180°. The inner line of the circuit is shorter than the outer line, causing an asymmetry in the transmission line lengths. When the phase difference diverges from 180°, differential-mode signals convert to common-mode signals creating differential-to-common-mode noise conversion [5]. Previous efforts to suppress differential-to-common-mode noise include changing the width of the microstrip line [6], using compensation inductance [7], using bandgap structures [8], and using U-shaped compensation structures [9] [10–19]. These methods either change the DTL structure or embed a structure in the printed circuit board. In contrast to differential-to-common-mode noise suppression methods, studies in common-mode noise suppression techniques include defected ground structures [20] and absorptive common-mode filters [21].

In this paper, we present a method of suppressing differential-to-common-mode noise by placing a 3D-printed dielectric material on top of the inner line of the DTLs. The 3D-printed dielectric material increases the effective permittivity, decreases the phase velocity, and increases the

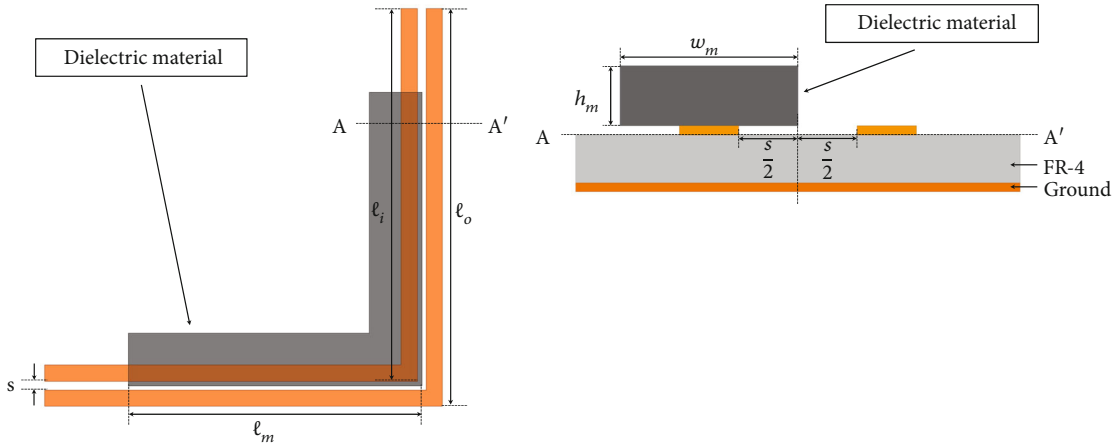



FIGURE 1: Design of the proposed method: (a) top view and (b) side view.

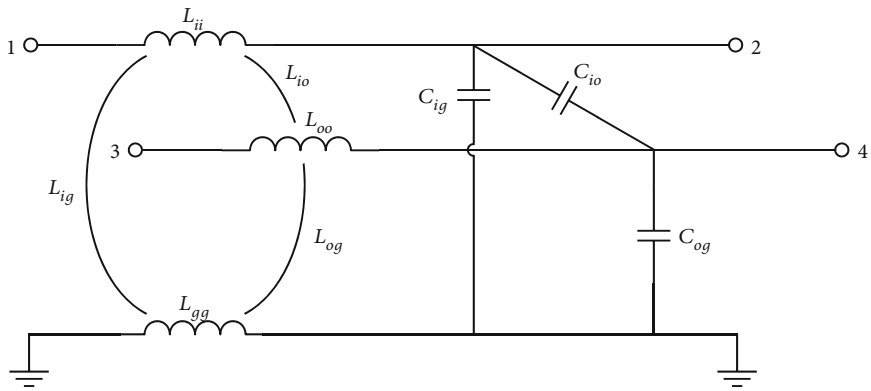



FIGURE 2: Equivalent circuit model of the right-angle-bent differential transmission lines.

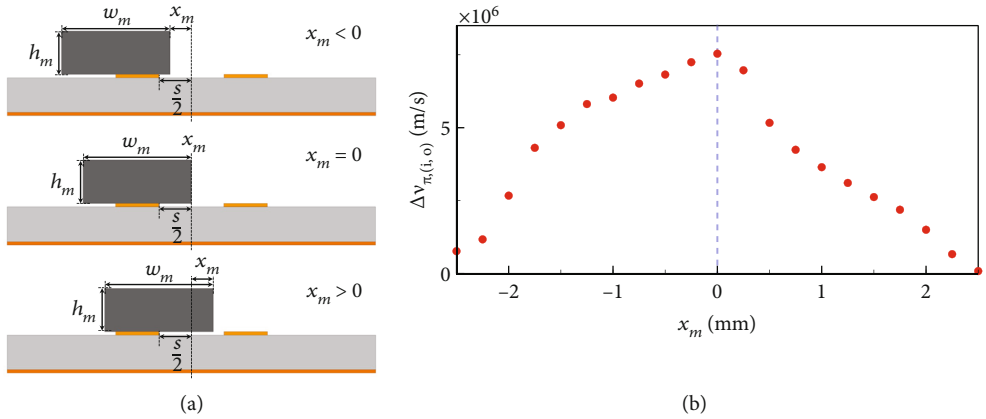



FIGURE 3: Layout (a) and simulated $\Delta v_{\pi,(i,o)}$ (b) as the location ($x_m$) of the dielectric material is changed with the $h_m$ of 2 mm and $w_m$ of 5 mm.

electrical length of the inner line. The decrease in the inner line phase velocity keeps the phase difference between the inner and outer lines close to 180°, and the differential-to-common-mode noise is suppressed. The proposed method is based on the detachable 3D-printed dielectric material on existing DTLs without modifying DTLs. The benefits of the detachable structure are mentioned in Reference [22], where the advantages of a removable electromagnetic band-gap (EBG) common-mode filter are addressed. The detachable structure without modifying the PCBs allows

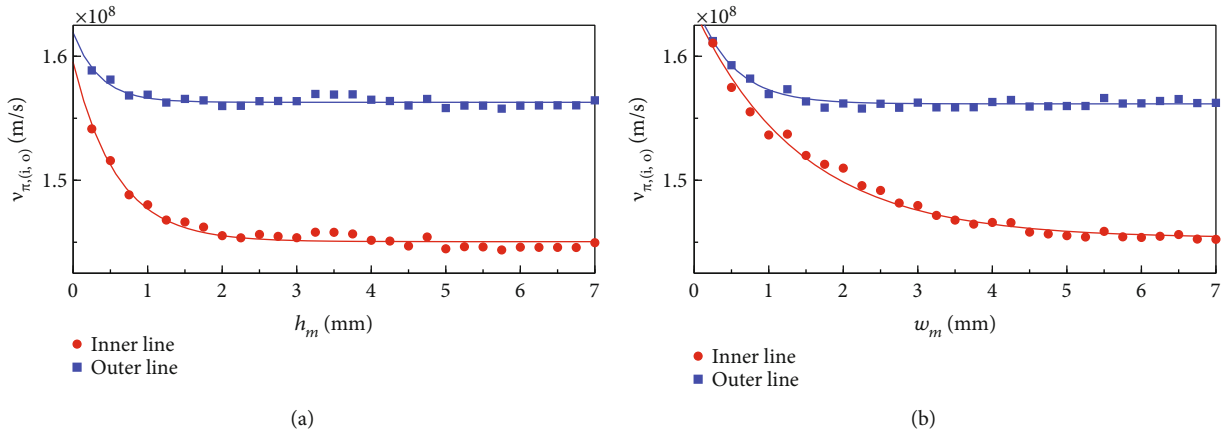



FIGURE 4: Simulated $v_{\pi,i}$ and $v_{\pi,o}$ as (a) height ($h_m$) and (b) width ($w_m$) of the dielectric material increase with the $x_m$ of 0 mm.

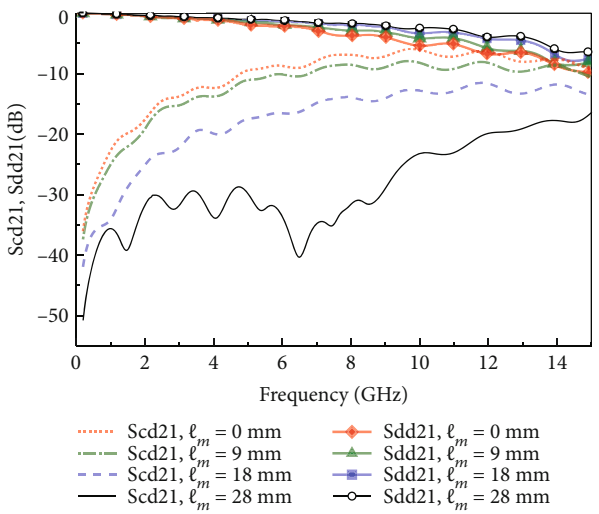



FIGURE 5: Simulated $S$-parameters with increasing $\ell_m$ when $\varepsilon_r = 5.0$.

scalability and flexibility in the structure. In addition, this method can be used along with the previously proposed methods to suppress common-mode noise. Since previous efforts to suppress differential-to-common-mode noise are focusing on the changes of transmission line or ground structures, the proposed method can be used with previous methods, simultaneously. Therefore, the proposed method based on 3D-printed dielectric material has the flexibility to be detached or placed with various PCB structures.

## 2. Design Concept

The substrate used in the right-angle-bent DTLs is FR-4 epoxy with a height of $h = 1.6$ mm and a dielectric constant of 4.4. The dimensions of the DTLs in Figures 1(a) and 1(b) are an inner-line length $\ell_i = 34.15$ mm, outer-line length $\ell_o = 37$ mm, line widths $w_i = w_o = 1.6$ mm, and line spacing $s = 0.75$ mm. A 3D-printed dielectric material with a dielectric constant of $\varepsilon_r$ is placed on top of the right-angle-bent DTLs.

The 3D-printed dielectric material on the inner line increases the effective dielectric constant of the inner line. The increased effective dielectric constant reduces the phase velocity and increases the electrical length of the inner line. The increased electrical length of the inner line compensates for the physical length difference between the inner and outer lines of the DTLs. Therefore, the phase difference between the inner and outer lines is maintained at 180°, and the common-mode noises from the inner and outer line length difference are reduced. The dielectric material is placed on the inner line instead of the outer line because the decrease in the outer line phase velocity will further increase the electrical length difference between the two lines leading to more significant phase divergence.

The optimal location, height, and width of the 3D-printed dielectric material were found by observing the change in the phase velocities. The height and width of the 3D-printed dielectric material adjust the phase velocity of the inner line, and its length adjusts the overall electrical length of the inner line. The length of the 3D-printed dielectric material is changed to match the phase difference of 180° for the inner and outer lines. Because of the added 3D-printed dielectric material, the phase difference matching 180° suppresses differential-to-common-mode noise.

In asymmetric coupled lines, the $\pi$ propagation mode is similar to the odd mode in symmetric coupled lines driven at a phase difference of 180°. The ? mode is used to find the phase velocities of the inner and outer lines ($v_{\pi,i}$, $v_{\pi,o}$). The equations for finding the phase velocities are [23, 24].

$$v_{\pi,i} = \frac{1}{\sqrt{L_{\pi,i}C_{\pi,i}}},$$
$$v_{\pi,o} = \frac{1}{\sqrt{L_{\pi,o}C_{\pi,o}}}, \quad (1)$$

where $L_{\pi,(i,o)}$ and $C_{\pi,(i,o)}$ are the calculated $\pi$ mode inductance and capacitance of the inner and outer lines per unit length. $L_{\pi,(i,o)}$ are calculated with $L_{ii}$, $L_{io}$, $L_{oo}$, $L_{ig}$, $L_{og}$, and $L_{gg}$ using the equations from references [23, 24] (equivalent circuit model shown in Figure 2). As the dielectric material

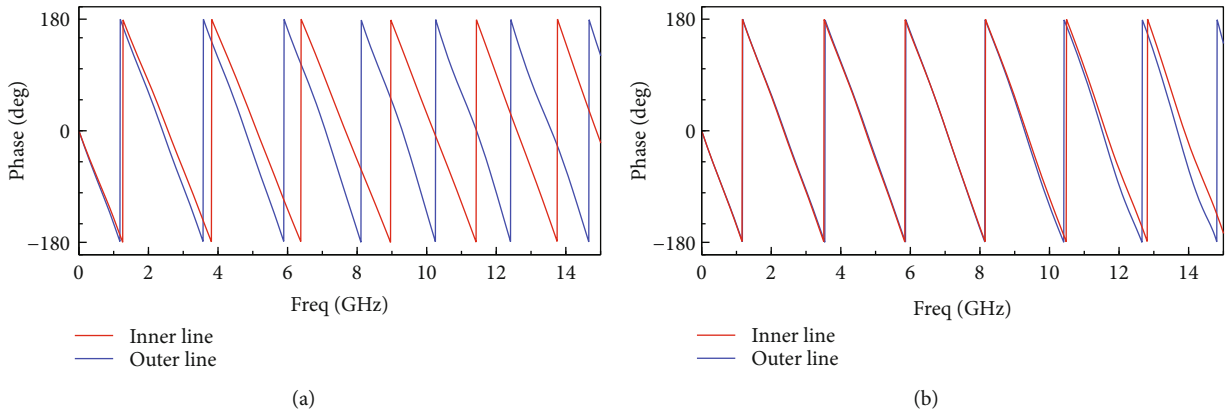



FIGURE 6: Simulated inner and outer line phases in single-ended mode when (a) $\ell_m = 0$ mm and (b) $\ell_m = 28$ mm.

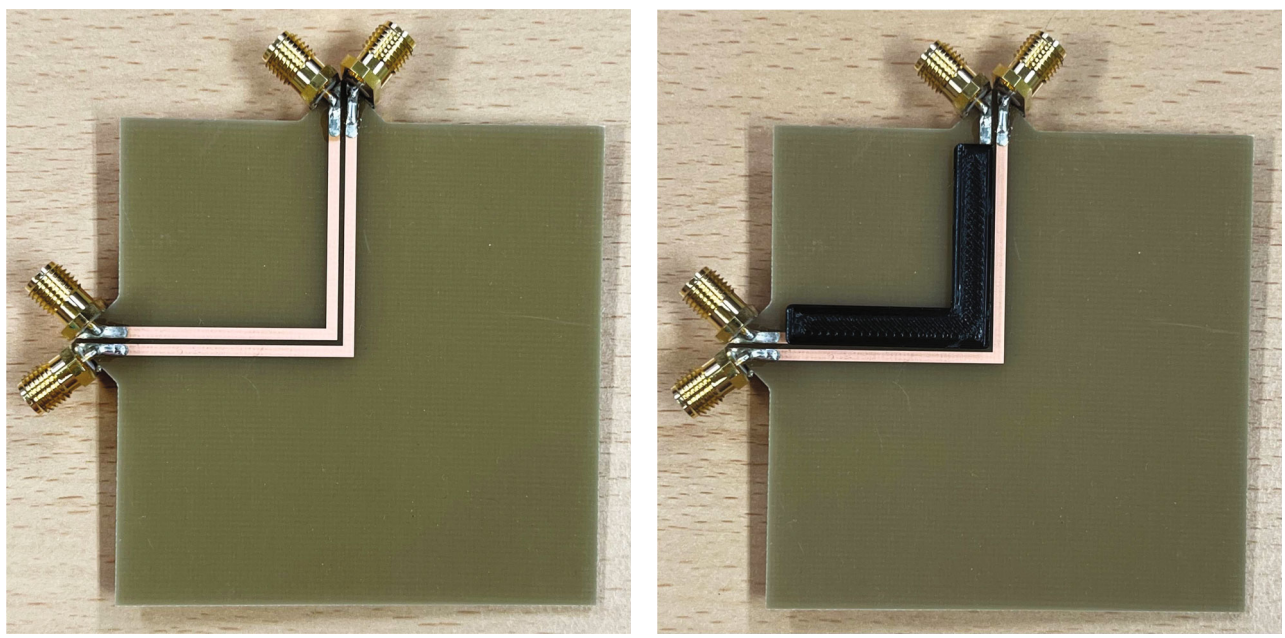



FIGURE 7: Photographs of right-angle-bent DTLs (a) without dielectric material and (b) with a dielectric material.

affects the capacitance of the DTLs while keeping the inductance stable, an increase in the inner line capacitance leads to a decrease in inner line phase velocity. The $\pi$ mode capacitances are found using the following equations [23, 24]:

$$C_{\pi,i} = C_{ig} + 2C_{io},$$
$$C_{\pi,o} = C_{og} + 2C_{io}, \tag{2}$$

where $C_{(i,o)g}$ is the capacitance per unit length between the ground and inner (or outer) line, and $C_{io}$ is the capacitance per unit length between inner and outer lines. The length of the dielectric material increases $C_{ig}$ and $C_{io}$, keeping $C_{og}$ stable and leading to an increase in $C_{\pi,i}$, hence decreasing the phase velocity of the inner line. Among the capacitance analysis methods [25–27], ANSYS Q3D is used to simulate the asymmetric coupled line as the properties of dielectric material change. Calculating the phase velocities with the simulated results tests the validity of the proposed method. The simulated environment uses the 3D-printed dielectric material with $\varepsilon_r = 5.0$ on top of the system.

The optimal location of the dielectric material was found by changing the material location for maximum $\Delta v_{\pi,(i,o)}$ (absolute difference between $v_{\pi,o}$ and $v_{\pi,i}$) with the fixed $h_m$ of 2 mm and $w_m$ of 5 mm. As shown in Figure 3(a), $x_m = 0$ mm is where the right edge of the material is centered between the two DTLs. By observing the simulated result shown in Figure 3(b), the optimal location is selected where maximum $\Delta v_{\pi,(i,o)}$ occurs ($x_m = 0$ mm). Figures 4(a) and 4(b) show the changes in $v_{\pi,i}$ and $v_{\pi,o}$ with increasing height and width. The simulated result of increasing the dielectric material height ($h_m$) shows a decrease in $v_{\pi,i}$, as in Figure 4(a).

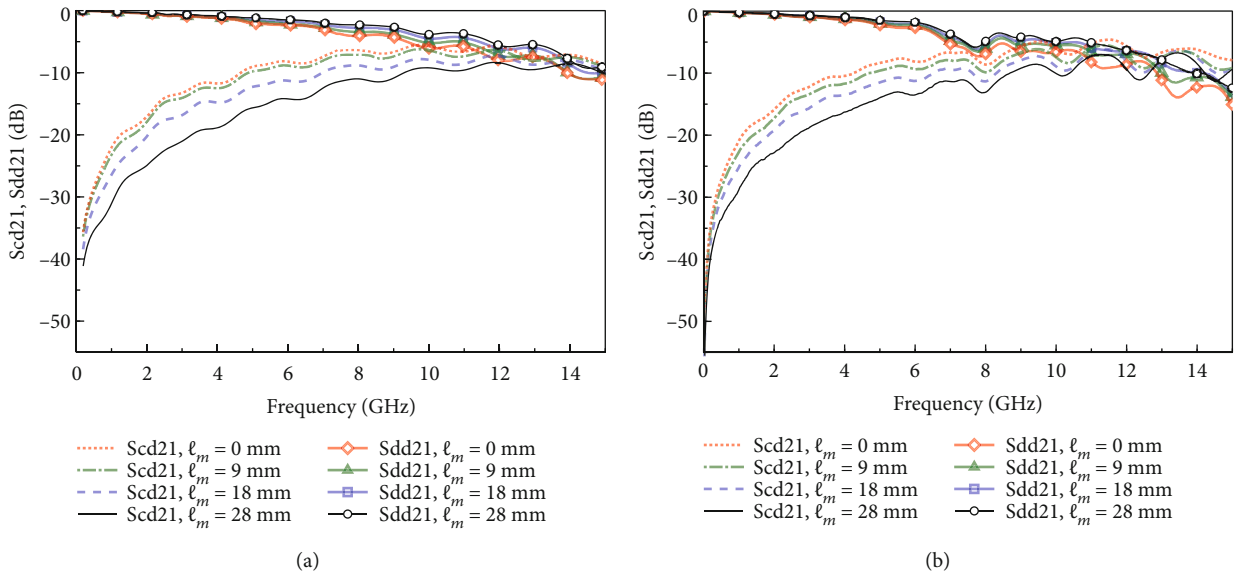



FIGURE 8: *S*-parameters with increasing $\ell_m$ using nylon as the 3D-printed dielectric material (a) simulation (b) measured.

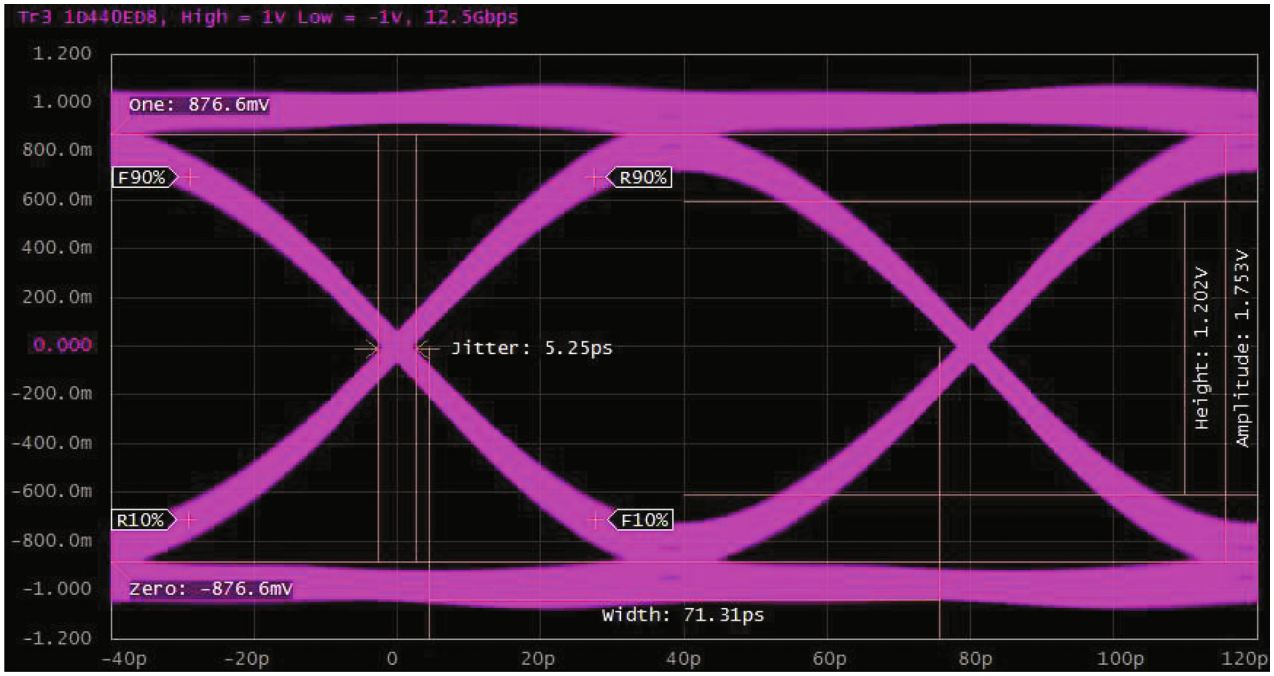
The increase in $h_m$ creates more electric fields in the 3D-printed dielectric material with a higher electric constant, leading to a decrease in $v_{\pi,i}$. A $h_m$ of 2 mm is selected for the experiment because 2 mm is the inflection point of the saturation. After setting $h_m$ to 2 mm, the effect of changing the dielectric-material width ($w_m$) is simulated (Figure 4(b)). From the center of the two signal lines, the width gradually increases away from the center. Like $h_m$, increasing $w_m$ shows a decrease in $v_{\pi,i}$ and saturates as $w_m$ increases. A $w_m$ of 5 mm is selected for the experiment because it is the saturation inflection point. Increasing $h_m$ and $w_m$ increases the inner-line phase and electrical length. To compensate for the difference in length between the inner and outer lines, $v_{\pi,i}$ is kept as low as possible while having no significant change in the inner line inductance ($L_{\pi,i}$).

## 3. Simulation and Experimental Validation

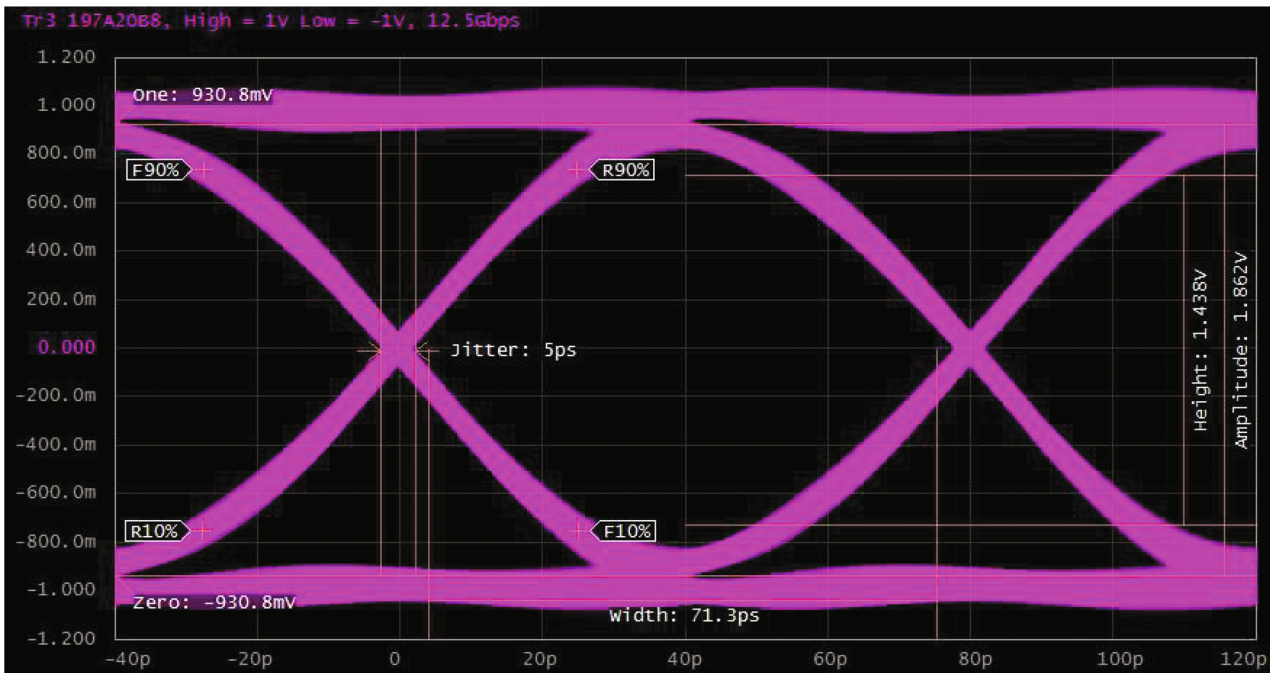
The signal integrity in the differential signals was assessed by evaluating the *S*-parameters of differential insertion loss (Sdd21) and differential-to-common-mode conversion (Scd21). Converting the network into a mixed-mode two-port network from a single-ended four-port network makes it possible to evaluate differential-mode *S*-parameters. Ports 1 and 3 are grouped, and ports 2 and 4 are grouped to form a mixed-mode two-port network. The *S*-parameters were first evaluated through a simulation using ANSYS HFSS. Through simulations, various dielectric material lengths ($\ell_m$) were tested to examine how the performance of the DTLs changed.

Using the simulated phase velocity results, the $h_m$ and $w_m$ for the dielectric material were 2 and 5 mm, respectively. Simultaneously, $\ell_m$ was changed to examine the *S*-parameters. Here, $\ell_m = 0$ (no dielectric material placed), 9, 18, and 28 mm were the critical lengths used in the simulation. The simulated *S*-parameters are shown in Figure 5 for the case in which the dielectric constant of the 3D-printed dielectric material was 5.0. Dielectric material with a dielectric constant of 5.0 was first examined to observe the simulated results of an ideal solution first. An increase in $\ell_m$ decreased Scd21, whereas Sdd21 did not decline severely. The decrease in Scd21 indicates suppression of common-mode noise, whereas a decrease in Sdd21 indicates increasing differential insertion loss. When $\ell_m = 0$ mm was chosen as the base case scenario, $\ell_m = 28$ mm had the most suppression. Increasing the dielectric material length increased the phase and electrical lengths of the inner line and reduced the common-mode noise arising from the length mismatch between the inner and outer lines of the DTLs. The added dielectric material on the inner line reduced the phase velocity and increased the total phase shift. Figures 6(a) and 6(b) show the simulated inner and outer line phases in single-ended mode. The simulated results show that the phase difference between inner and outer lines occurs when $\ell_m = 0$ mm due to the physical length mismatch, and a reduction in phase difference when $\ell_m = 28$ mm. The simulated results in Figures 6(a) and 6(b) show the inner and outer line phases starting at 0° to observe the phase shift of the two lines in a single-ended mode instead of a differential (mixed) mode. The simulated results for $\ell_m = 28$ mm show that the electrical lengths of inner and outer lines are similar, and the electrical length mismatch is reduced.

To validate the simulation results, nylon ($\varepsilon_r = 3.4$) was selected as it has the highest $\varepsilon_r$ value that could be used in the 3D printers available in our experimental environment. Ultimaker S5, a FDM (fused deposition modeling) 3D-printer, was employed to print the dielectric material using the nylon filament. The dielectric material was printed with a resolution of 0.1 mm and a 100% infill setting. The material was printed as an L-shaped block of dielectric material, as




(a)




(b)

Figure 9: Measured eye diagrams: (a) $\ell_m = 0$ mm and (b) $\ell_m = 28$ mm.

Table 1: Measured eye diagram parameters.

| $\ell_m$ (mm) | Eye height (V) | Eye width (ps) | Eye jitter (ps) |
|---|---|---|---|
| 0 | 1.20 | 71.31 | 5.25 |
| 9 | 1.31 | 71.21 | 5.25 |
| 18 | 1.40 | 71.68 | 5.25 |
| 28 | 1.44 | 71.30 | 5.00 |

Table 2: Comparison table with other works.

| Schemes | Scd21 bandwidth under -20 dB | Detachability |
|---|---|---|
| Capacitance compensation [5] | From DC to 3 GHz | X |
| U-shape compensation [9] | From DC to 10 GHz | X |
| Inductance compensation [10] | From DC to 11 GHz | X |
| Periodic structure [18] | From DC to 8 GHz | X |
| 3D-printed dielectric material (this work) | From DC to 11 GHz ($\varepsilon_r = 5.0$)<br>From DC to 3 GHz (with nylon) | O |

shown in Figure 7(b). The 3D-printed dielectric material was placed on the inner line of the DTLs shown in Figure 7(b), whereas Figure 7(a) shows the DTLs without the dielectric material ($\ell_m = 0$ mm). Keysight's E5071C ENA Vector Network Analyzer was used to measure the *S*-parameters and validate the simulation results. The measured *S*-parameters (Figure 8(b)) agree with the simulated results in Figure 8(a). The measured results indicate that a longer dielectric material can suppress Scd21. When $\ell_m = 28$ mm and nylon was used as the 3D-printed dielectric material, the increased phase shift in the inner lines was limited; thus, the decrease in Scd21 was also limited.

Differential eye diagrams were measured using an E5071C Network Analyzer to test the signal integrity of the system. Figures 9(a) and 9(b) show measured eye diagrams for an input data rate of 12.5 Gbps. The measured eye diagram parameters (Figures 9(a) and 9(b) and Table 1) show that the increase in the length of the dielectric material improved the signal quality. The 28 mm dielectric material improved the jitter from 5.25 to 5.00 ps and the eye height by 19.63%.

The method proposed in this paper is compared to previous methods for suppressing differential-to-common-mode noise conversion on right-angle-bent DTLs, as shown in Table 2. Our approach differs from previous methods by providing the advantage of a detachable structure that can be applied to existing structures. Implementing our method enables the suppression of differential-to-common-mode noise conversion without modifying the PCB.

## 4. Conclusion

This paper presents a method of suppressing differential-to-common-mode noise conversion in right-angle-bent DTLs by placing a 3D-printed dielectric material on the inner line. The difference in length between the inner and outer lines could be mitigated by reducing phase velocity and increasing electrical length of the inner line using the dielectric material. An efficient method of adjusting and suppressing noise is adjusting the material length. Material with a high $\varepsilon_r$ is suitable for achieving sufficient differential-to-common-mode noise reduction owing to physical size limitations. The advantage of the proposed method is its flexibility in application. Previous techniques alter the shape and structure of the PCBs before manufacturing; however, the method presented in this paper can be applied to the PCB when needed. The proposed method has the versatility and flexibility to be used along with previous noise suppression techniques. The measured *S*-parameters and eye diagrams showed that the method improved signal integrity. The proposed method achieved differential-to-common-mode noise reduction by maintaining the DTL phase difference at 180°.

## Data Availability

The data used to support the findings of this study are included within the article.

## Conflicts of Interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

## Acknowledgments

This study was supported in part by the Basic Science Research Program through the National Research Foundation of Korea (NRF), funded by the Ministry of Education, Republic of Korea (grant no. NRF-2018R1D1A1B07049347), and in part by Samsung Electronics, Inc.

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