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Research Article

Design of Hybrid Bandpass Filter Chips with High Selectivity and Wideband Using IPD and FBAR Technology

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A novel hybrid bandpass filter (BPF) with wideband and high selectivity is proposed in this paper. The hybrid BPF is composed of two film bulk acoustic resonator (FBAR) cells and three lumped component resonators realized by the integrated passive device (IPD) technology. The *ABCD* matrix to *S*-parameters matrix method is used to calculate the frequency response of the BPF. Moreover, the expressions of transmission zeros (TZs) have been extracted. In the design process, an iterative design approach is proposed to improve the circuit and layout of the hybrid filter based on the packaged acoustic-electric hybrid simulation effect. Finally, two parts of the filter are packaged based on the flip-chip method, and two prototypes for the BPF are measured. The measured results of two chips with 3 dB fractional bandwidth of 13.7% and 15.8% are designed and fabricated, which verifies the validity of the proposed design principle.

1. Introduction

With the increasing development of 5G mobile communication systems, it is becoming more and more important to design a filter chip with the advantages of small size, large bandwidth, and high selectivity. Acoustic wave resonators (AWRs) such as surface acoustic wave (SAW) resonators and film bulk acoustic resonators (FBARs) have the superiorities of excellent quality factor (Q), high sideband roll-off, and small size. A narrowband bandpass filter composed of FBAR is proposed [1]. The simultaneous existence of series and parallel resonance of the FBAR provides high selectivity for the filter. Similarly, a Band-3 duplexer is proposed in [2], which reveals high isolation between its two bands provided by the high selectivity of FBAR. However, these filters consisting of trapezoidal acoustic resonators are usually narrowband filters; due to the double-resonance characteristic combined with a finite electromechanical coupling coefficient (k_t^2), the bandwidth generally reaches a maximum of 200 MHz. Moreover, in C-band, the performance of SAW/FBAR in the broadband and high-frequency fields deteriorates significantly. Cavity filters also have the advantage of low insertion loss. A quad-mode cylindrical cavity dual-band bandpass filter is proposed and achieves insertion loss better than 0.2 dB [3], yet both passbands are too narrow as well.

Correspondingly, for the requirements that are not satisfied with narrowband filters, many of the large bandwidth filters on the market are implemented by the integrated passive device (IPD) technology. An ultraminiaturized bandpass filtering matching network based on GaAs substrate IPD technology is proposed [4], which is suitable for frequency-dependent complex source and load. Two IPD filters with adjustable bandwidth and transmission zeros (TZs) are proposed [5], and the maximum 3 dB fractional bandwidth (FBW) can reach 83.6%. A tunable bandstop filter (BSF) with a wideband balun using IPD technology is proposed for multichip modules [6]. The compact tunable BSF uses barium strontium titanate (BST) varactors demonstrating a tuning range of 55% from 1.3 to 2.3 GHz with a 20 dB rejection level.

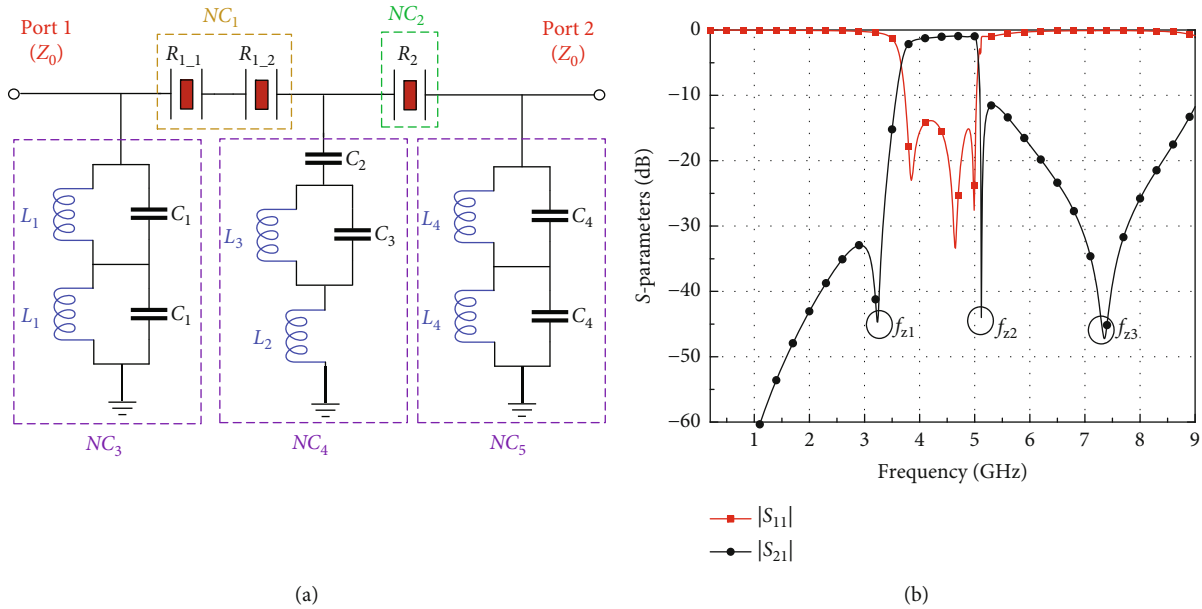


FIGURE 1: (a) The circuit schematic of the proposed hybrid BPF. (b) The simulated results of the ideal circuit ($L_1 = 0.24$ nH, $C_1 = 4.39$ pF, $L_2 = 0.56$ nH, $C_2 = 1.98$ pF, $L_3 = 0.38$ nH, $C_3 = 2.70$ pF, $L_4 = 0.34$ nH, and $C_4 = 3.12$ pF).

However, due to the process limitations, the Q factor of lumped circuit components based on IPD technology generally cannot reach very high, resulting in the fact that it is usually not possible to guarantee low insertion loss and high roll-off at the same time. The functions implemented based on the IPD technology mentioned above have not been able to significantly optimize the roll-off of filtering either. The printed circuit board (PCB) technology is also suitable for wideband filters. A broadband bandpass filter with a cross-shaped resonator and parallel coupled lines is proposed based on PCB technology, which realizes a 3 dB FBW of 58.6% [7]. Yet, the selectivity is not able to compare with FBAR filters.

To solve the above problems, a broadband filter composed of conventional microwave transmission lines (TLs) and SAW resonators is proposed [8]. These filters use the transmission poles and zeros of TLs to control in-band insertion loss (IL) and out-of-band rejection. Wu et al. [9] design and implement broadband hybrid filters by cascading high- and low-pass frequency bands based on FBARs, TLs, and CLs. This design idea allows the bandwidth and TZ to be greatly adjusted, which realizes a bandwidth adjustable from 0.27 GHz to 0.97 GHz. Filters using the same method even provided an FBW of up to 56% [10]. Such bandwidth and its adjustment range are out of reach for the conventional FBAR filters. However, such a design encapsulates the FBAR network onto the PCB board, resulting in its excessive size and not being suitable for intelligent mobile terminals. Due to the inverse correlation between the size of the microstrip line and the operating frequency, it is theoretically proved that in the sub-6G frequency band, the defect of the large size of the filter composed of the microstrip line realized by the PCB technology and the FBAR is unsolvable. Therefore, after changing the way of thinking, a filter combining SAW resonators and surface-mounted device (SMD) inductors is proposed [11]. However, the bandwidth of such a design is too narrow, and the size is still too large to be used for intelligent mobile communication equipment. Two duplexers designed jointly using low-temperature cofired ceramic (LTCC) technology and acoustic resonators are introduced [12, 13]. This design method has successfully reduced the chip size, but IPD technology inherently has higher quality factors and accuracy than LTCC technology. Hybrid filters composed of acoustic and IPD chips are proposed [14–16] and the design process of this type of hybrid filter is summarized, but they do not significantly demonstrate the large bandwidth advantage of hybrid filters. This shows that acoustic wave resonators can be combined with traditional lumped elements without weakening their roll to increase their bandwidth. The impact of the size of the lumped element on its operating frequency band is significantly smaller than that of TL, ensuring that IPD technology can be used for implementation in the sub-6G frequency band. A hybrid filter circuit containing five series FBARs is proposed in Chapter 5.2 of [16], but the losses caused by lumped components are not considered in the circuit design, resulting in a significant difference between its EM simulation and circuit performance. This work refers to its circuit structure and FBAR layout and proposes better circuits, layouts, and design processes.

In this paper, a novel hybrid bandpass filter (BPF) with an operating frequency range of 3.8-5.0 GHz is constructed by combining the lumped element realized by IPD technology and FBAR cells. The overall structure of the filter is shown in Figure 1(a). The filter is analyzed using the *ABCD* matrix analysis method and the Butterworth-Van Dyke (BVD) model of FBAR [17]. Through the advantageous characteristics of FBAR, the roll-off of the upper sideband is strengthened, and it also has the advantage of the large bandwidth of the IPD filter.

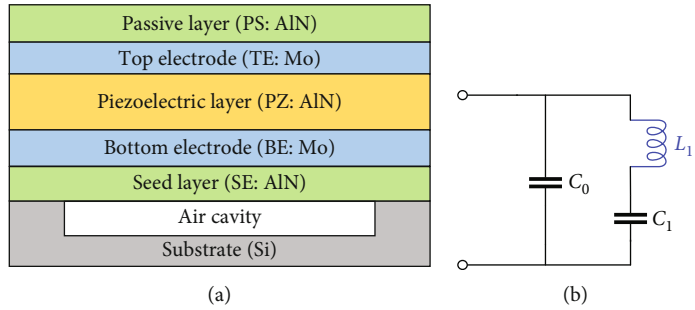


Figure 2: (a) The stack of an FBAR. (b) The circuit of the BVD model.

2. The Proposed BPF

As shown in Figure 1(a), three sets of lumped element-based parallel paths are used to control the low-frequency TZs and in-band matching. The upper sideband of the filter is defined by two sets of FBAR networks connected in series, which result in an excellent roll-off of the upper sideband of the filter. Each of the resonators provides one TP, which does not mean that when they are connected as a filter, five TPs should be observed. The characteristic impedance (Z_0) of the two lines connected to port 1 and port 2 is 50 Ω. When the Q factor of all inductors (Q_L) is set at 30 and capacitors (Q_C) at 200, the ideal frequency responses are shown in Figure 1(b). The resonant frequencies of an FBAR are determined by the stacks, as shown in Figure 2(a).

2.1. Scattering Parameter Theory. To calculate the frequency response of the circuit, the expression for the electrical properties of a single FBAR needs to be calculated first. In [17], the impedance expression of FBAR under the equivalence of the BVD model shown in Figure 2(b) is

$$Z_{\mathrm{FBAR}} = \frac{j(\omega L_1 - 1/\omega C_1)}{1 - \omega^2 C_0 L_1 + C_0/C_1}, \tag{1}$$

where L_1 is the motional inductor and C_1 is the motional capacitor, both in series modeling the series resonance of an FBAR in parallel with a plate capacitor C_0. The stack of two FBARs in NC_1 is the same, which means they have the same impedance.

As shown in Figure 1(a), the hybrid filter is composed of two series cells (NC_1, NC_2) and three parallel cells (NC_3, N C_4, and NC_5). Among them, the two resonators in NC_1 were originally one, and they were split into two identical resonators to control the area. After the impedance of a single FBAR is obtained, according to [18], the *ABCD* matrix of the five branches in Figure 1(a) can be written as

$$[A]_{\mathrm{NC}_1} = \begin{bmatrix} 1 & Z_{R_{1\_1}} + Z_{R_{1\_2}} \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 2Z_{R_{1\_1}} \\ 0 & 1 \end{bmatrix},$$
$$[A]_{\mathrm{NC}_2} = \begin{bmatrix} 1 & Z_{R_2} \\ 0 & 1 \end{bmatrix}. \tag{2}$$

$$[A]_{\mathrm{NC}_3} = \begin{bmatrix} 1 & 0 \\ \left(2 \times \dfrac{(1/j\omega C_1) \times j\omega L_1}{(1/j\omega C_1) + j\omega L_1}\right)^{-1} & 1 \end{bmatrix}, \tag{3}$$

$$[A]_{\mathrm{NC}_4} = \begin{bmatrix} 1 & 0 \\ \left(\dfrac{(1/j\omega C_3) \times j\omega L_3}{(1/j\omega C_3) + j\omega L_3} + \dfrac{1}{j\omega C_2} + j\omega L_2\right)^{-1} & 1 \end{bmatrix}, \tag{4}$$

$$[A]_{\mathrm{NC}_5} = \begin{bmatrix} 1 & 0 \\ \left(2 \times \dfrac{(1/j\omega C_4) \times j\omega L_4}{(1/j\omega C_4) + j\omega L_4}\right)^{-1} & 1 \end{bmatrix}, \tag{5}$$

where Z_{R1_1} and Z_{R2} are calculated by (1).

The *ABCD* matrix of the whole filter is the product of these five branches, which means

$$[A]_0 = \underbrace{[A]_{\mathrm{NC}_1}[A]_{\mathrm{NC}_2} \cdots [A]_{\mathrm{NC}_5}}_{5\ \text{matrixes}} = \begin{bmatrix} 1 + Z_{\mathrm{F}} Z_{\mathrm{LC}} & Z_{\mathrm{F}} \\ Z_{\mathrm{LC}} & 1 \end{bmatrix}, \tag{6}$$

where

$$Z_{\mathrm{F}} = 2Z_{R_{1\_1}} + Z_{R_2}, \tag{7}$$

$$Z_{\mathrm{LC}} = K_1 + K_4 + \frac{1}{(1/j\omega C_2) + j\omega L_2 + (1/K_3)}, \tag{8}$$

$$K_i|_{i=1,2,3,4} = \frac{C_i((1/j\omega C_i) + j\omega L_i)}{2L_i}. \tag{9}$$

After the *ABCD* matrix of the whole filter is calculated, according to [18], the conversion relationship between the *S*-parameters and the *ABCD* matrix of the two-port reciprocal lossless network is

$$S_{11} = \frac{A + B/Z_0 - CZ_0 - D}{A + B/Z_0 + CZ_0 + D}, \tag{10}$$

$$S_{21} = \frac{2}{A + B/Z_0 + CZ_0 + D}. \tag{11}$$

Bring (6)–(9) into (10) and (11), resulting in the *S*-parameters of the hole hybrid filter which can be expressed

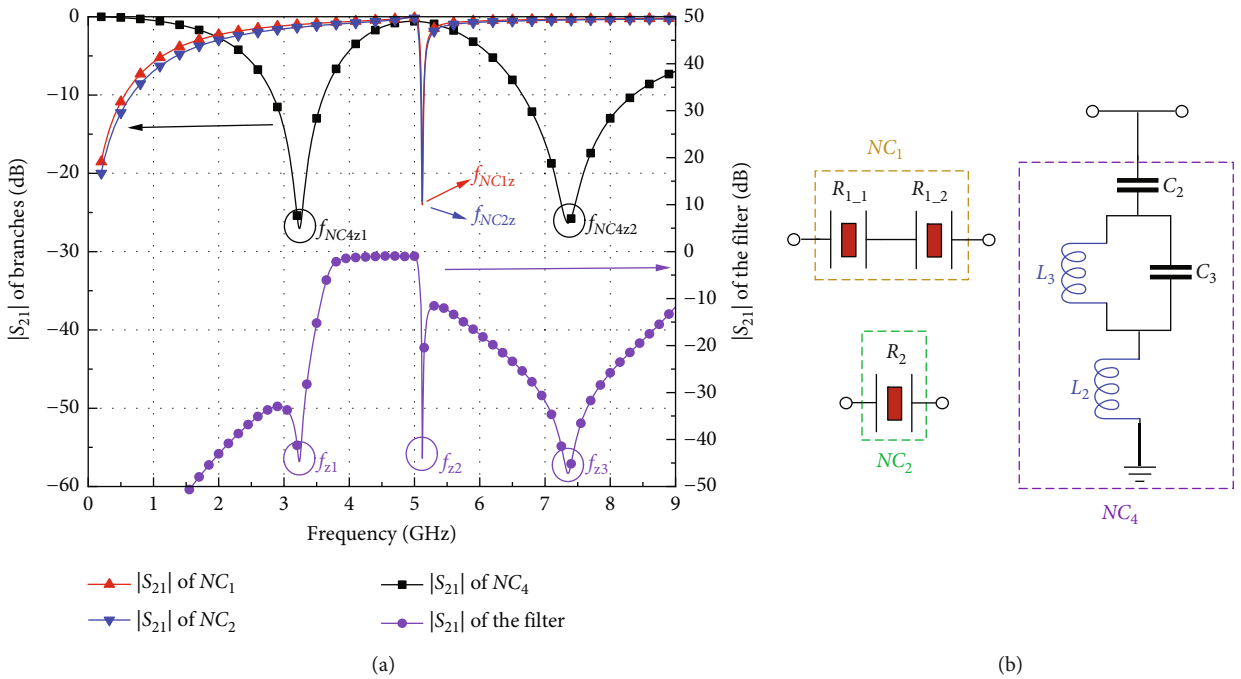


FIGURE 3: (a) The ILs of the filter and LC branches. (b) The independent view of NC_1, NC_2, and NC_4.

as

$$S_{11} = \frac{Z_F Z_{LC} + Z_F/Z_0 - Z_{LC}Z_0}{Z_F Z_{LC} + Z_F/Z_0 + Z_{LC}Z_0 + 2}, \tag{12}$$

$$S_{21} = \frac{2}{(Z_F Z_{LC} + Z_F/Z_0 + Z_{LC}Z_0 + 2)}, \tag{13}$$

2.2. Transmission Zeros and Controllable Bandwidth. The TZs can be obtained when $S_{21} = 0$ is satisfied. Unfortunately, it is too complicated to insert (6)–(9) to (11), simplify, and solve the equation. As shown in Figure 3(a), f_{z1} and f_{z3} of the filter are at the same frequencies as the TZs proposed by NC_4, and f_{z2} is proposed by f_{NC1z} and f_{NC2z}, which are at the same frequency, due to their same stack. In theory, f_{z1} and f_{z3} are provided by C_2 and L_2, respectively, and are independently regulated by C_2 and L_2. The simulation results shown in Figure 3(a) further prove that the TZs provided by L_2, C_2, and FBAR cells are not affected by each other, resulting in a frequency offset. Thus, the expressions of f_{z1} and f_{z3} are the same as f_{NC4z1} and f_{NC4z2}, which means by analyzing NC_4, as shown in Figure 3(b), f_{z1} and f_{z3} are easy to calculate.

Using the same method, f_{NC4z1} and f_{NC4z2} can be obtained when $S_{21NC4} = 0$ is satisfied. By inserting (4) into (11), the expression of S_{21NC4} can be calculated as

$$S_{21NC4} = \frac{2Z_{NC4}}{Z_0 + 2Z_{NC4}}, \tag{14}$$

where

$$Z_{NC4} = \frac{(1/j\omega C_3) \times j\omega L_3}{(1/j\omega C_3) + j\omega L_3} + \frac{1}{j\omega C_2} + j\omega L_2. \tag{15}$$

When $S_{21NC4} = 0$ is satisfied, frequencies of f_{z1} and f_{z3}, which are the same as f_{NC4z1} and f_{NC4z2}, can be extracted as

$$f_{z1} = \frac{1}{2\pi}\sqrt{\frac{p-q}{2C_2C_3L_2L_3}},$$
$$f_{z3} = \frac{1}{2\pi}\sqrt{\frac{p+q}{2C_2C_3L_2L_3}}, \tag{16}$$

where

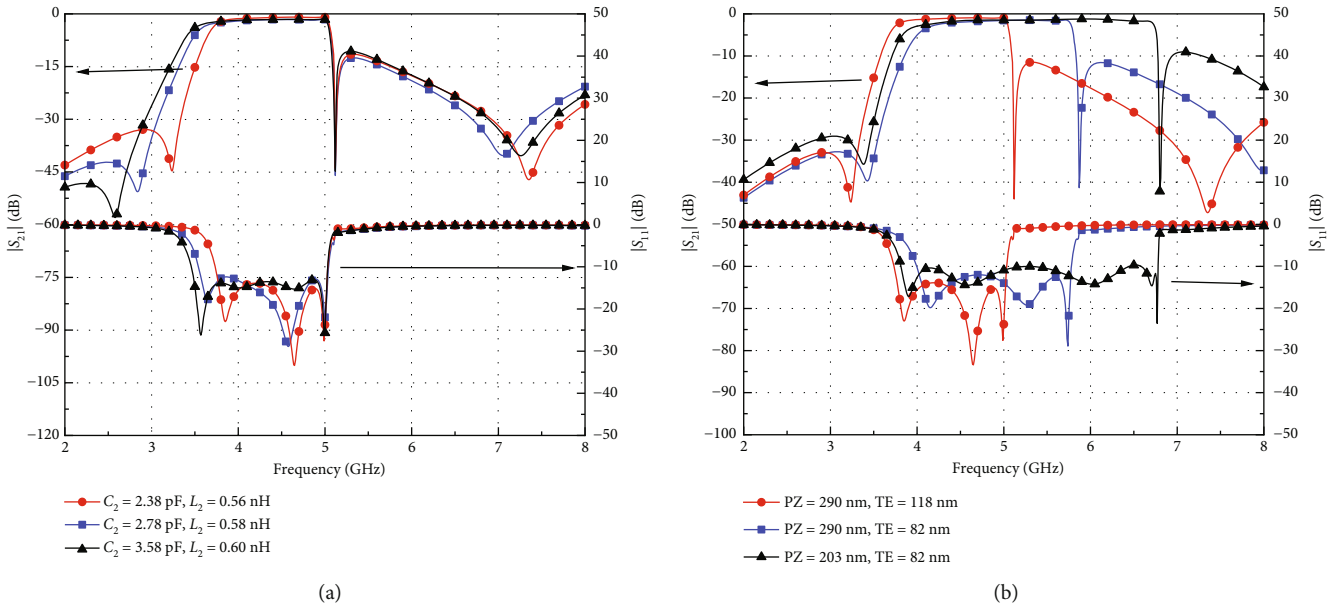
$$p = C_2L_2 + C_2L_3 + C_3L_3,$$
$$q = \sqrt{(C_2L_2 - C_3L_3)^2 + C_2L_3(2C_3L_3 + 2C_2L_2 + C_2L_3)}. \tag{17}$$

As to the expression of f_{z2}, it can be seen from Figure 3(a) that f_{z2} is at the same frequency as f_{NC1z} and f_{NC2z}. In [17], the expressions of series resonant frequency (f_s) and parallel resonant frequency (f_p) of the BVD model are extracted as

$$\omega_s = \frac{1}{\sqrt{L_1C_1}}, \tag{18}$$

$$\omega_p = \sqrt{\frac{C_1 + C_0}{L_1C_1C_0}} = \omega_s\sqrt{1 + \frac{C_1}{C_0}}. \tag{19}$$

In this case, the FBAR cells are connected in series in the circuit, resulting in the f_p producing the TZ of the upper sideband and the f_s producing the transmission



(a) (b)

FIGURE 4: The simulated frequency response versus the values of (a) L_2 and C_2 and (b) PZ and TE (PS = 80 nm).

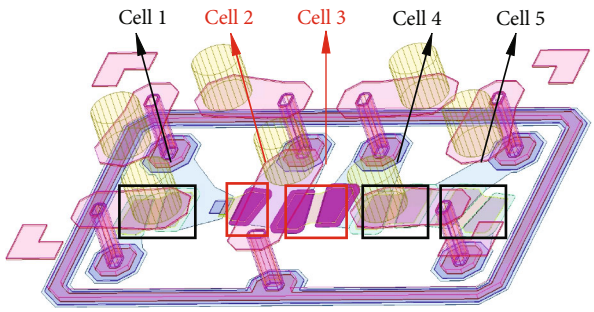


FIGURE 5: The EM model of the FBAR chip.

pole (TP) which is next to the TZ. Thus, the expression of f_{z2} is the same as (19):

$$f_{z2} = \frac{\omega_p}{2\pi}. \tag{20}$$

It should be noted that the BVD model cannot accurately describe the acoustic losses of the FBARs, which does not affect the analysis of resonant frequency. However, when it comes to the analysis of the Q factor and losses, the modified BVD (mBVD) model, which can accurately describe the various losses of the resonator, should be used.

Figure 4(a) shows the variation of f_{z1}, which is determined by C_2 and L_2. The TZ provided by FBAR can also be independently regulated. By changing the thickness of FBAR layers, the upper sideband can be significantly adjusted to change bandwidth, as shown in Figure 4(b). When the thickness of the FBAR layer changes, its static capacitance value will also change. To ensure matching, the value of the lumped component is also adjusted, so the TZ of the lower sideband is frequency-shifted, as shown in Figure 4(b). Therefore, the upper and lower sidebands can be independently regulated, and the bandwidth can be adjusted freely.

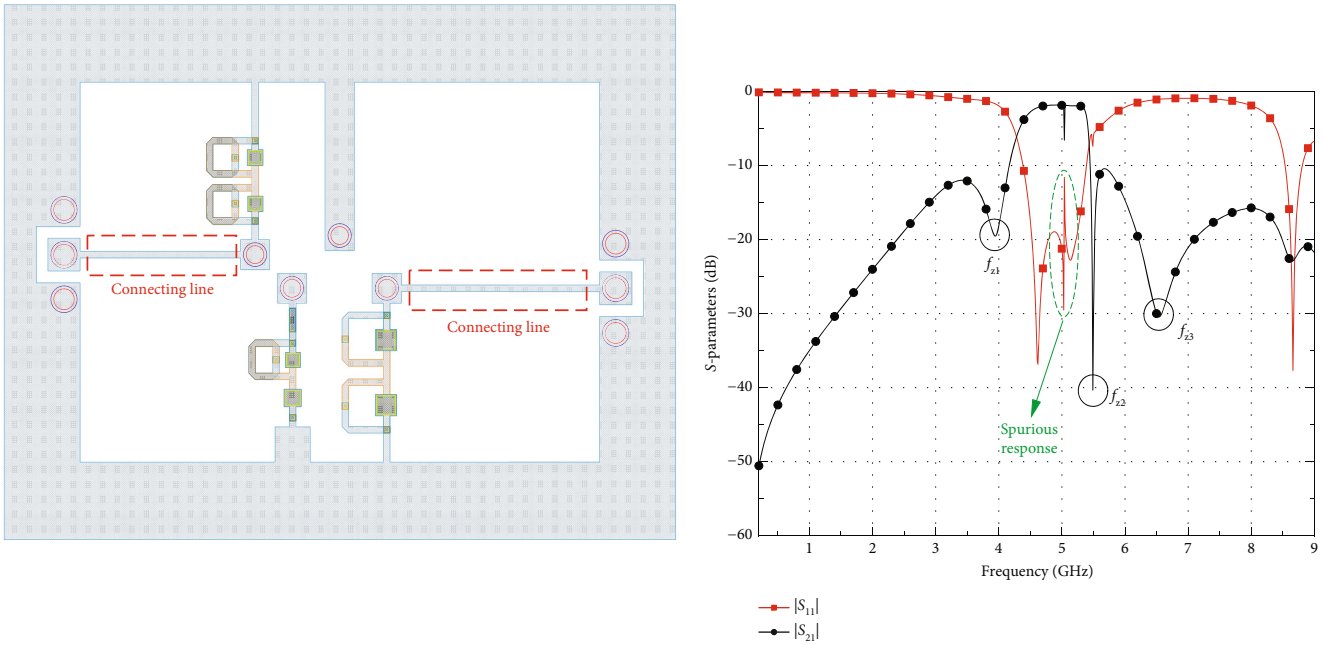
TABLE 1: Stacks and resonant frequencies of R_1 and R_2.

	Thickness (nm)					Resonant frequencies[1] (GHz)
	PS	TE	PZ	BE	SEED	
R_1	160	75	290	140	30	f_{s1}: 5.343, f_{p1}: 5.530
R_2	160	75	290	140	30	f_{s1}: 5.343, f_{p1}: 5.530

[1] f_{si} and f_{pi} ($i = 1, 2$) are series resonant frequencies and parallel resonant frequencies of R_1 and R_2.

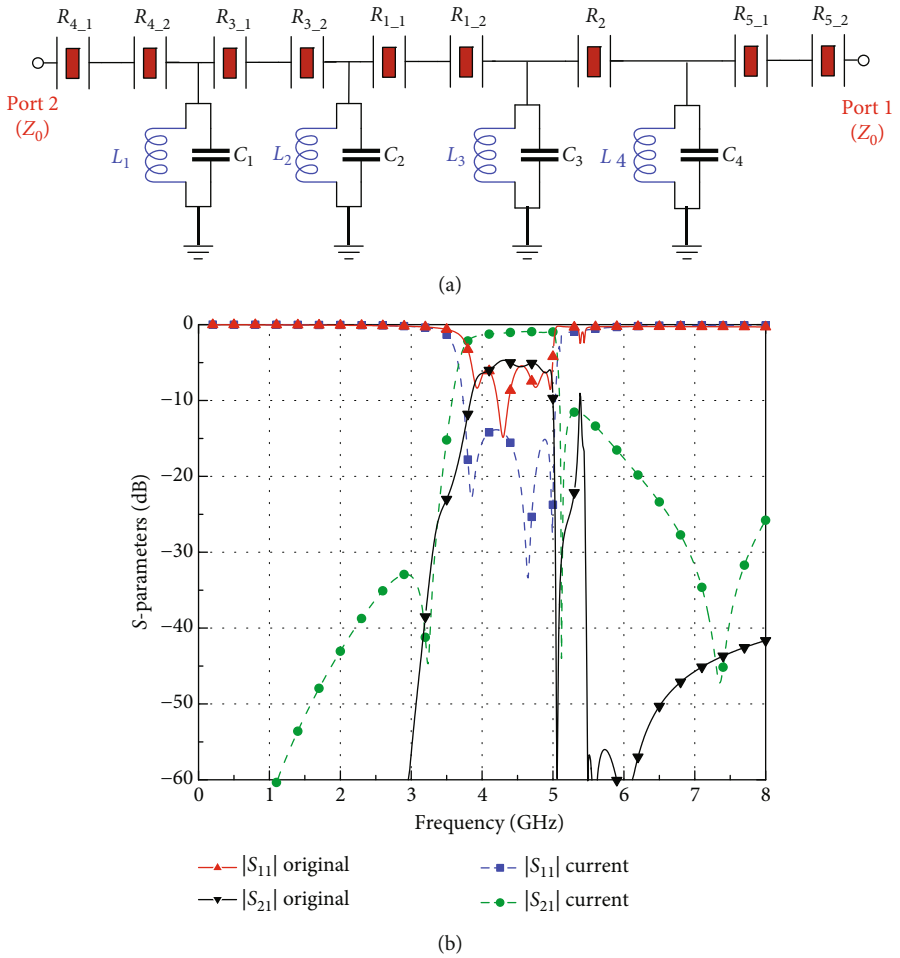
3. Full-Wave Simulation and Experimental Validation

For a demonstration, two prototypes operating at 4.08-5.45 GHz are simulated, manufactured, and measured. Traditionally, packaging chips use the method of front-mount wiring bonding to combine the two parts of the chip. Generally, the corresponding ports are connected using a gold wire, which is convenient and efficient. However, this will cause the dielectric part of the upper chip to be sandwiched between the metal layer of the upper chip and the lower chip's metal, resulting in unavoidable and uncontrollable parasitic effects. The method of flipping chips (FC) on a PCB substrate for packaging is proposed [19, 20]. As for FBAR and IPD, this paper uses the IPD chip as the substrate, flips the FBAR chip on the IPD chip, and uses the Ni and SnAg parts on the copper pillar of both chips to weld the two corresponding port pads together. The IPD technology adopted in this paper does not use the back metal to improve the Q value of the inductance. Therefore, when the reverse package is adopted, a circle of metal is designed outside the



(a) (b)

FIGURE 6: (a) The original IPD layout with GSG ports. (b) The acoustic-electric hybrid simulation results based on the original IPD chip.



(a)

(b)

FIGURE 7: (a) The originally designed circuit. (b) The acoustic-electric hybrid simulation results of the originally designed circuit based on the measured FBAR chip and lumped component with losses.

IPD circuit as the ground. The EM model of the FBAR part is shown in Figure 5. The resonant frequencies of FBARs are determined by their stacks. To reduce the free variables, stacks are preselected for R_1 and R_2, where R_1 represents R_{1_1} and R_{1_2}. Their stacks and series/parallel resonance frequencies (f_{si} and f_{pi}, $i = 1, 2$) are listed in Table 1. The design process of this work is as follows: firstly, tape out the FBAR chip with the predetermined stack, and then, adjust the IPD chip based on the performance of the FBAR chip and the selected packaging method to optimize the hybrid filtering performance.

Starting from this chapter, the simulation results are all based on acoustic-electrical hybrid simulations of the FBAR chip, instead of schematic simulations.

3.1. Packaging with the GSG Port IPD Chip (Chip A). It should be noted that since the IPD chip is used as the substrate and the actual size of the FBAR chip after cutting will be slightly larger than its 3-D modeling size, the chip size of the IPD needs to be much larger than the FBAR chip to ensure that the GSG port on the IPD chip after packaging not be covered by the FBAR chip. The originally designed IPD layout and the acoustic-electric hybrid simulation are shown in Figures 6(a) and 6(b). It can be seen that because the IPD needs to be enlarged in size, there is a large gap between the two GSG ports and the circuit part, and a connecting line is needed to connect them. The connecting line of this length can be equivalent to a small inductor, which leads to the performance of the filter further deteriorating. Thus, this paper considers the use of series lumped element resonators that provide TPs instead, to reduce the influence of equivalent inductance.

Compared with the circuit of the proposed hybrid filter, it can be found that the tape-out FBAR chip has three more FBAR cells (cell 1, cell 4, and cell 5) than the original design (cell 2 stands for NC_2, cell 3 stands for NC_1). At the beginning of the design, the design follows the traditional FBAR design approach, using multiple series resonators and multiple parallel connections. However, for hybrid designs, this approach can lead to a sharp deterioration of ILs and the emergence of out-of-band parasitic responses, increasing the complexity of the design. The originally designed circuit is shown in Figure 7(a), yet the lumped components in the design do not consider the Q value. After the FBAR chip is taped out, simulations are conducted based on the EM model of the FBAR chip and lumped components considering losses ($Q_L = 30$, $Q_C = 200$). The simulated ILs reach around 5 dB, as shown in Figure 7(b), which means too many resonators will lead to a high loss. Therefore, decrease the number of resonators of the circuit and design the circuit in Figure 1(a). The actual equivalent circuit based on the EM model is shown in Figure 8. Due to the influence of the acoustic performance of the FBAR, even if the FBAR is not fully connected to the circuit, that is, only one port is connected to the circuit, it will still have an impact on the final filtering performance. In this design, it is specifically manifested as parasitic in the passband, as shown in Figure 6(b). It should be noticed that such parasitism only appears on the level of acoustic-electric hybrid simulation,

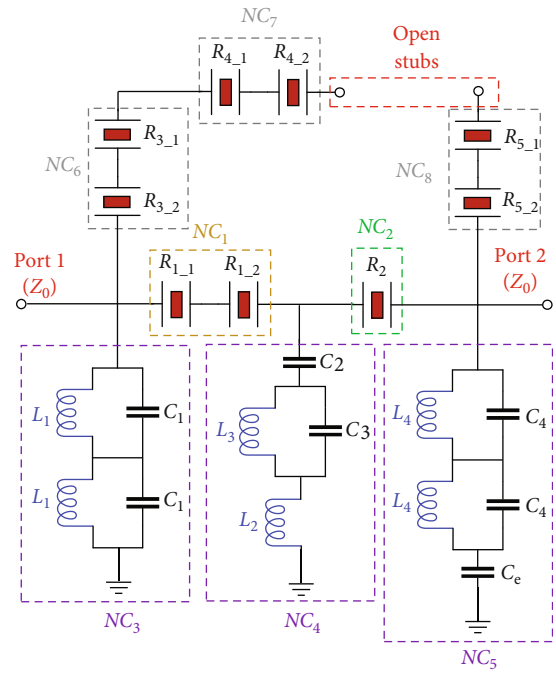


FIGURE 8: The actual equivalent circuit based on the EM model of the FBAR chip (NC_6 stands for cell 4, NC_7 stands for cell 5, and NC_8 stands for cell 1).

as the ideal model of an FBAR does not independently and specifically reflect its acoustic performance and EM performance. Unfortunately, the current conditions are not enough to support another tape-out, so it is necessary to design additional traces at the layout level to suppress parasitic effects.

The acoustic performance of an FBAR can only be activated when a potential difference exists between the upper and lower electrodes and the piezoelectric layer is electrically excited. The piezoelectric layer cannot be electrically excited when only one end of the resonator is connected to the circuit. However, nearby resonators will couple a portion of energy to the one-port-connected FBAR, resulting in an uncontrollable parasitic response. To observe the performance impact on the whole circuit of FBAR with a single port access circuit more intuitively, a first-order network composed of NC_3 and an FBAR is designed, as shown in Figure 9(a), and simulated on the level of acoustic-electric hybrid simulation. In theory, a separate TP should be provided by NC_3. It can be seen in Figure 9(b) that when the FBAR is connected to the circuit with only one port, a significant parasitic response appears in the simulation results. To erase that, a small inductor L_0 which is supposed to simulate the metal wiring is designed to connect to both ends of the FBAR, ensuring that there is no potential difference between the upper and lower electrodes, resulting in the parasitic response almost disappearing entirely, with only a slight frequency shift. It should be noted that the suppression effect of this parasitic response will weaken as the complexity of the circuit increases. Therefore, using the same method will worsen the effects of suppressing parasitic effects for the entire circuit.

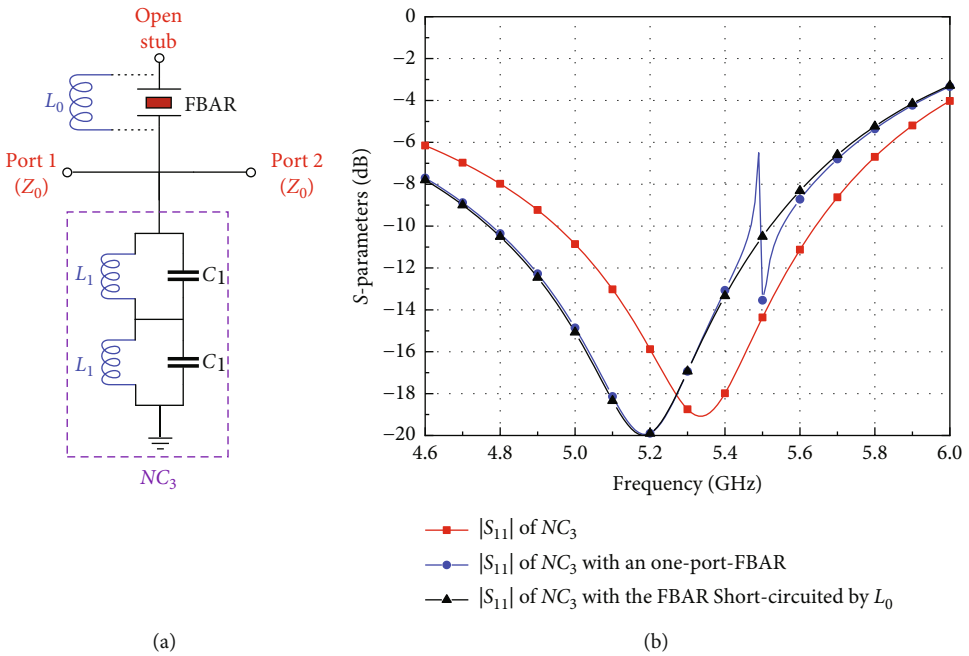


FIGURE 9: (a) The circuit of the first-order network. (b) The acoustic-electric hybrid simulation results in different statuses (L_0 = 0.0001 nH).

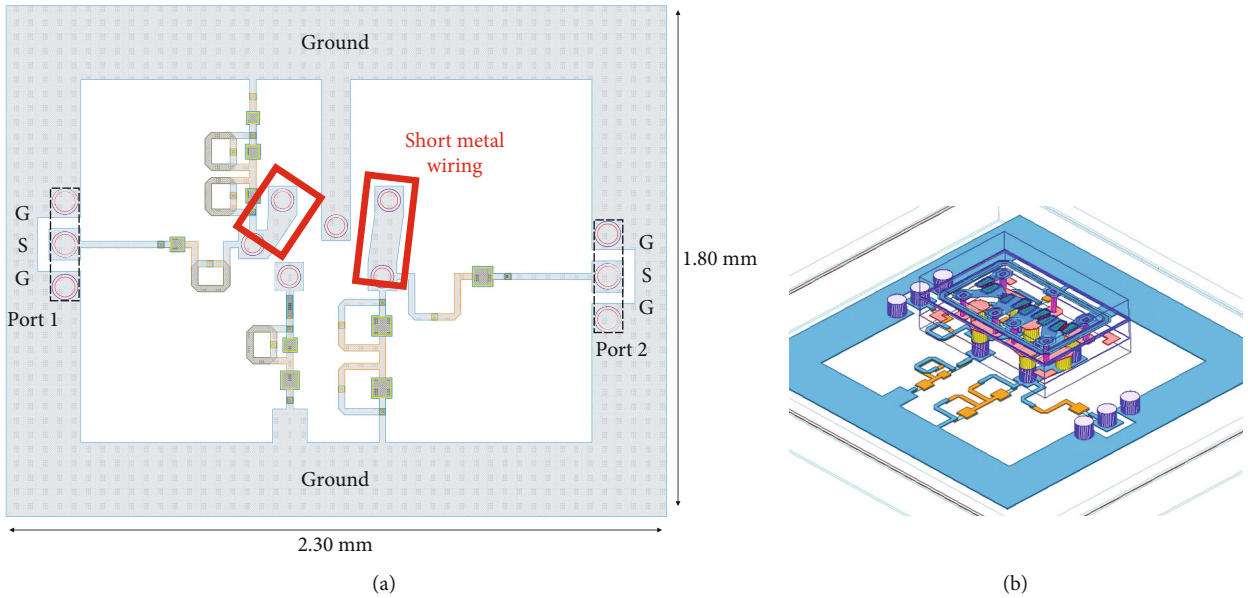


FIGURE 10: (a) The final designed IPD layout with GSG ports. (b) 3-D stereogram of the packaging renderings of chip A.

In this packaging method, the parasitic effects are suppressed by designing additional circuits and pads on the IPD chip. After packaging, the additional circuits on the IPD will make the redundant FBAR cells short-circuited. It can be seen from Figure 6(b) that the low-frequency suppression is worse than the ideal circuit simulation effect by about 20 dB; thus, a capacitor C_e is introduced in the NC_5 branch to generate additional TZ (f_{tz_extra}) in low frequency, as shown in Figure 8.

The IPD layout based on the optimized circuit with GSG ports and packaging model is shown in Figures 10(a) and 10(b). The enlarged view of the layout with physical dimensions and the acoustic-electric hybrid simulation *S*-parameters are shown in Figures 11(a) and 11(b). The 3-D modeling size after packaging is $2.30 \times 1.80 \times 0.56\,\text{mm}^3$. It can be seen that the in-band parasitic response is significantly suppressed, and the low-frequency suppression is greatly deepened by 36.75 dB due to the introduction of f_{tz_extra} (C_e = 1.16 pF).

3.2. Packaging with Extra Substrate (Chip B). It can be seen from Figure 11(b) that the optimized filtering effect is still

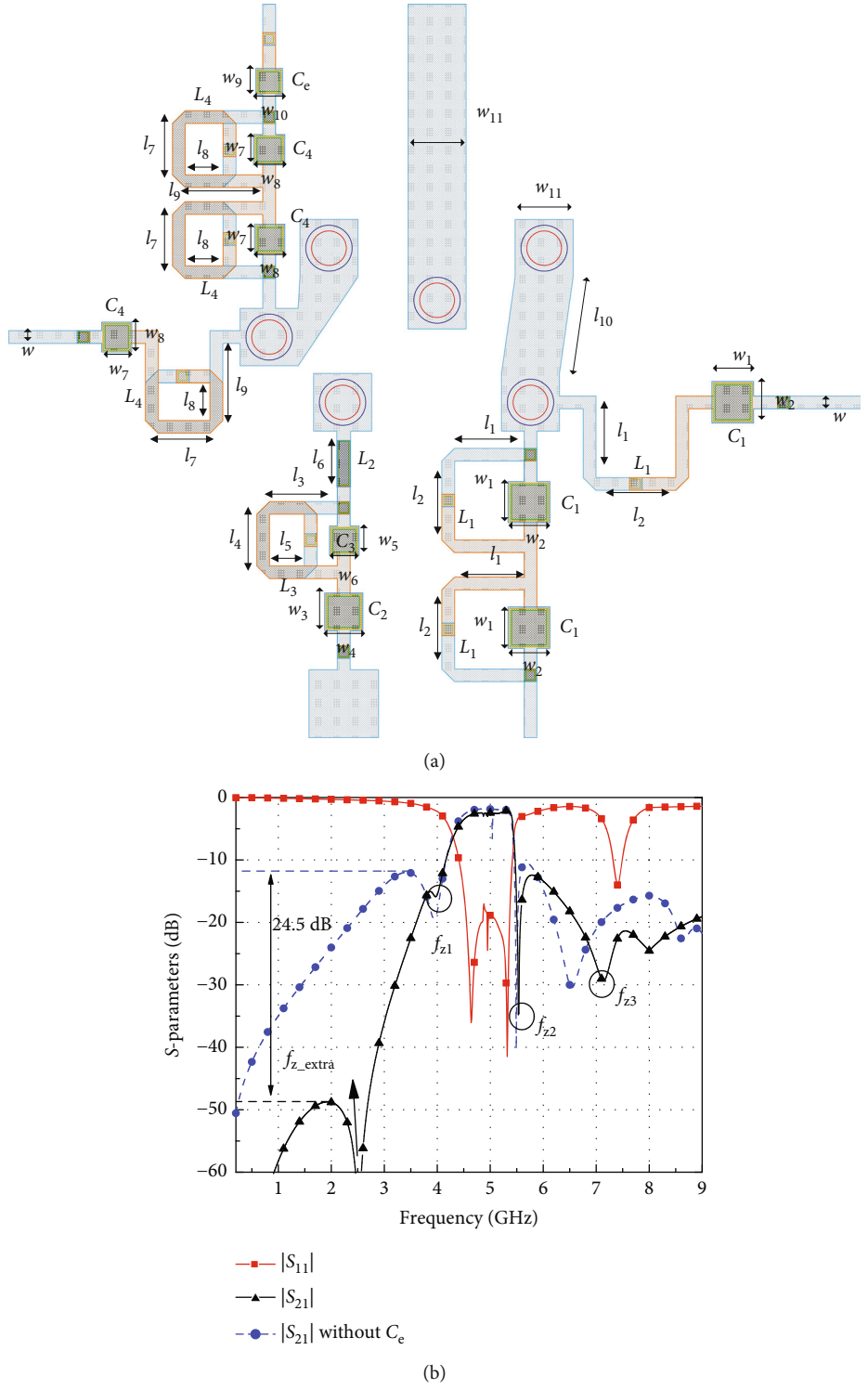


FIGURE 11: (a) The enlarged schematic diagram of circuit section with physical dimensions (units: μm) ($w = 22$, $w_1 = 72$, $w_2 = 72$, $w_3 = 66$, $w_4 = 66$, $w_5 = 51$, $w_6 = 51$, $w_7 = 52$, $w_8 = 52$, $w_9 = 46$, $w_{10} = 46$, $w_{11} = 100$, $l_1 = 142$, $l_2 = 137.8$, $l_3 = 117$, $l_4 = 90$, $l_5 = 60$, $l_6 = 81$, $l_7 = 89.55$, $l_8 = 65.5$, $l_9 = 133.85$, and $l_{10} = 169.6$). (b) The acoustic-electric hybrid simulation results of chip A.

not satisfactory, there is still a certain degree of parasitic response in the band and out-of-band high frequency, and the lower sideband selectivity is not sharp. This shows that although the dielectric layer of the IPD chip is prevented from being sandwiched between the metal layer of the IPD and the top electrode of the FBAR through flip-down packaging, the stacking of the two chips will still cause the filter to cause unavoidable parasitic responses.

To solve the above problems, keep the FC packaging method unchanged; the difference is that the IPD chip is

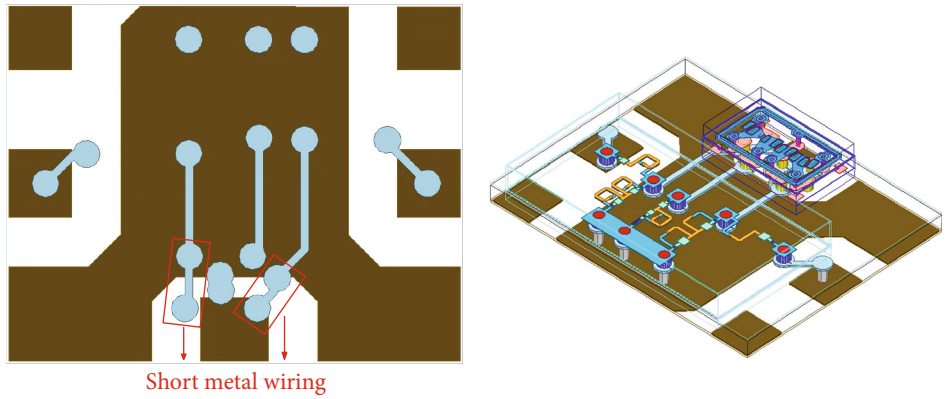


FIGURE 12: (a) The vertical view of the substrate. (b) 3-D stereogram of the packaging renderings of chip B.

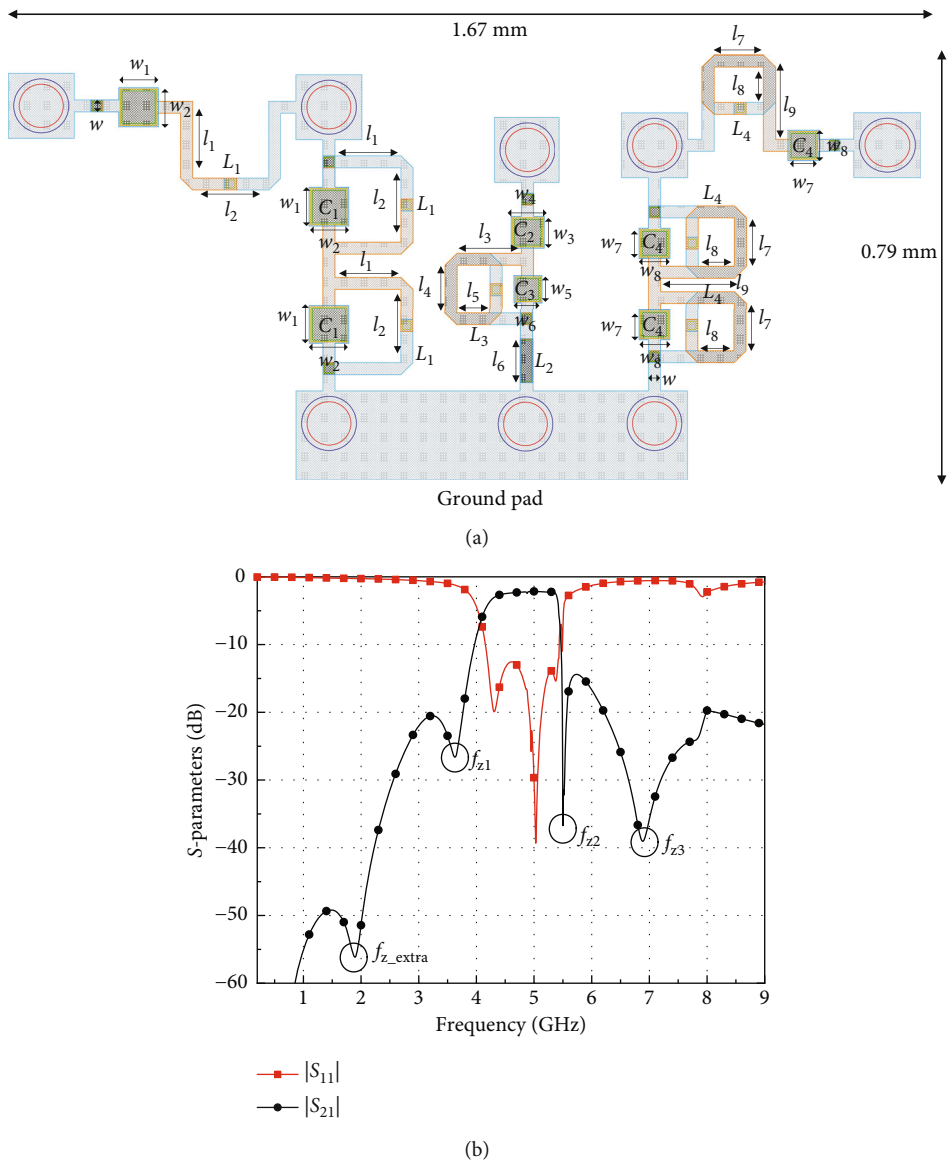


FIGURE 13: (a) The finally designed IPD layout without GSG ports and physical dimensions (units: μm) ($w = 22$, $w_1 = 72$, $w_2 = 72$, $w_3 = 60$, $w_4 = 60$, $w_5 = 51$, $w_6 = 51$, $w_7 = 56$, $w_8 = 56$, $w_9 = 46$, $l_1 = 142$, $l_2 = 137.8$, $l_3 = 117$, $l_4 = 90$, $l_5 = 60$, $l_6 = 81$, $l_7 = 89.55$, $l_8 = 65.5$, and $l_9 = 133.85$). (b) The acoustic-electric hybrid simulation results of chip B.

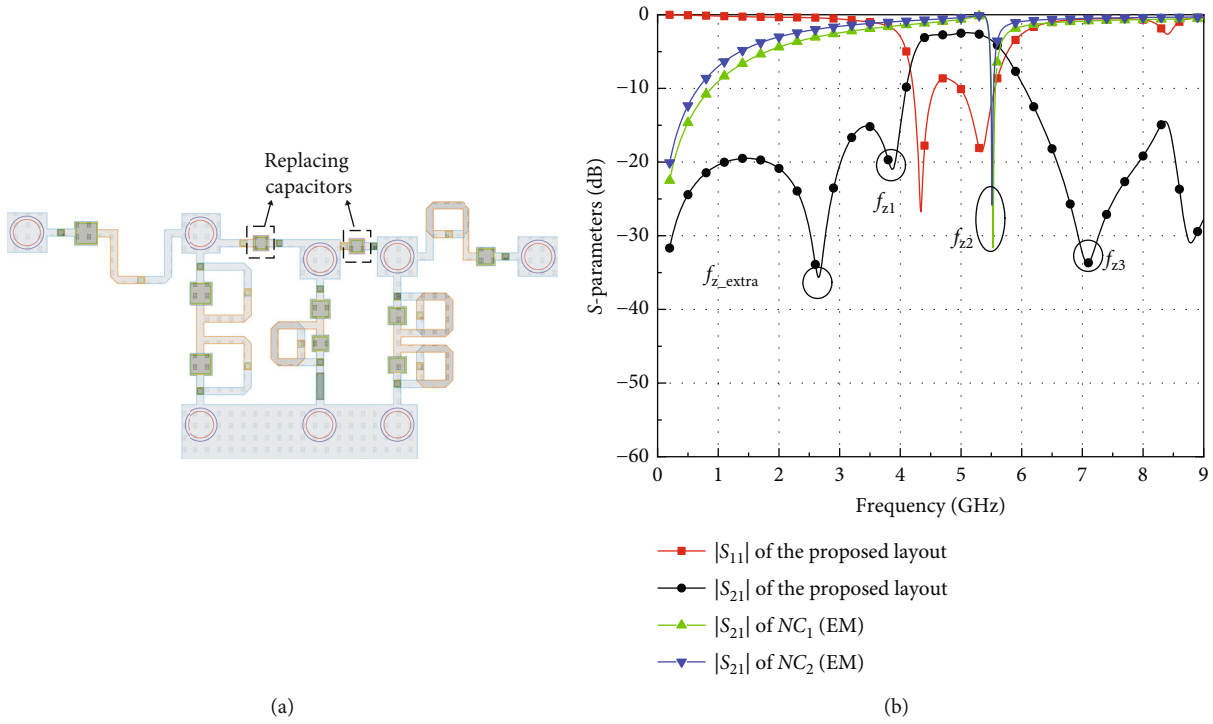


FIGURE 14: (a) The layout after replacing the FBARs with capacitors. (b) The EM simulation results of the layout, NC_1, and NC_2.

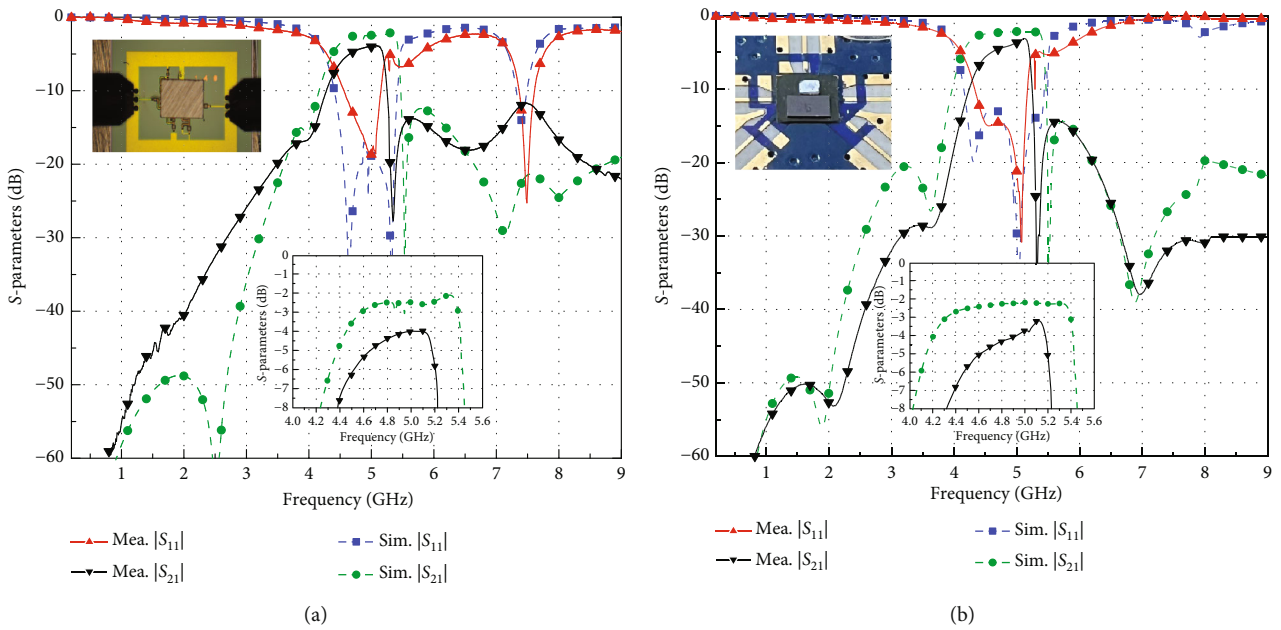


FIGURE 15: The simulated and measured results of (a) chip A and (b) chip B.

no longer seen as the substrate of the FBAR chip; instead, a separate substrate is used, and the layout of the IPD chip is redesigned by using the optimized circuit. Place the IPD chip and the FBAR chip upside down on the substrate side by side, and solder the corresponding pads together to avoid the parasitic response caused by the stacking between the chips. During this process, it should be noted that the sum of the widths of IPD chips and FBAR chips cannot be greater than the width of the substrate. Thus, the additional capacitor C_e is not introduced to control the width of the IPD chip. To suppress parasitic response, the metal wiring originally implemented based on IPD for short-circuiting redundant FBARs is now set on the substrate, as shown in Figures 12(a) and 12(b). The IPD layout of chip B with

Table 2: The performance comparison with previous works.

Refs.	f_0 (GHz)	FBW (%)	Size ($\lambda_g \times \lambda_g$)	Min.IL (dB)	SF[1]	Implementation
[1]	3.52	5.7	0.013×0.011	2.50	0.92*	FBARs
[5] B-2	3.58	53.8	0.028×0.016	1.67	0.77	IPD
[8]	2.02	28.8	0.240×0.450	1.05	0.88	SAW resonators and TLs
[9]	2.15	24.9	0.540×0.160	1.87	0.91	FBARs, TLs, and CLs
[11]	0.418	2.87e-4	0.007×0.018	4.30	N/A	SAW and SMD inductor
Chip A	4.88	13.7	0.037×0.029	3.86	0.67	FBARs and IPD
Chip B	4.83	15.8	0.038×0.030	3.07	0.68	FBARs, IPD, and substrate

*Estimated value. SF[1]: shape factor (3 dB bandwidth/10 dB bandwidth).

physical dimensions and the acoustic-electric hybrid simulation results are shown in Figures 13(a) and 13(b). The EM modeling size after packaging is $2.34 \times 1.84 \times 0.42\,\text{mm}^3$. In the case of almost the same size, the packaging method mentioned above brings extremely small in-band and high-frequency parasitic effects, obviously two low-frequency TZs, and three TPs, which have a high degree of agreement with the simulation of the ideal circuit. To sum up, this kind of hybrid filter design process is not one way from circuit to layout to the hybrid simulation. Even for the same circuit, using different packaging methods can result in significantly different simulation performances. Therefore, the recommended design process is as follows:

(1) Determine the desired operating frequency (f_0), bandwidths, return loss in the passband and the rejection in the stopband, and fit FBAR stacks based on the ideal model

(2) Design the ideal hybrid circuit, and choose the packaging method

(3) Design the layout based on IPD technology, build the packaging 3-D model of both chips, and do the acoustic-electric hybrid simulation

(4) Optimize the circuit based on the simulation results, redo the previous two steps, and realize the expected EM simulation result by iteration

It is worth noting that as shown in Figure 13(b), f_{z1} is generated by C_2; however, no resonator or lumped element can generate f_{z_extra}. As is well known, the stacking of FBARs is very similar to the sandwich structure of metal-insulator-metal (MIM) capacitors in the IPD technology, which leads to similar capacitance effects in FBARs. To identify the cause of f_{z_extra}, the impact of the capacitance performance of FBAR on the circuit will be separately considered. Specifically, NC_1 and NC_2 will be replaced with capacitances to eliminate the impact of the acoustic performance of FBAR networks, and a new layout will be designed for EM simulation, as shown in Figure 14(a). The EM simulation results are shown in Figure 14(b). It can be seen that f_{z_extra} still exists, yet f_{z2} which is produced by the FBAR networks disappears in the insertion loss of the proposed layout, which reveals that f_{z_extra} is produced by the capacitance effect of NC_1 and NC_2. The packaging stacking issue mentioned above and the metal ground of the outer ring on the IPD chip result in the absence of f_{z_extra} in the acoustic-electric hybrid simulation of chip A.

3.3. Fabrication and Measurement. To verify the feasibility of the proposed chips, the complete chip test system is used to measure the manufactured chip, which includes the probe station TS2000-SE and the vector network analyzer N5242B. The results of EM simulation and measurement are shown in Figures 15(a) and 15(b). First of all, the measured results of both chips hardly show a parasitic response, proving the effectiveness of the proposed method of using metal wiring to short-circuit redundant FBARs. It can be observed that the measured insert losses of both chips are higher than the simulated results. This is because the loss of the copper pillars is not considered in the simulation results. As shown in Figures 15(a) and 15(b), the FBWs of chip A and chip B are 13.7% (4.550-5.217 GHz) and 15.8% (4.451-5.213 GHz), respectively. The roll-off can be defined by

$$\text{roll-off} = \left| \frac{17\,\text{dB}}{\text{freq}_{3\,\text{dB\_IL}} - \text{freq}_{20\,\text{dB\_IL}}} \right|, \tag{21}$$

where $\text{freq}_{3\,\text{dB\_IL}}$ and $\text{freq}_{20\,\text{dB\_IL}}$ are the frequencies that correspond to the minimum insert loss attenuation of 3 dB and 20 dB. Thus, the upper roll-offs of chip A and chip B are calculated by (21) as 163.46 dB/GHz and 209.88 dB/GHz, respectively. The above data fully proves that these two chips successfully combine the high selectivity of FBAR technology and the large bandwidth characteristic of IPD technology. For chip A, the measured TZs are located at 3.986 and 5.349 GHz, and the minimum IL is 3.862 dB and located at 5.090 GHz.

The high-frequency suppression is better than 13.8 dB, with the low-frequency suppression better than 17.1 dB. For chip B, the measured TZs are located at 2.079, 3.633, and 5.321 GHz, and the minimum IL is 3.072 dB and located at 5.119 GHz. The return loss is better than 14.5 dB within the passband, with the high-frequency suppression better than 14.3 dB and the low-frequency suppression better than 28.5 dB. In comparison, the measured results of chip B are closer to the simulation results, which further indicates that using FC packaging on the substrate will result in a smaller parasitic response and more accurate simulation.

It can be observed that there is a certain frequency shift in the TZ provided by FBAR. This is because the FBAR chip has not been trimmed to the expected thickness, and the actual thickness of the PS layer is slightly greater than the simulation thickness, resulting in the resonance frequency of FBAR being lower than the simulation resonance frequency.

The research on filter chips is of great significance, verifying the research idea that FBAR and IPD technology can complement advantages. Finally, to highlight the advantages of this work, the comparison with other works is listed in Table 2. Although some references (e.g., Ref. [8] and Ref. [9]) also have the advantages of high selectivity and wide passband, none of them are of chip-scale size. To sum up, filter chips that combine the three advantages of large bandwidth, high selectivity, and chip-level size, like the proposed chips, are extremely rare.

4. Conclusion

In this paper, a novel hybrid BPF is proposed, packaged, and measured. Its measured FBW of 15.8% and roll-off of 209.88 dB/GHz show that the filter successfully combines the wideband advantage of LC filters and the high selectivity advantage of FBAR filters. For the redundant FBARs, a method of using metal wiring to short-circuit them is proposed to suppress parasitic effects, and the experimental results show that the method is effective. The reasons for the differences between testing and simulation are analyzed. Such performance is superior to traditional IPD filters and FBAR filters. The lumped component resonator implemented based on IPD technology ensures the small size of the final chip, verifying the idea of combining the two technologies mentioned above. The proposed design methods and theories are of great significance for the research of high-performance chips.

Data Availability

The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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