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Research Article

Optimally Matched 189-232 GHz 6.8 dBm Output Power CMOS Frequency Doubler

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This paper presents the design and measurements of a 215-252 GHz 40 nm bulk CMOS frequency doubler with a 6.8 dBm deliverable peak output power and a conversion gain of 11.8 dB. The designed chip is composed of a 28.5 dB gain 6-stages 110 GHz power amplifier, an optimized push-push doubler biased in class-C configuration, and an output impedance matching network. A numerical method had been applied here for designing each implemented matching network achieving the optimum matching while maintaining the minimum insertion loss as well. The presented design shows the highest output power among the other sub-THz-designed CMOS counterparts. The design occupies an area of 0.795 mm^2 and shows a total DC power dissipation of 262 mW and DC-RF efficiency of 1.87%.

1. Introduction

Recently, subterahertz (THz) technology has emerged paving the way for a wide range of applications in different fields, such as wireless communication, material analysis, and noninvasive imaging for both medical and security applications [1–3]. Signal sources with sufficient driving power capabilities are therefore required. Frequency multiplier chains, which resemble one of the most challenging modules in the design, are frequently employed for generating the THz signal. In this regard, a frequency doubler equipped with four ways power combiner had been developed in the 90 nm SiGe process and shown a saturation output power of 8 dBm at 215 GHz [4]. Frequency multipliers in the CMOS process had also shown a remarkable breakthrough. For instance, frequency doubler had been developed in the 65 nm CMOS process offering a 3 dBm peak output power at 200 GHz [5]. Furthermore, in 40 nm CMOS, a frequency multiplier chain design that is potentially offering 4.1 dBm at 225 GHz has been reported [6]. Recently, with the aid of phase shifters, a four-way phase compensated multiplier has been presented delivering a 3 dBm output power as measured at 260 GHz in the same latter technology [7].

By virtue of impedance matching and its significant influence on optimizing the efficiency, different studies had been presented investigating the matching considerations from different prospectives and for various applications [8, 9]. Yet, ideal behaviors of the matching network's elements, such as frequency independence or lossless characteristics, are still assumed under the conventional matching techniques. Such ideal characteristics, however, will not hold true as the frequency increases. Therefore, several research directions, such as matching-insertion loss tradeoffs or proper bandwidth, have been highlighted. In the literature, different studies have been made to consider the lossy response of the matching network's passives [10–13]. Recently, the optimum impedance transformation path had been analytically researched for millimeter wave (mmW) application to offer the impedance matching while minimizing the network insertion loss. Furthermore, the significance of load-pull simulation had been highlighted as well [14]. Due to the severe losses in passives at sub-THz band, with the inspiration of the latter work, the optimal matching network that

offers impedance matching with the reduced losses in passives will be adopted through this work for the chain interstage matching networks to boost the output power of the doubler chain.

Along with optimization of the matching networks, the multiplier efficiency as well as driver amplifier's driving capability has been enhanced through conscientious design, resulting in a further increase in the output power.

The arrangement of this paper is started by first highlighting the circuit design of each of the multiplier chain in section 2. Section 3 demonstrates in detail the measurement setup and explores the measurement results with a short analysis. Section 4 concludes the significant outcomes of the work presented in this paper.

2. Circuit Design

The technology is constrained from one perspective by the limitation of its NMOS transistors' maximum oscillation frequency (fmax) below 290 GHz. Moreover, the statistical variation that significantly takes place in this technology is adding another constraint making the design using this technology very challenging. The performance of the doubler, such as its output power and operating bandwidth, will therefore be greatly limited with 40 nm technology. The overall block diagram of the designed module as well as its micrograph image is shown in Figures 1(a) and 1(b). The driver amplifier (DA) is designed in a pseudo differential amplifier architecture and fed through an integrated 110 GHz rat-race balun. The frequency of the doubler, on the other hand, is implemented as a push-push class-C amplifier. To enable high deliverable output power from the doubler, the gate biasing voltage has been optimized while the load-pull simulation is being referred.

2.1. 110 GHz Balun and Driver Amplifier. The 6-stage DA, as shown in Figure 1, is designed and implemented in the front of the doubler to boost the power level of the 110 GHz input signal. The pseudo differential amplifier is adopted for this section to enable the usage of cross-coupled capacitor feedback to compensate the effects of the transistors' gate-drain capacitance promoting for a higher gain [15].

To employ the differential circuit configuration, a rat-race balun is implemented at the input to feed the amplifier. Figures 2(a) and 2(b) show the layout of the balun as well as the simulation analysis results. The balun is designed on the top thick copper metal layer for a reduced insertion loss. Simulation analysis has been conducted through the Virtuoso SpectreRF environment, and the simulation results have shown that the insertion losses S21 and S31 at 110 GHz are -4.4 dB and -4.8 dB, respectively, while the phase imbalance is less than ±3 degrees.

The first three stages of the DA are implemented using NMOS transistors of the size of 16 μm/40 nm. For the consequent following stages, however, the implemented configurations of the NMOS transistors are 32 μm/40 nm, 2×32 μm/40 nm, and 4×32 μm/40 nm, respectively.

The four NMOS transistor configurations are employed at the final stage to enhance the output power. At that stage, the input signal is applied to the gates of NMOS transistors through an equally divided signal path, whereas the drains are connected to the leading structure located at the centre of the structure. The sources are directly connected to the surrounding ground. It is worth noting that the matching networks in between all these stages will be designed following the same methodology that will be presented in section 2.3. The maximally efficient gain (G_{me}) is referred as the figure of merit useful for optimizing the design of power amplifier through this work [14, 16, 17] and expressed in terms of the NMOS pairs' Y-parameters by Eq. (1) as follows:

$$G_{me} = \frac{|Y_{21}|^2 - |Y_{12}|^2}{4\,\mathrm{Re}\,[Y_{11}]\,\mathrm{Re}\,[Y_{22}] - 2\,\mathrm{Re}\,[Y_{12}Y_{21}] - 2|Y_{12}|^2}. \quad (1)$$

According to the simulation results presented in Figure 3(a), the G_{me} is boosted by around 1 dB at 110 GHz by using a cross-coupling 8.7 fF feedback capacitor. Furthermore, the output power analysis is presented in Figure 3(b), and the amplifier obviously exhibits 28.5 dB simulated peak small-signal gain and saturation output power of 14 dBm. The flat response at higher input power levels is referred to the saturation of the amplifier.

2.2. 220 GHz Frequency Doubler. The simplified circuit diagram of the 220 GHz frequency doubler is illustrated in Figure 1(a). The nonlinearity of the NMOS transistors is basically employed for exciting the higher order harmonics. The push-push amplifier model is applied for implementing the frequency doubler section. The class-C biasing configuration is adopted for this section to enhance the second harmonic component, which will then be extracted through the output matching network. The simulated output power of the doubler versus gate bias is presented in Figure 4 showing an output power of 8.0 dBm at Vgs = 0 V. The load-pull simulation results at Vgs = 0 V are demonstrated as inset in the same figure. According to the presented simulation, the optimal output impedance of the doubler is found to be $5.6 + 4.2i\,\Omega$.

2.3. Impedance Matching Networks. Impedance matching networks are implemented at the output of each stage of the DA module as well as the output of the doubler module. These networks are configured as a π network, realized mainly from transmission lines (TLs) and metal-oxide-metal (MOM) capacitor elements. Along with impedance matching, the applied configuration will also serve as the DC biasing network for the NMOS transistors. At sub-THz band of spectrum, however, such passive components exhibit severe lossy response. Accordingly, the impedance matching section must be optimized in a diligent sense as such elements are to be included in the design. In this regard, the numerical model for the generalized optimization will be adopted through this work to realize the optimal impedance transformation path that offers the desired matching while maintaining the minimum insertion loss as well. On this subject, the per-length scalable equivalent model for the TL and MOM capacitor is first estimated. Integrand EMX 3D electromagnetic simulator is used to

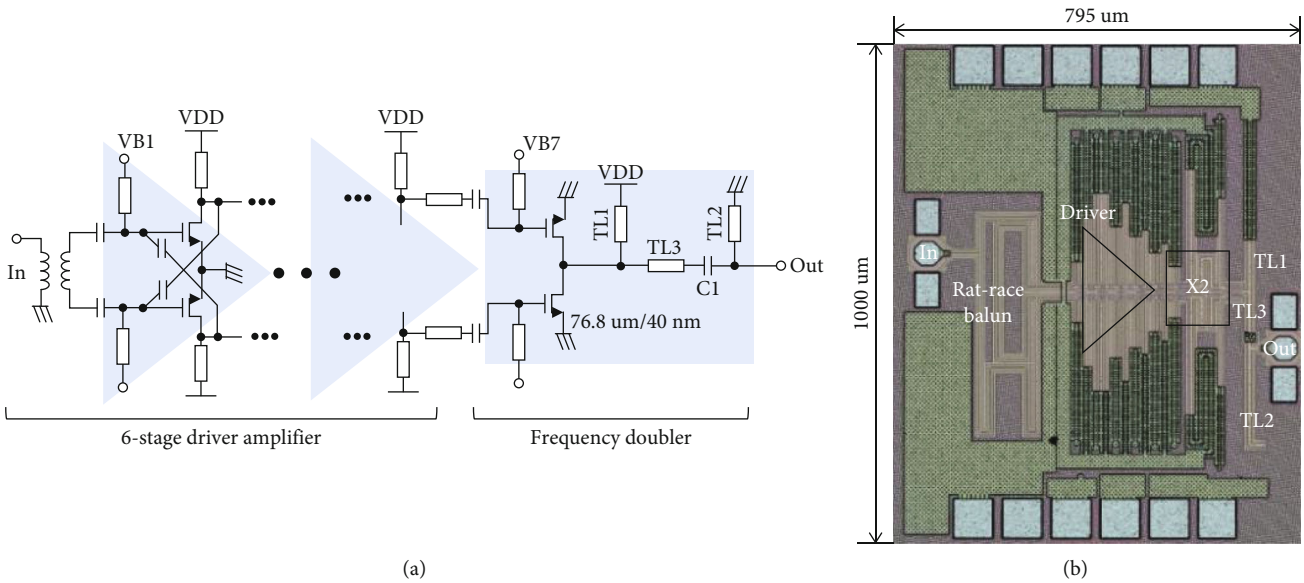

Figure 1: The designed model: (a) schematic diagram and (b) micro photograph.

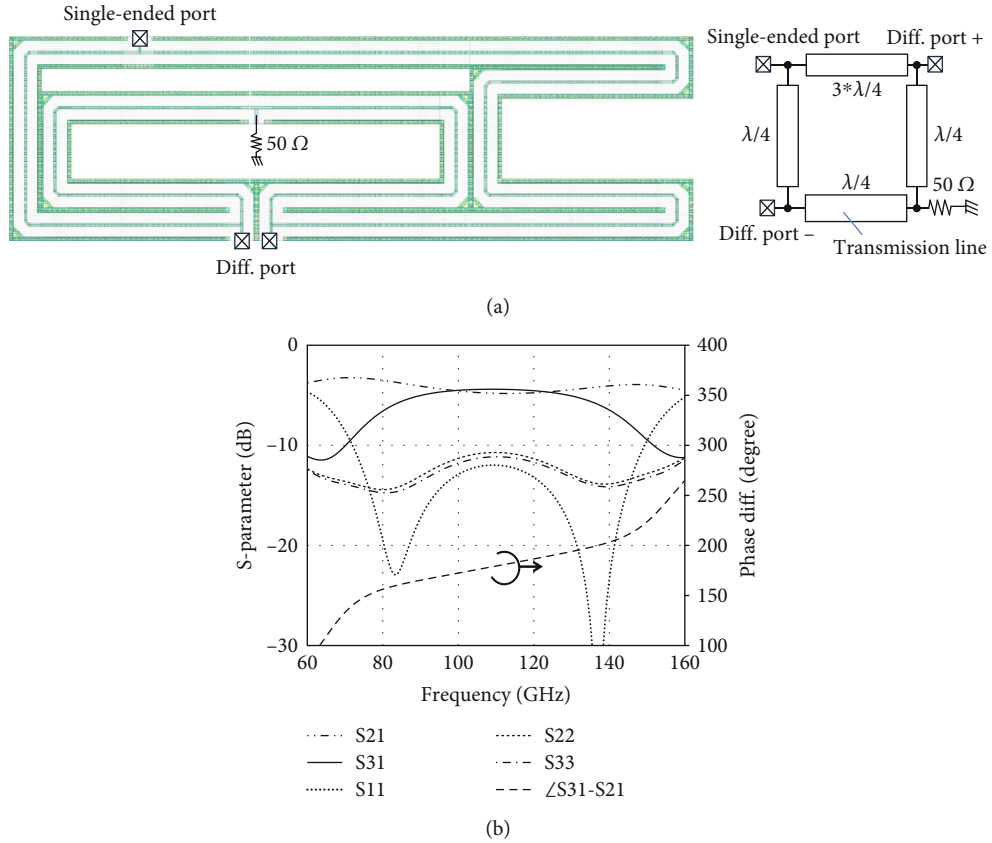

Figure 2: Folded rat-race balun: (a) schematic and layout and (b) simulated results.

extract the RLGC model for the implemented TL elements in this work. On the other hand, the equivalent π-model for the adopted square-shaped MOM capacitor is generated from the technology data provided by the foundry. The Y-parameters of the MOM capacitor (Y_{ij}), as illustrated in Figure 5, are then obtained for each matching network through a polynomial fitting and expressed as a 4th order polynomial function in terms of MOM side length, x, as follows:

$$Y_{ij} = \left(a_1 x^4 + \bullet\bullet\bullet + a_5\right). \tag{2}$$

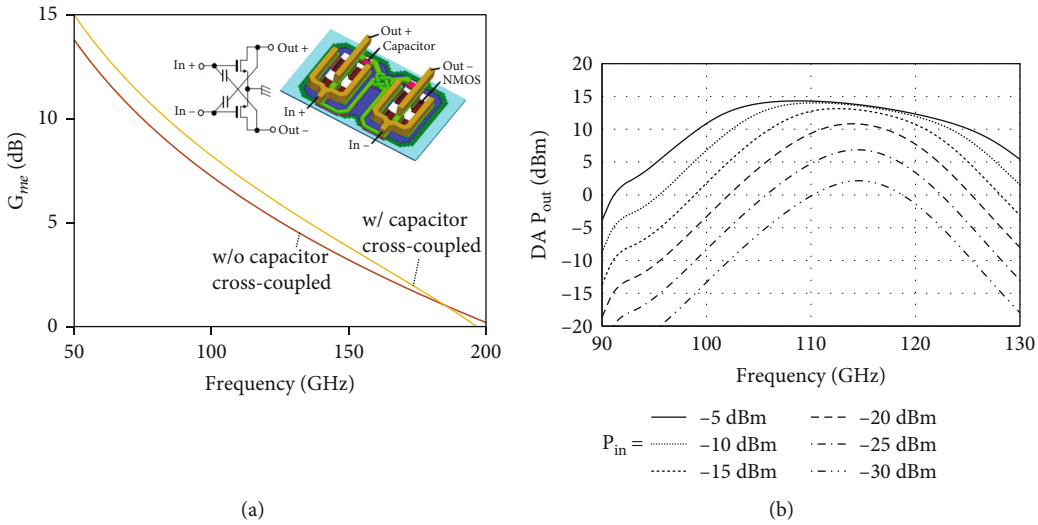

FIGURE 3: (a) Simulated G_{me} of NMOS (size: $4 \times 32\ \mu$m/40 nm) pairs and (b) simulated output power of DA with various input power levels.

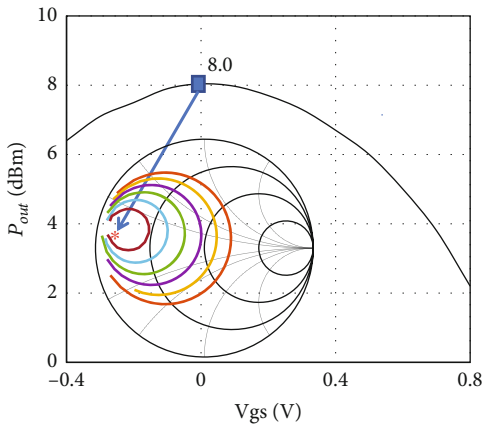

FIGURE 4: Simulated output power of the doubler versus gate bias at 220 GHz. Load-pull simulation at Vgs = 0 V is demonstrated in the inset.

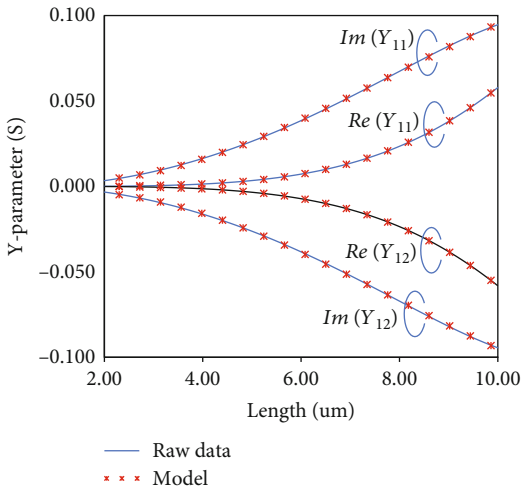

FIGURE 5: Y-parameter representation of the MOM capacitor model in terms of its length evaluated at 110 GHz.

The illustration of the matching network is shown in Figure 6. The overall ABCD matrix of the matching network can be calculated by cascading the ABCD matrix of each component, and consequently, the S-parameters (S_{ij}) and Y-parameters (Y_{ij}) of each matching network are then estimated. Accordingly, the input impedance of the nth matching network is then given by

$$Z_{in} = \frac{1}{Y_{in}} = \frac{1}{(Y_{11} - (Y_{21}Y_{12}/Y_L - Y_{22}))}. \tag{3}$$

Furthermore, the efficiency which is considered as another alternative representation for the insertion loss for each network is also evaluated as follows:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\mathrm{Re}\,(V_2 I_2^*)}{\mathrm{Re}\,(V_1 I_1^*)} = \frac{\mathrm{Re}\,\left(1/Y_L |Y_{21}/(1 + Y_{22}/Y_L)|^2\right)}{\mathrm{Re}\,(Y_{in})}, \tag{4}$$

where Y_{in} and Y_L are representing the admittances at the input and output, respectively.

A wide-range sweep analysis had been performed for numerous combinations of the TLs and MOM capacitors, and the closed-form equations had been applied to numerically calculate both impedance and efficiency for each network. The optimal networks that showed the lowest loss had been selected accordingly. Table 1 lists the various applied matching networks through this work, showing the electrical length of each TL and the resultant capacitance of the MOM. The matching networks were optimized individually. The resultant impedance as well as insertion loss corresponding to each network is also presented in Table 1.

3. Measurement Results

The presented frequency multiplier had been fabricated in the 40 nm CMOS process occupying an area of 0.795 mm^2.

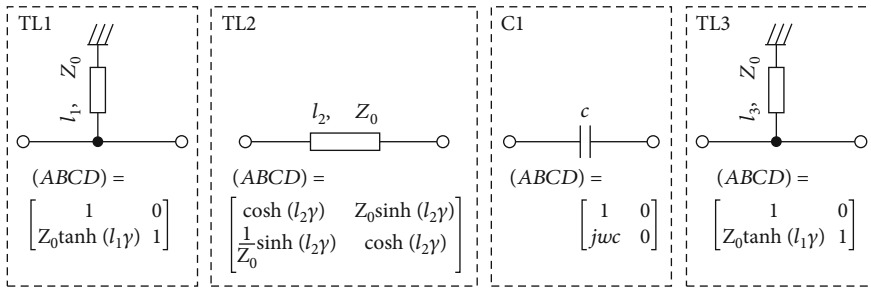

Figure 6: Matching network model and ABCD matrix equations of each element.

Table 1: Applied matching networks at different stages.

Match. net.	TL_1 (deg)	TL_2 (deg)	C_1 (fF)	TL_3 (deg)	Efficiency η (%)	Z_{in} (Ω)	Zload (Ω)
DA 1	37.0	11.9	190	50.1	47.9	$73 + 50i$	5.6-44.4i
DA 2	37.0	11.9	190	50.1	47.9	$73 + 50i$	5.5-45.1i
DA 3	44.9	11.9	45	27.0	51.3	$50.3 + 55.6i$	3.8-27.9i
DA 4	30.3	11.9	238	18.1	64.6	$23.2 + 9.5i$	2.6-14.3i
DA 5	23.1	11.9	330	10.7	64.6	$9.2 + 11.1i$	2.1-9.3i
DA 6	62.4	41.4	330	47.3	46.8	$5.8 + 9.0i$	2.7-17.2
Output	77.5	23.5	36	126.7	74.1	$5.6 + 4.2i$	50

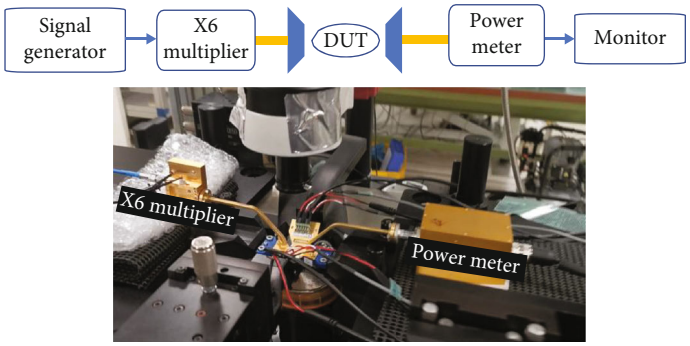

Figure 7: Illustration of the setup used for the power measurement.

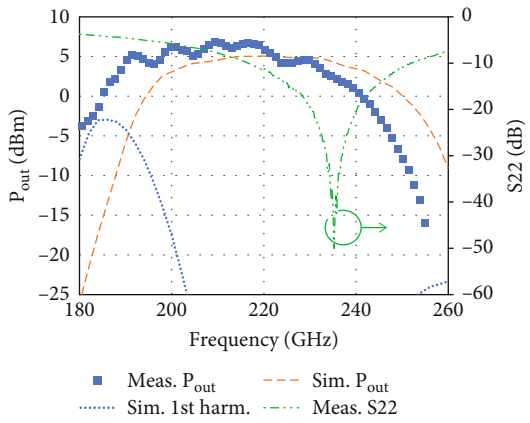

Figure 8: Measurement results for the output power and reflection loss. The simulated output power and fundamental leakage are also demonstrated.

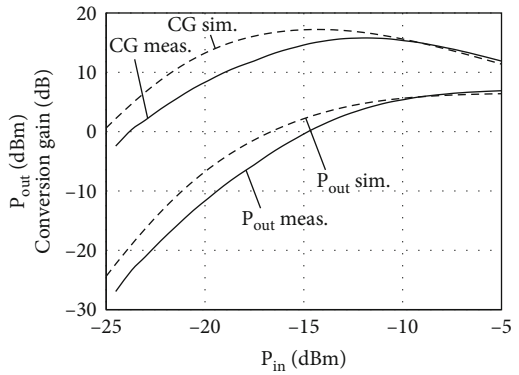

Figure 9: Output power and conversion gain versus input power (210 GHz).

The on-wafer measurements had been performed as shown in Figure 7. The input signal is applied from the Anritsu (6097A) signal generator followed by active frequency multiplier AFM6 90-140 +10 to feed the input port through the Cascade Infinity WR8 probe. The VDI Erickson PM5 power meter was used to measure the output power level through the proper waveguide probe. For the reflection loss measurement at the output port, the Keysight vector network analyzer (PNA) together with 220 to 330 GHz VDI mmW extender was used to measure the one port *S*-parameter at the output while only applying the DC bias.

The frequency of 220 GHz resides at the band transition boundary between WR3 and WR5 waveguide probes. Accordingly, the full output frequency response measurement had been divided into two measurement bands and

Table 2: Comparison with other reported designs in literature.

	Tech.	Freq. (GHz)	Mult.	DC-RF (%)	Ways	Conv. gain (dB)	P_{out} (dBm)	Area (mm^2)	P_{dc} (mW)
2016 [4]	90 nm SiGe	220-230	2	0.23	4	4.7	8	3.63	2700
2016 [5]	65 nm CMOS	160-310	2	2.85	1	3	3	0.71	70
2021 [6]	40 nm CMOS	213-233	9	1.39	1	4.1	4.1	1.7	185
2022 [7]	40 nm CMOS	249-266	6	—	4	NA	3	7.3	890
2011 [18]	130 nm SiGe	215-240	2	0.08	1	NA	-3	—	630
2016 [19]	130 nm SiGe	165-230	2	0.87	2	5.2	5.2	N.A	380
2018 [20]	130 nm SiGe	170-220	2	—	2	6.5	6.5	N.A	90
2018 [21]	80 nm InP	220-265	6	—	1	4	5	2	124.8
2019 [22]	130 nm SiGe	220-255	8	1.6	4	18	12	2.15	990
2020 [23]	130 nm SiGe	152-220	4	1.8	1	-1	-1	1.3	45
2022 [24]	130 nm SiGe	220-261	18	1.47	1	15	8	0.58	429
2022 [25]	65 nm CMOS	200-220	2	2.85	1	4.6	4.6	0.106	83
2022 [26]	28 nm CMOS	208-233	2	1.1	1	-7.2	-4.9	0.2	26.4
This work	40 nm CMOS	189-232	2	1.87	1	11.8	6.8	0.795	262

measured using two setup configurations, which employ either I325-T-GSG-75-BT WR3 or I220-T-GSG-75-BT WR5 Cascade probe. The agreement between both of these measurement setups at the transition boundary is taken as evidence on the accuracy of the conducted measurement.

Figure 8 demonstrates the measured output power level as well as the reflection loss at the output port S22 of the doubler. The leakage of the fundamental signal is also demonstrated as well. The output power versus input power as well as the conversion are both demonstrated in Figure 9.

The peak output power of 6.8 dBm had been measured at 210 GHz, while the measured conversion gain is 11.8 dB. The design had shown a 3 dB bandwidth of 43 GHz defined from 189 to 232 GHz. The DC dissipation of DA and the doubler are 216 mW and 46 mW, respectively. Accordingly, the overall DC-RF efficiency is 1.87% at 210 GHz. Table 2 highlights the chronological development through a brief performance comparison for some state-of-the-art frequency multipliers in contrast to the presented work. The output power of the presented frequency multiplier has shown the highest level among other CMOS frequency multipliers. In contrast to compound semiconductor counterparts, it shows comparable driving power capabilities while offering lower power consumption and compact design.

4. Conclusion

The optimally matched CMOS amplifier-doubler chain has been presented, which shows a peak output power of 6.8 dBm at 210 GHz, a conversion gain of 11.8 dB, and a 3 dB bandwidth of 43 GHz. The optimal matching technique, which optimizes the impedance transformation path to minimize the network insertion loss, has been adopted for all matching networks included in this work. The amplifier-doubler chain employs a low loss rat-race balun at the input, followed by a 6-stage DA that delivers 14 dBm output power. The whole chain consumes 262 mW of DC power, and the overall DC-RF efficiency is 1.87% at 210 GHz. The presented design is expected to be used in applications such as imaging, radar, air sensing, biomedicine, and ultra-high-data-rate wireless communications.

Data Availability

Research data are shared.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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