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*Research Article*

# Design of Ultrasmall Plasmonic Logic Gates Based on Single Nanoring Dielectric-Metal-Dielectric Waveguide

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This paper proposes a new configuration of dielectric-metal-dielectric (DMD) waveguides to design optical logic gates. Seven plasmonic logic gates, including NOT, OR, AND, NAND, NOR, XOR, and XNOR, are realized by one nanoring and four DMD plasmonic waveguides. To realize the logic gates, an ultrasmall size of 300 nm × 300 nm device is designed. The performance of the plasmonic logic gates is based on constructive and deconstructive interference between input and control ports. To evaluate the logic state of the output port, the threshold transmission limit is assumed to be 0.35. The transmission ratio, $T$, contrast ratio, CR, modulation depth, MD, insertion loss, IL, and contrast loss, CL, parameters measure the seven logic gates' performance. A maximum $T$ of 232% is obtained for AND, OR, and XNOR logic gates. Simulation results show that the dimensional parameters are optimized because of very high MD for all seven logic gates. Maximum values of CR and CL are obtained for the NOT gate. For the AND gate, a minimum IL value is achieved. The studied plasmonic logic gates can be employed in building blocks of all-optical signal-processing nanocircuits and nanophotonics devices. The finite element method (FEM) simulates the structure with COMSOL Multiphysics 5.4 software.

## 1. Introduction

The surface plasmon polaritons (SPPs) are the waves that propagate on metal-dielectric interfaces due to interactions between electromagnetic waves in dielectric and free electrons in metal. The ability to manufacture the low loss devices with dimensions less than 100 nm and confining the light beyond the diffraction limit lead to the design of all-optical SPP structures [1]. Control of the constructive and destructive interferences between light signals in plasmonic waveguides is the basic idea for designing plasmonic devices [2–5]. In recent years, many passive and active SPP devices such as switches [6, 7], logic gates [5, 8–18], sensors [19, 20], nanowires [21–23], splitters [24], filters [25, 26], couplers [27], resonators [28, 29], and multi- and demultiplexers have been designed [30–33]. In design of plasmonic logic gates, DMD [14, 34–36] and metal-dielectric-metal (MDM) plasmonic waveguides are mostly used [37–44]. DMD plasmonic waveguides offer advantages such as longer propagation length, reduced propagation loss, higher quality factor, improved figure of merit, ease of fabrication, and lower coupling loss [5]. In this way, a NOT plasmonic logic gate based on two nanoring DMD resonators with the size of 350 nm × 350 nm has been designed [34]. The transmission threshold limit has been assumed to be 0.5, and a maximum transmission value of 72% has been obtained. Five optical plasmonic logic gates, consisting of OR, NOR, AND, NAND, and NOT, have been realized by two DMD nanoring resonators [35]. The size of the structure is 200 nm × 400 nm. The transmission threshold value of 0.3 has been considered, and a maximum transmission value of 152% at the resonant wavelength of 1550 nm has been reported. The performance of the plasmonic gates is evaluated by $T$ and CR parameters. DMD square-shaped cavities have been utilized for the design of NOT, OR, AND, NOT-OR, NAND, XOR, and XNOR optical logic gates [36]. The structure with the size of 400 nm × 400 nm has been proposed. The $T$, CR, MD, and IL parameters are used for evaluating the gate's performance.

Transmission threshold has been assumed to be 0.3, and the transmission peak of 202% at the wavelength of 1310 nm has been obtained. Seven plasmonic logic gates, including NOT, OR, AND, NOT-OR, NAND, XOR, and XNOR, have been designed based on DMD waveguides and four ring resonators [14]. The transmission and extinction ratio (ER) parameters have been used for evaluating the gate's performance. The size of the structure is 400 nm × 380 nm, and the transmission threshold limit has been assumed to be 0.25. The maximum values of $T$ have been obtained as 239% and 187% at the wavelengths of 900 nm and 1330 nm, respectively.

In this article, seven plasmonic logic gates, including NOT, OR, AND, NOR, NAND, XOR, and XNOR, are designed. The ultrasmall structure with an area of 300 nm × 300 nm based on DMD plasmonic waveguides and single ring resonator is proposed. The threshold transmission value is 0.35 in order to evaluate the output logic state. $T$, CR, MD, IL, and CL parameters measure all seven logic gates' performance. The maximum value of $T$ is 232% for AND, OR, and XNOR logic gates at the resonant wavelength of 1310 nm. The simulation results are obtained by the FEM using COMSOL Multiphasic software. This research is considered fundamental for achieving an all-optical computer in the future.

## 2. Structure Layout and the Theoretical Model

A two-dimensional view of the symmetrically designed optical plasmonic gates with an area of 300 nm × 300 nm is indicated in Figure 1. Symmetrical design supports strong absorption and scattering of light leading to enhance electromagnetic fields near the metal surface [45]. The metal region is assumed to be silver with the dispersive relative permittivity characterized by Johnson and Christy's data [46]. The dielectric region is flint glass with a refractive index of 1.8 [47, 48]. The structural parameters are the height and width of the structure, $H$, the length of the side stripes, $L_s$, the length of the middle stripe, $L_m$, the nanoring outer radius, $b$, the nanoring inner radius, $a$, the width of the strips, $w$, and the distance between the stripes and nanoring, $d$. The dimensional parameters are listed in Table 1. In the studied structure, two ports are considered input ports; the two other ports are assumed to be output and control ports. The input ports are excited by a transverse magnetic (TM) polarized plane wave with electromagnetic filed components of $E_x$, $E_Y$, and $H_z$, as shown in Figure 1. The equation describing the dispersion relation for the TM mode in the waveguide is as follows [5]:

$$\varepsilon_m k_d + \varepsilon_d k_m \tanh\left(\frac{k_m}{2} w\right) = 0, \tag{1}$$

where $\varepsilon_d$, $\varepsilon_m$, and $w$ are the dielectric constant of the insulator, the dielectric constant of the metal, and the thickness of the thin metal layer, respectively. The dielectric wave number, $k_d$, and the metal wave number, $k_m$, are linked to the propagation constant of $\beta$ as follows:

$$\begin{aligned} k_d &= \left(\beta^2 + \varepsilon_d k_o^2\right)^{1/2}, \\ k_m &= \left(\beta^2 + \varepsilon_m k_o^2\right)^{1/2}, \end{aligned} \tag{2}$$

where $k_0$ is the free space wave number and is calculated as follows:

$$k_o = \frac{2\pi}{\lambda}. \tag{3}$$

The effective refractive index of the waveguide for SPPs waves is obtained as follows:

$$n_{\text{eff}} = \frac{\beta}{k_o}. \tag{4}$$

The Maxwell equations have been numerically solved using the two-dimensional FEM (2-D FEM) with the utilization of a convolutional perfectly matched layer (CPML) as the absorbing boundary condition within the simulated area.

The parameters of $T$, CR, MD, IL, and CL evaluate the optical gate's performance. $T$ is obtained by outgoing optical power, Pout, and the incoming optical power, Pin, as follows [14]:

$$\text{T} = \left(\frac{P\text{out}}{P\text{in}}\right). \tag{5}$$

The output state of the desired logic gates is determined by the threshold limit value. In our proposed structure, the threshold value is assumed to be 0.35. Therefore, the output state will be logic one or ON when the transmission ratio is greater than the threshold limit. If the transmission ratio is smaller than the threshold limit, the output state is interpreted as logic 0 or OFF.

The CR is defined as follows [49]:

$$\text{CR}(\text{dB}) = 10\log\left(\frac{P\text{out} \mid \text{ON}_{\min}}{P\text{out} \mid \text{OFF}_{\max}}\right), \tag{6}$$

where $P\text{out} \mid \text{ON}_{\min}$ is the minimum output power of the output port for a logic state of 1 and $P\text{out} \mid \text{OFF}_{\max}$ is the maximum output power of the output port for a logic state of 0.

The relationship between the maximum transmission in the ON state, Max $T_{\text{ON}}$, and the minimum transmission in the OFF state, Min $T_{\text{OFF}}$, is described by the MD parameter obtained as follows [40]:

$$\text{MD} = \left(\frac{\text{Max}\, T_{ON} - \text{Min}\, T_{OFF}}{\text{Max}\, T_{ON}}\right). \tag{7}$$

Another parameter is IL defined as the loss in signal power from the input port to the minimum transmission of the output port in the case of the ON state. The IL is calculated as follows [50]:

$$\text{IL}(\text{dB}) = -10\log\left(\frac{P\text{out} \mid \text{ON}_{\min}}{P\text{in}}\right). \tag{8}$$

The description of the IL values in dB is given in Table 2.

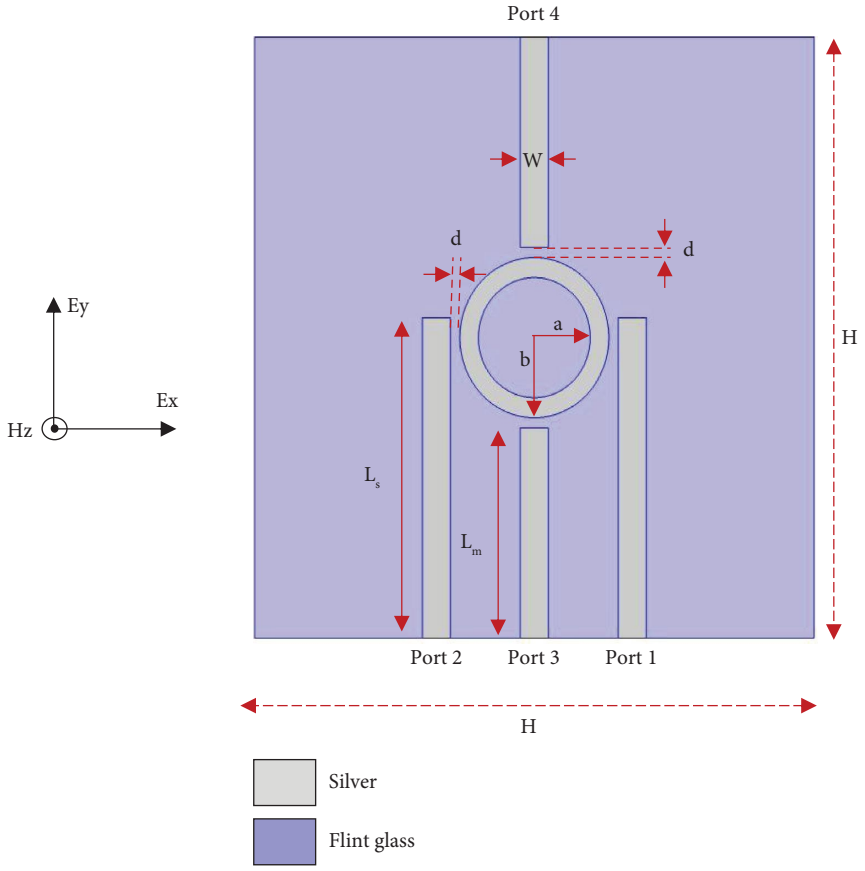



Figure 1: The suggested plasmonic all-optical logic gates with the area of 300 nm × 300 nm.

Table 1: The dimensional parameters of the proposed structure.

| Structural parameter | Description | Value (nm) |
|---|---|---|
| $H$ | Height and width of the structure | 300 |
| $L_s$ | Length of the side stripes | 160 |
| $L_m$ | Length of the middle stripes | 105 |
| $b$ | Nanoring outer radius | 40 |
| $a$ | Nanoring inner radius | 30 |
| $W$ | Width of the stripes | 15 |
| $d$ | Distance between the stripes and resonator | 5 |

Table 2: The description of the IL values in dB.

| IL (dB) ranges | Description | Assessment of IL |
|---|---|---|
| More than 5 | Very high | Bad and inefficient |
| More than 3–5 | High | Acceptable |
| More than 1–3 | Medium | Moderate |
| More than 0-1 | Low | Good |
| More than −1-0 | Very low | Very good and efficient |
| −1 and less | Ultralow | Excellent and efficient |

The new parameter is CL, which measures the losses due to the CR; when the CR is high and IL is low, the induced losses are low and vice versa. The CL is defined as follows [50]:

$$\mathrm{CL}(\mathrm{d}B) = \mathrm{CR}(\mathrm{d}B) - \mathrm{IL}(\mathrm{d}B). \quad (9)$$

Explanation of the values for the CL parameter is given in Table 3.

The structure performance is based on constructive and destructive interferences between the control signal and the input signal(s). The destructive and constructive interferences between the control signal and the input(s)

Table 3: Explanation of the CL values.

| CL (dB) ranges | Description | Assessment of CL |
|---|---|---|
| Negative value | Ultralow | Bad and inefficient |
| Less than or equal 4 | Very low | Acceptable |
| More than 4–8 | Low | Moderate |
| More than 8–12 | Medium | Good |
| More than 12–16 | High | Very good and efficient |
| More than 16–20 | Very high | Excellent and efficient |
| More than 20 dB | Ultrahigh | Excellent and optimum |

depend on the position of the control and the input ports and the phase of the incident signal when the dimensions of the structure, materials, size, and shape are fixed. When the incident waves at the input ports and the selector port have the same phase and direction of propagation, constructive interference occurs. In the case of the phase or direction of the propagation of the incident wave at the input ports and selector ports are different, the destructive interference happens.

Destructive and constructive interference between incident signals is described by the following equation [14]:

$$m = \frac{4n_{\text{eff}}d\cos\theta}{\lambda}, \tag{10}$$

where $m$ is the interference order as a positive integer greater than zero. $n_{\text{eff}}$, $\theta$, and $\lambda$ are the effective refractive index of the silver material, the phase of the incident wave, and the incident wavelength, respectively.

## 3. Parameters Validation

This section provides a detailed explanation of the approach utilized to determine the parameter dimensions of the proposed structure, as depicted in Figure 1, which operates at the wavelength of 1310 nm. The geometrical parameters of $W$, $L_s$, $L_m$, $a$, and $d$ are considered.

For optimal performance in the suggested structure, as illustrated in Figure 2, it is recommended to configure the $W$ parameter at 15 nm. This specific width value guarantees resonance at the desired wavelength and maximizes the transmission efficiency.

Furthermore, within the suggested framework, optimal transmission at the wavelength of 1310 nm is achieved by adjusting the $L_s$ to a value of 160 nm, as illustrated in Figure 3. It is worth mentioning that when the side stripes are extended beyond a length of 160 nm, there is an observed displacement of the resonance wavelength towards the longer wavelength. Conversely, a reduction in the length of the side stripes below 160 nm leads to a displacement of the resonance wavelength towards the shorter wavelength.

As depicted in Figure 4, the transmission values remain consistent across all three options for the length of the middle stripes in the proposed structure. Specifically, the Lm is set at 105 nm, which leads to a 5 nm separation distance (d) between all stripes and the resonator, simplifying the structure.

In contrast, the proposed structure exhibits its highest transmission at the 1310 nm wavelength when the inner radius of the nanoring is set to 30 nm, as depicted in Figure 5. However, if the length of the side stripes is extended beyond 30 nm, it causes a shift towards longer wavelengths in the resonance. Conversely, decreasing the length of the side stripes below 30 nm causes a shift towards shorter wavelengths in the resonance. Upon establishing the optimal values for the parameters ($a$) and ($d$), it can be inferred that the most favorable choice for the outer radius of $b$ is 40 nm. Consequently, for this investigation's proposed structure, the selected dimensions of $W$, $L_s$, $L_m$, $a$, $b$, and $d$ are set at 15, 160, 105, 30, 40, and 5 nm, respectively.

## 4. Design of Optical Gates

The performance of seven plasmonic logic gates, including NOT, OR, AND, NOR, NAND, XOR, and XNOR gates, is determined by choosing input, output, and control ports. The studied wavelength range for the input and control ports is 1000–1800 nm.

*4.1. Plasmonic NOT Logic Gate.* A schematic of the NOT gate circuit symbol with the truth table is shown in Figure 6. For the NOT gate performance, ports 1 and 2 are considered as the control ports and ports 3 and 4 are input and output ports, respectively. According to the truth table, if the input port is OFF, logic 0, the output port will be ON, logic 1. When the input port state is ON, the output port state is OFF.

The transmission spectrum for the NOT gate is indicated in Figure 7. In the case of the control, ports 1 and 2 are excited by an incident light of wavelength 1310 nm with a phase angle of 180° and 45°, respectively, and when the input port state is ON, destructive interference occurs between the input signal and the two control signals. At the wavelength of 1310 nm, the transmission value is 0.056, less than the transmission threshold of 0.35. Therefore, the state of the output port is OFF.

Constructive interference occurs if the state of the input port is OFF and the state of the control ports is ON with a phase shift of 0°. The transmission value is 1.55 and greater than the transmission threshold of 0.35 at the wavelength of 1310 nm. In this case, the output port is ON.

The $z$ component of the magnetic field distribution, Hz, while the input port state is ON and OFF is shown in Figures 8(a) and 8(b), respectively.

The simulation results of the NOT logic gate are summarized in Table 4.

According to the results, the CR of the NOT logic gate is high, 15 dB; therefore, the gate's performance is very good and efficient [49]. The gate is designed with optimum dimensions because of the very high MD of 96.77% [40]. According to Table 2, an ultralow IL value of −1.9 dB is obtained. Also, a CL value of 16.9 dB is achieved, which means that the NOT gate CL parameter is excellent and efficient, as provided in Table 3 [50].

*4.2. Plasmonic OR Logic Gate.* The conventional circuit symbol of the OR logic gate and the truth table are indicated in Figures 9(a) and 9(b), respectively. The output logic is 1 if

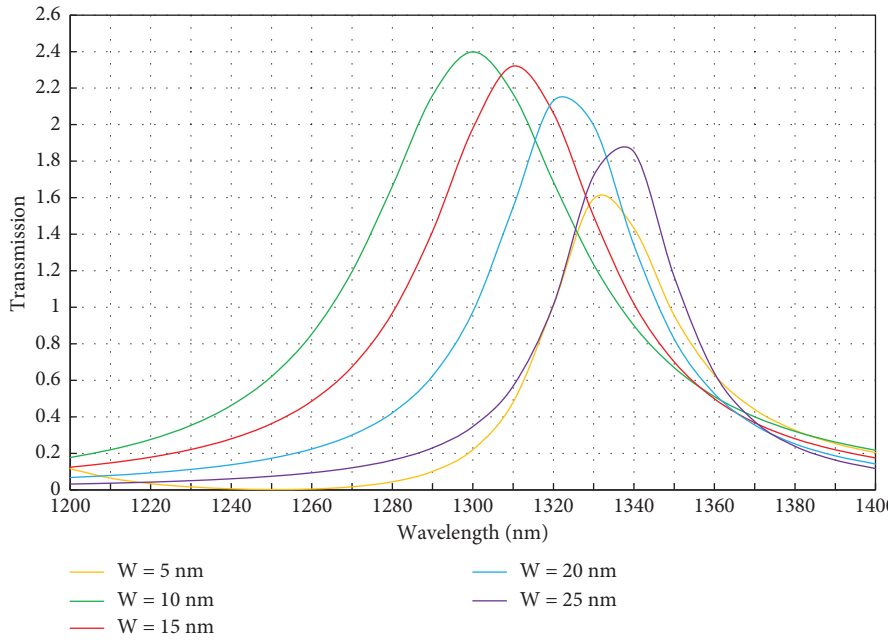



Figure 2: Validating of the $W$ parameter.

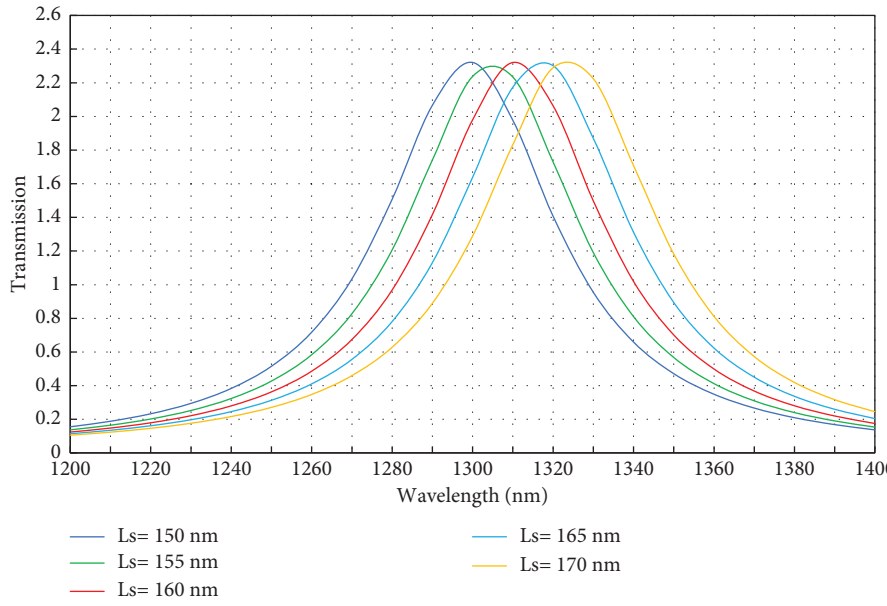



Figure 3: Validating the length of the side stripes ($L_s$).

both inputs or one of the inputs is ON. When both inputs are OFF, the output state is OFF.

In the proposed structure, ports 1 and 2 are input ports as input 1 and input 2, respectively. The port 3 and 4 are the control port and the output port, respectively. The transmission spectrum of the OR plasmonic gate is shown in Figure 10.

When the input ports are OFF and the control port is ON with the phase of 0°, the output is OFF. As shown in Figure 10, for the transmission spectrum, the transmission is 0.07, less than the transmission threshold of 0.35. Therefore, the output port state is logic 0. In the case of one of the input ports being ON and there is no phase difference between the ON input port and control port, constructive interference occurs. Therefore, the transmission reaches 0.81 and the state of the output port is ON. As shown in Figure 10, when both input ports are ON, the transmission peak is 2.32. Because there is no phase difference between input ports and control ports, constructive interference between the input and control ports occurs and the greatest transmission value of 2.32 is obtained.

The $z$ component of the magnetic field distribution, Hz, when the input ports are OFF and ON is shown in Figures 11(a) and 11(b), respectively.

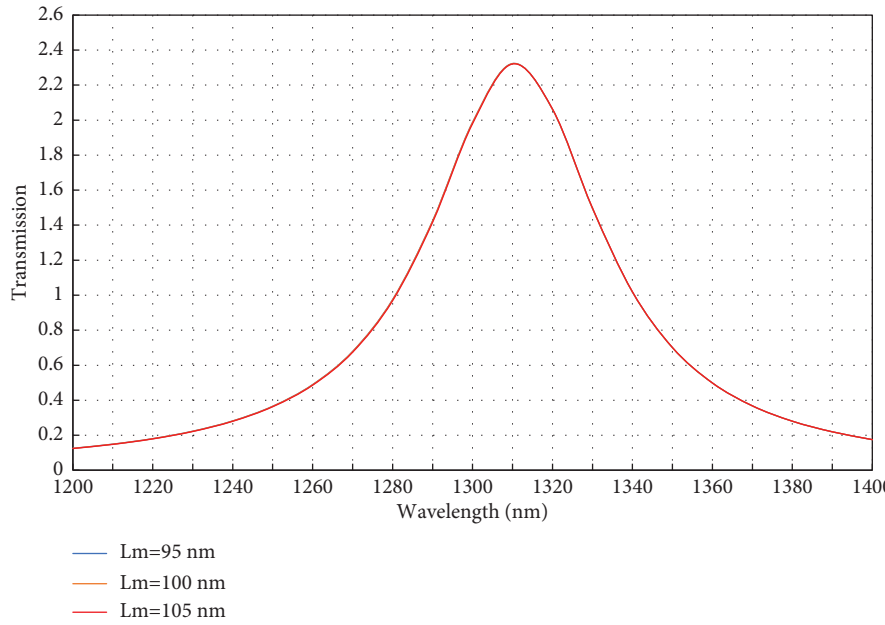



Figure 4: Validating the length of the middle stripes ($L_m$).

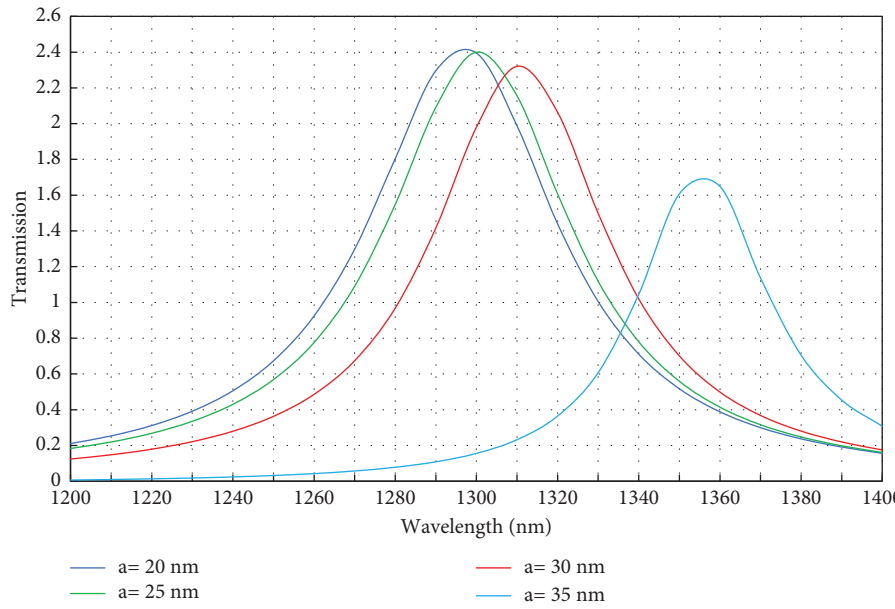
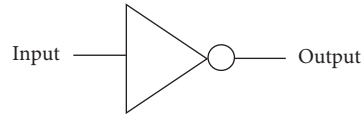



Figure 5: Validating of the nanoring inner radius ($a$).




(a)

| Truth Table | |
|---|---|
| Input Port 3 | Output Port 4 |
| 0 | 1 |
| 1 | 0 |

(b)

Figure 6: (a) NOT logic gate's conventional symbol and (b) the truth table. The ports 3 and 4 are considered as input and output ports, respectively.

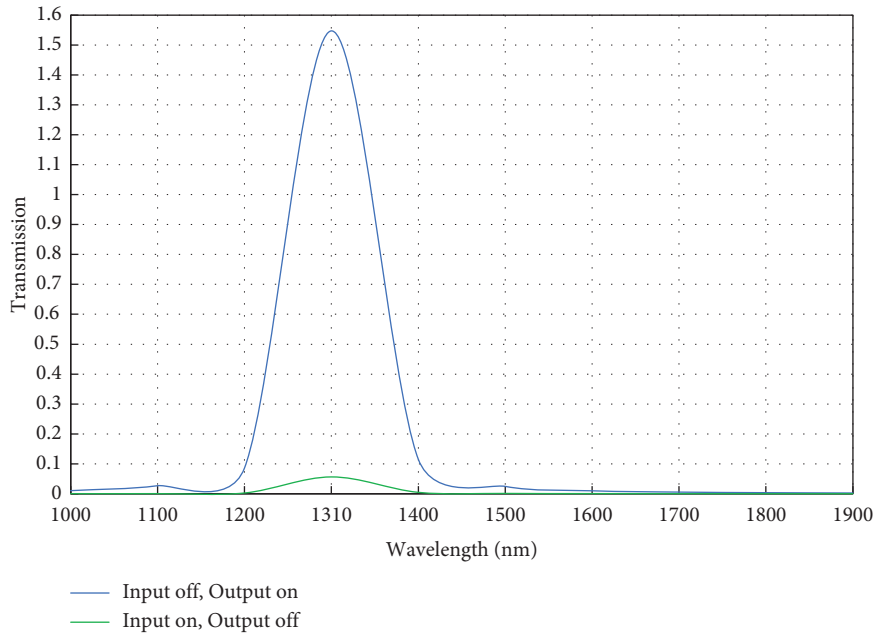



Figure 7: The transmission spectrum for the NOT gate.

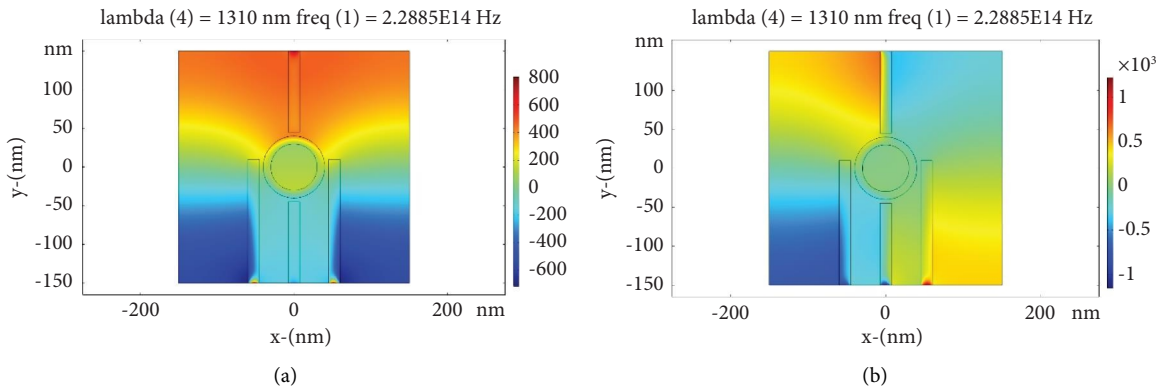
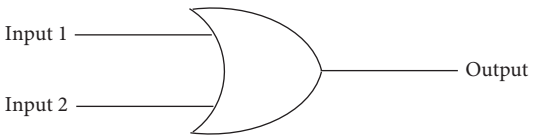



Figure 8: The $z$ component of the magnetic field distribution, Hz, while the input port is (a) ON and (b) OFF.

Table 4: Summarized simulation results for the NOT gate.

| Input (port 3) | Control 1 (port 1) | Control 2 (port 2) | Output (port 4) | Transmission threshold | $T$ | CR (dB) | MD (%) | IL (dB) | CL (dB) |
|---|---|---|---|---|---|---|---|---|---|
| OFF | ON (180°) | ON (180°) | ON | 0.35 | 1.55 | 15 | 96.77 | −1.9 | 16.9 |
| ON (0°) | ON (180°) | ON (45°) | OFF | | 0.05 | | | | |




(a)

| Truth Table | | |
|---|---|---|
| Input 1 Port 1 | Input 2 Port 2 | Output Port 4 |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

(b)

Figure 9: (a) OR logic gate's conventional symbol and (b) the truth table. The ports 1 and 2 are considered as input ports. The ports 3 and 4 are assumed to be control and output ports, respectively.

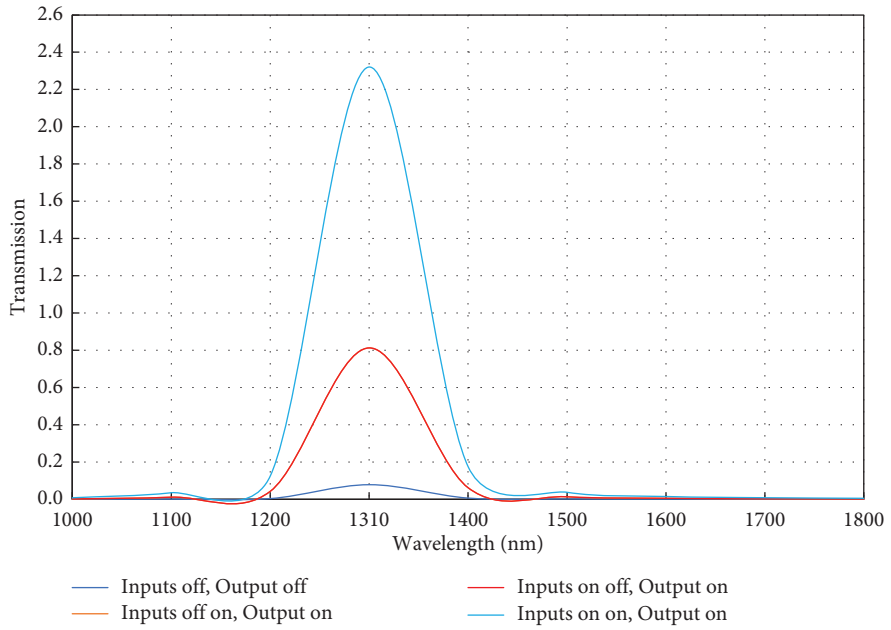



Figure 10: The transmission spectrum for the OR gate.

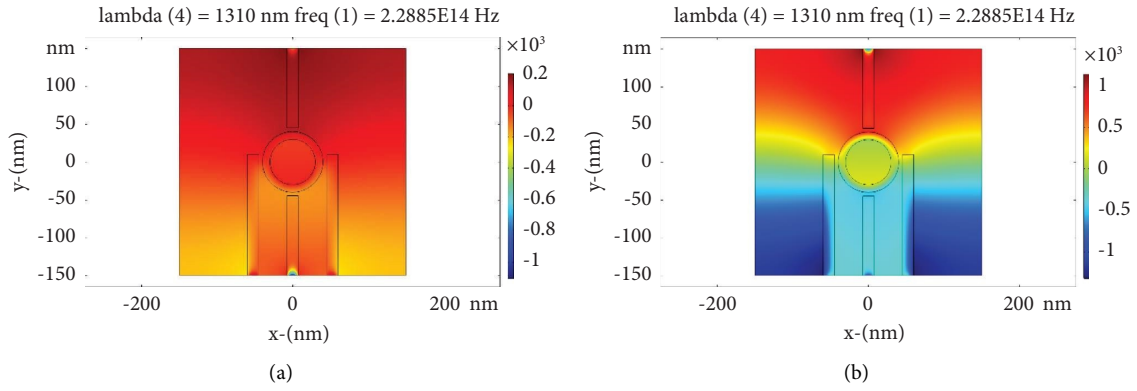



Figure 11: The field distributions of Hz inside the proposed structure related to the input ports of (a) OFF and (b) ON.

The simulation results of the OR logic gate are provided in Table 5.

For the plasmonic OR logic gate, the CR is medium. Therefore, the gate performance is good and efficient [49]. The MD of 96.95% shows an excellent design with optimal dimensions [40]. Low IL is obtained for the optical gate. According to Table 3, good CL is achieved [50].

*4.3. Plasmonic AND Logic Gate.* The AND logic gate circuit symbol and the truth table are shown in Figures 12(a) and 12(b), respectively. Ports 1 and 2 are used as input ports to design the gate. Ports 3 and 4 are assumed to be control and output ports, respectively.

The transmission spectrum of the AND logic gate is shown in Figure 13. Constructive interference happens when there is no phase difference between the input and control signals. According to the transmission spectrum, if the input ports and control port with the same phase shift of 180° is ON, the transmission is 2.32, logic 1 at the wavelength of 1310 nm.

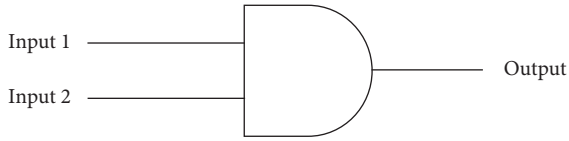
Deconstructive interference occurs because of a phase difference between the input and control signals. Therefore, the output port state is logic 0. For the second and third cases given in the truth table, the ON input port with the phase of 45° and the control port phase of 180° are considered. As shown in Figure 13, the peak of the transmission is 0.11, equivalent to logic 0. In the case of both input ports being OFF and the phase of the control port being 180°, the transmission peak is 0.078, equivalent to logic 0.

In the case of the input ports being OFF and ON, the $z$ component of the magnetic field distribution, Hz, is shown in Figures 14(a) and 14(b), respectively.

For the AND plasmonic gate, the simulation results are listed in Table 6.

Table 5: Summarized simulation results of Figure 9.

| Input 1 (port 1) | Input 2 (port 2) | Control (port 3) | Output (port 4) | Transmission threshold | $T$ | CR (dB) | MD (%) | IL (dB) | CL (dB) |
|---|---|---|---|---|---|---|---|---|---|
| OFF | OFF | ON (0°) | OFF | 0.35 | 0.07 | 10.6 | 96.95 | 0.9 | 9.7 |
| OFF | ON (0°) | ON (0°) | ON | | 0.81 | | | | |
| ON (0°) | OFF | ON (0°) | ON | | 0.81 | | | | |
| ON (0°) | ON (0°) | ON (0°) | ON | | 2.32 | | | | |




(a)

Truth Table

| Input 1 Port 1 | Input 2 Port 2 | Output Port 4 |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

(b)

Figure 12: (a) AND logic gate circuit symbol and (b) the truth table. The ports 1 and 2 are considered as input ports. The ports 3 and 4 are assumed to be control and output ports, respectively.

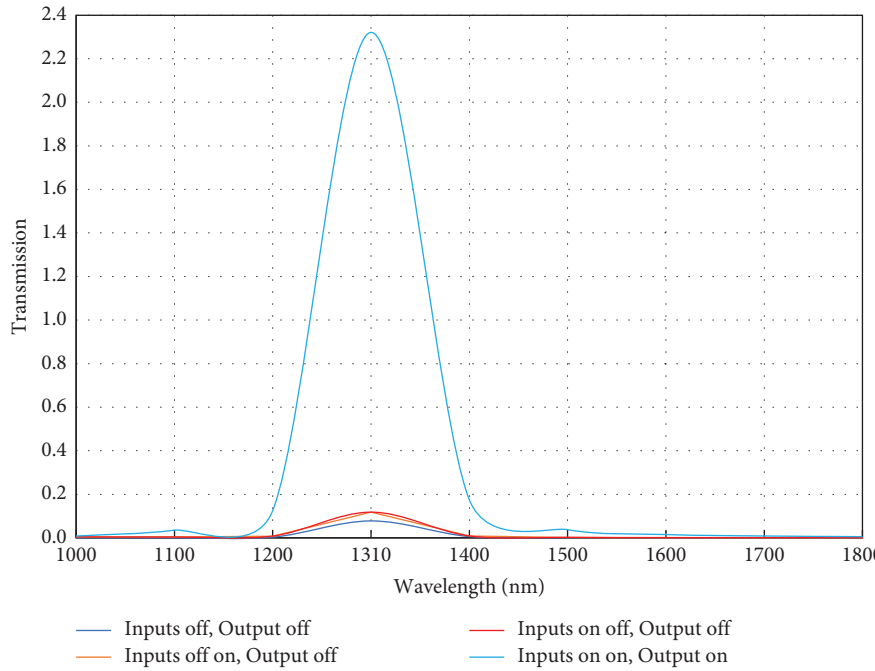



Figure 13: The transmission spectrum for the AND gate.

The CR of this logic gate is high; the gate is interpreted as a very good and efficient gate [49]. Excellent design with optimum dimensions is realized because of very high MD [40]. The ultralow IL results in an excellent and efficient CL value [50].

*4.4. Plasmonic NOR Logic Gate.* A schematic of the NOR gate circuit symbol with the truth table is shown in Figure 15. In this gate, ports 2 and 3 are assumed to be the input ports. The ports 1 and 4 are the control and output ports, respectively. For this gate, the control port is assumed to be ON with a phase shift of 180°. The transmission spectrum of the gate is shown in Figure 16.

As shown in Figure 16, when the input ports are OFF, the transmission peak is greater than the transmission threshold and the output state is ON. The peak of transmission is 0.39. In other cases, deconstructive interference occurs between the control and the input signals. If only one of the input ports is ON with the phase of 0°, the transmission value is

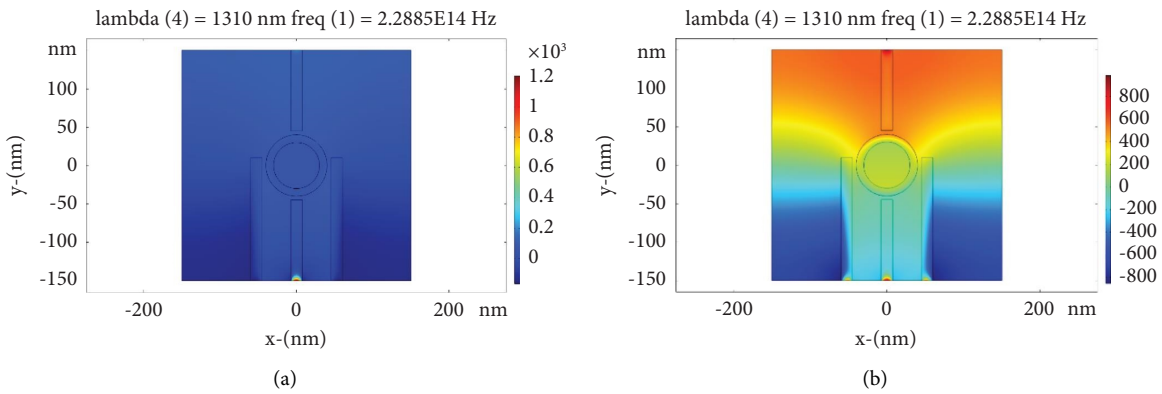
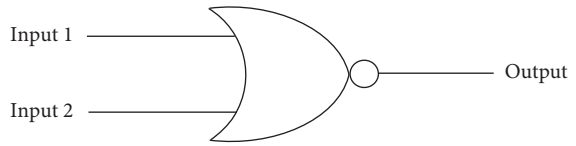



Figure 14: The Hz field patterns of the AND gate for the input ports of (a) OFF and (b) ON.

Table 6: The simulation results of the AND plasmonic gate.

| Input 1 (port 1) | Input 2 (port 2) | Control (port 3) | Output (port 4) | Transmission threshold | $T$ | CR (dB) | MD (%) | IL (dB) | CL (dB) |
|---|---|---|---|---|---|---|---|---|---|
| OFF | OFF | ON (180°) | OFF | 0.35 | 0.078 | 13.2 | 96.63 | −3.65 | 16.85 |
| OFF | ON (45°) | ON (180°) | OFF | | 0.11 | | | | |
| ON (45°) | OFF | ON (180°) | OFF | | 0.11 | | | | |
| ON (180°) | ON (180°) | ON (180°) | ON | | 2.32 | | | | |




(a)

| Truth Table | | |
|---|---|---|
| Input 1 Port 2 | Input 2 Port 3 | Output Port 4 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

(b)

Figure 15: (a) NOR logic gate circuit symbol and (b) the truth table. The ports 2 and 3 are considered as input ports. The ports 1 and 4 are assumed to be the control and output ports, respectively.

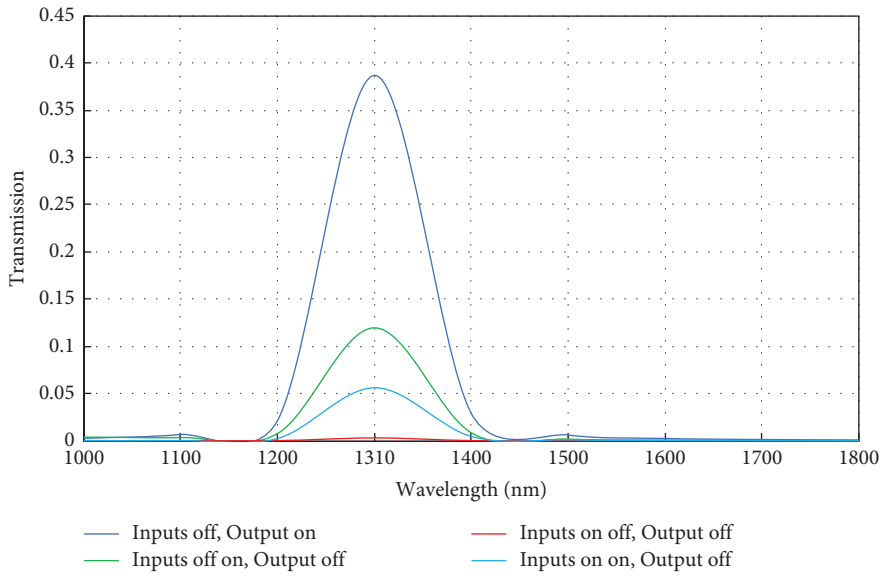



Figure 16: The transmission spectrum for the NOR logic gate.

less than the threshold transmission value due to the phase difference between the ON input port and the control port. At 1310 nm wavelength, the transmission values for cases 2 and 3 are 0.11 and 0.003, respectively. In the case of the input ports being ON, the port 2 with the phase of 45° and the port 3 with the phase of 0° are considered. The peak of the transmission is 0.05. Deconstructive interference occurs because of the phase difference between the ON input ports and the control port.

The $z$ component of the magnetic field distribution, Hz, when the input ports are OFF and ON, is shown in Figures 17(a) and 17(b), respectively.

The simulation results of the NOR logic gate are listed in Table 7.

This logic gate has a medium CR [49]. Therefore, the performance of this gate is moderate. An excellent design with optimum dimensions is done due to very high MD of 99.23 [40]. According to Tables 2 and 3, the IL and CL values are acceptable.

*4.5. Plasmonic NAND Logic Gate.* The conventional symbol of the NAND logic gate and the truth table are shown in Figures 18(a) and 18(b), respectively. To design the gate, the ports 2 and 3 are input ports. Port 1 and port 4 are assumed to be the control port and the output port, respectively. The control port is assumed to be ON with the phase of 0°.

The transmission spectrum of the designed gate is shown in Figure 19. In the case of both input ports being OFF and the control port being ON with the phase of 0°, there is only one effective light source and no interference occurs. Therefore, the output port will be in the ON state and the transmission peak is 0.39 at the wavelength of 1310 nm. When only one of the input ports is ON with the phase of 0°, constructive interference occurs between the signals of the input and control ports. As shown in Figure 19, the peak of the transmission is greater than the threshold limit and the output state becomes ON. If port 1 is ON and port 4 is OFF, the peak of the transmission is 0.81. When port 1 is OFF and port 4 is ON, the transmission peak is 1.54.

When the state of the input ports is ON with a difference phase, port 1 with the phase of 180° and port 4 with the phase of 90°, destructive interference occurs and the state of the output port is OFF. In this case, the transmission peak is 0.07.

Figures 20(a) and 20(b) show the $z$ component of the magnetic field distribution, Hz, when the input ports are OFF and ON, respectively.

The simulation results of the NAND logic gate are summarized in Table 8.

According to Table 8, the CR of this logic gate is medium. Therefore, its performance is moderate [49]. The MD is very high, and an excellent design with the best dimensions is carried out [40]. According to Tables 2 and 3, the IL and contrast loss values are acceptable [50].

*4.6. Plasmonic XOR Logic Gate.* A schematic of the XOR gate circuit symbol with the truth table is shown in Figure 21. For the XOR gate performance, ports 1 and 2 are considered as the input ports and ports 3 and 4 are the control and output ports, respectively. The control port is assumed to be ON with the phase of 0°.

The transmission spectrum of this plasmonic logic gate is illustrated in Figure 22. According to Figure 22, if the input ports are OFF, no interference occurs. The transmission peak is 0.07, and the output state is OFF. When only one of the input ports is ON, constructive interference occurs between the input and control signals and the transmission peak is 0.81. Therefore, the output state is ON. If port 1 is ON with a phase of 180° and port 2 is ON with a phase of 45°, destructive interference occurs because of the phase difference between the input and control signals. In this case, the transmission peak is 0.05 and the state of the output port is OFF.

Figures 23(a) and 23(b) show the $z$ component of the magnetic field distribution, Hz, when the input ports are OFF and ON, respectively.

The simulation results of the XOR logic gate are listed in Table 9.

For this plasmonic logic gate, the CR is medium. Therefore, the gate performance is good and efficient [49]. The MD is very high, so the gate design and dimensions are optimized [40]. The IL is low, according to Table 2. As given in Table 3, the CL is good [50].

*4.7. Plasmonic XNOR Logic Gate.* The conventional symbol of the XNOR logic gate and the truth table are shown in Figures 24(a) and 24(b), respectively. In order to design the gate, ports 2 and 3 are used as input ports. Ports 1 and 4 are assumed to be the control port and output port, respectively. The control port is assumed to be ON with a phase of 180°.

The transmission spectrum of the designed gate is shown in Figure 25. When the input ports are OFF, the applied light at the control port is sufficient to make the transmission peak, 0.39, greater than the threshold limit and the output port is ON. In the case of only one of the input ports being ON with the phase of 45°, destructive interference occurs between the input port signal and the control port. Therefore, the state of the output port is OFF. The transmission peak is given in Table 10. The constructive interference

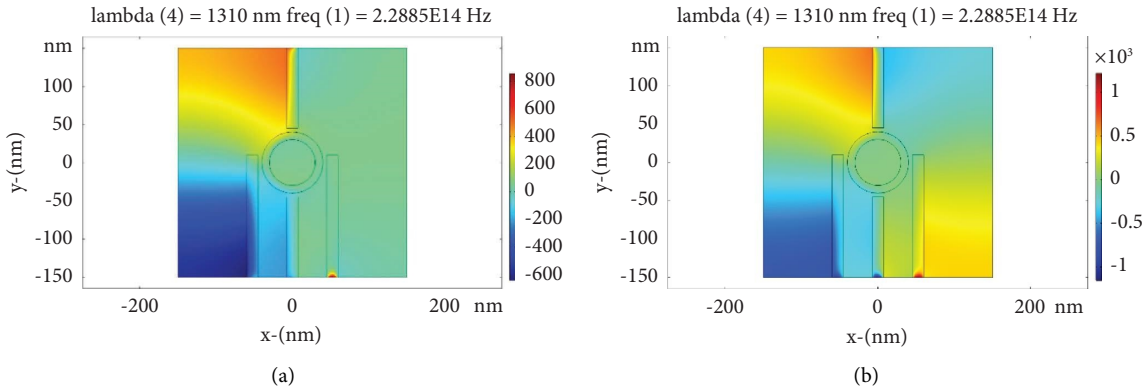
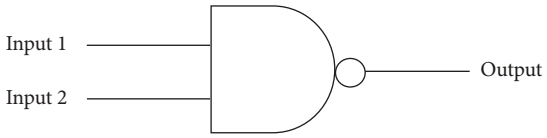



Figure 17: Field profiles of Hz inside the device when the input ports are (a) OFF and (b) ON.

Table 7: Summarized simulation results for the NOR logic gate.

| Input 1 (port 2) | Input 2 (port 3) | Control (port 1) | Output (port 4) | Transmission threshold | $T$ | CR (dB) | MD (%) | IL (dB) | CL (dB) |
|---|---|---|---|---|---|---|---|---|---|
| OFF | OFF | ON (180°) | ON | 0.35 | 0.39 | 5.5 | 99.23 | 4.09 | 1.41 |
| OFF | ON (0°) | ON (180°) | OFF | | 0.11 | | | | |
| ON (0°) | OFF | ON (180°) | OFF | | 0.003 | | | | |
| ON (45°) | ON (0°) | ON (180°) | OFF | | 0.05 | | | | |




(a)

| Truth Table | | |
|---|---|---|
| Input 1 Port 2 | Input 2 Port 3 | Output Port 4 |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

(b)

Figure 18: (a) NAND logic gate circuit symbol and (b) the truth table. The ports 2 and 3 are considered as input ports. The ports 1 and 4 are assumed to be control and output ports, respectively.

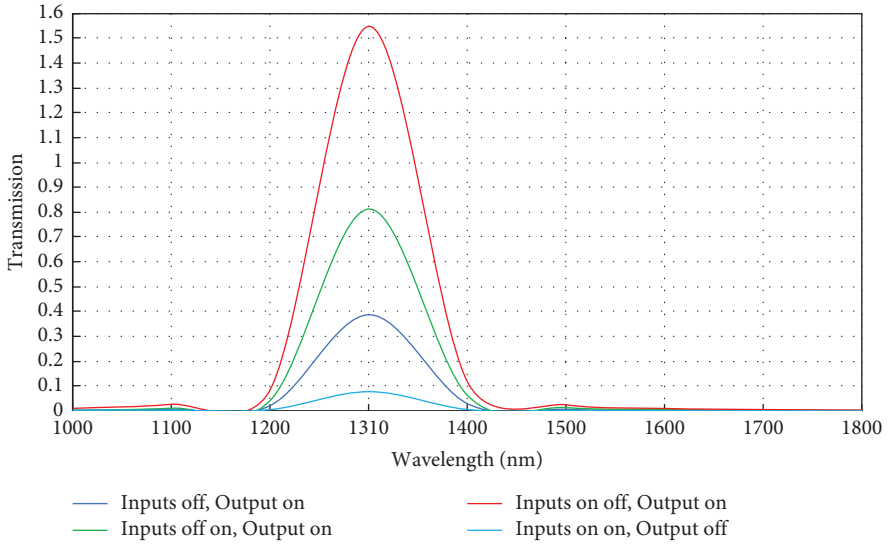



Figure 19: The transmission spectrum for the proposed NAND logic gate.

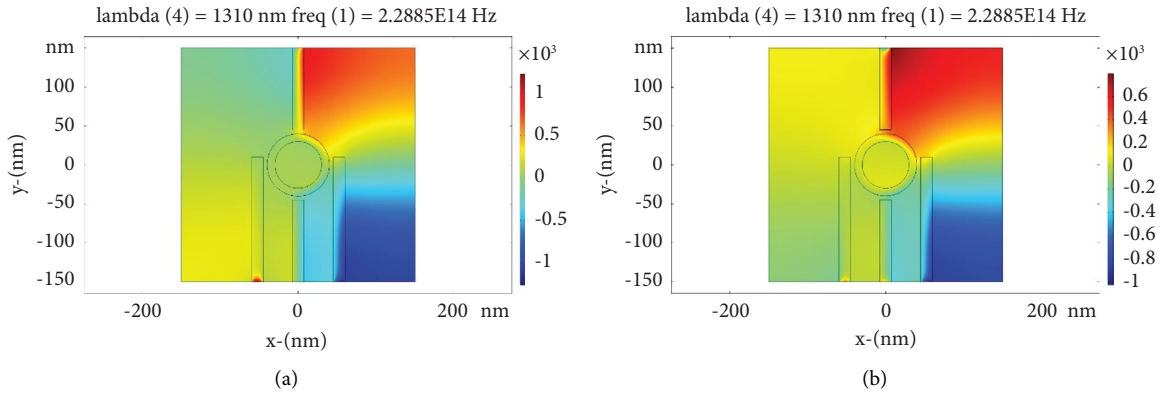
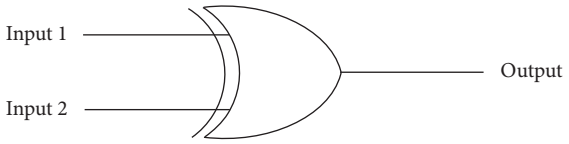



Figure 20: The Hz field profiles in two cases of the input ports are (a) OFF and (b) ON.

Table 8: Summarized simulation results for the NAND logic gate.

| Input 1 (port 2) | Input 2 (port 3) | Control (port 1) | Output (port 4) | Transmission threshold | $T$ | CR (dB) | MD (%) | IL (dB) | CL (dB) |
|---|---|---|---|---|---|---|---|---|---|
| OFF | OFF | ON (0°) | ON | 0.35 | 0.39 | 7.5 | 95.45 | 4.09 | 3.41 |
| OFF | ON (0°) | ON (0°) | ON | | 0.81 | | | | |
| ON (0°) | OFF | ON (0°) | ON | | 1.54 | | | | |
| ON (180°) | ON (90°) | ON (0°) | OFF | | 0.07 | | | | |




| Truth Table | | |
|---|---|---|
| Input 1 Port 1 | Input 2 Port 2 | Output Port 4 |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

(b)

Figure 21: (a) XOR logic gate circuit symbol and (b) the truth table. The ports 1 and 2 are considered as input ports. The ports 3 and 4 are assumed to be the control and output ports, respectively.

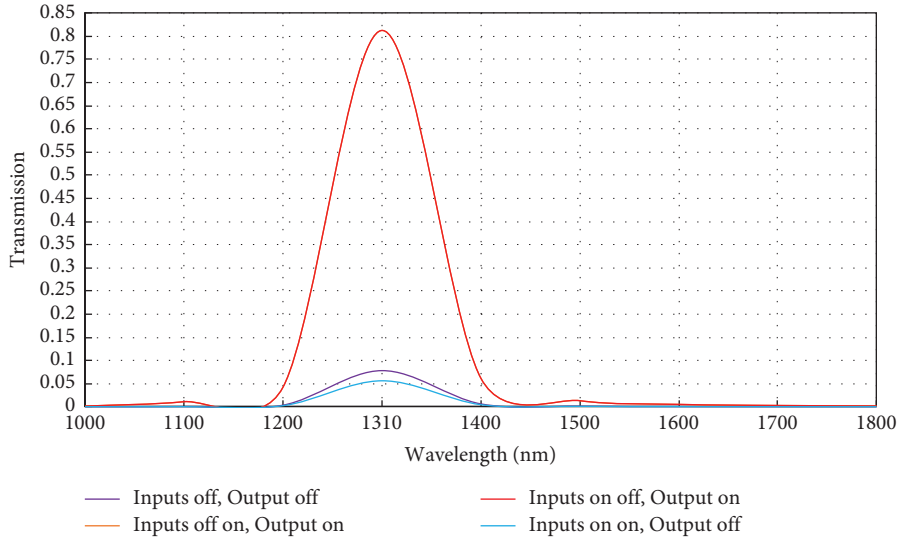



Figure 22: The transmission spectrum for the designed XOR logic gate.

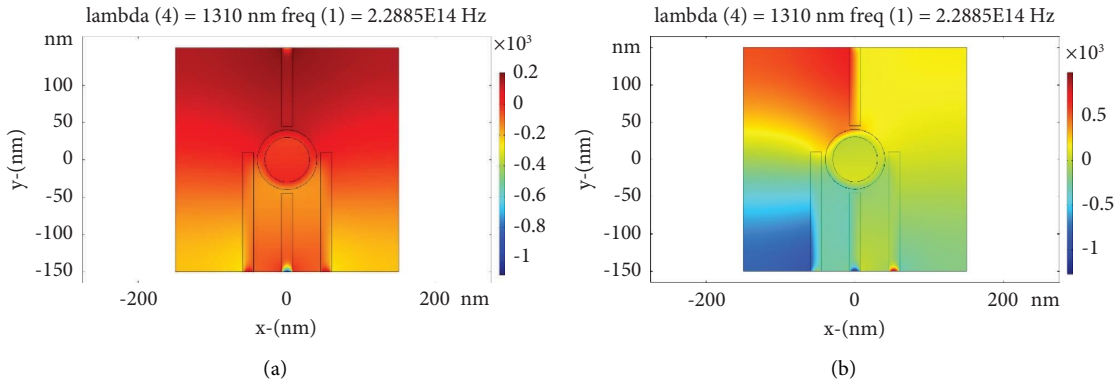
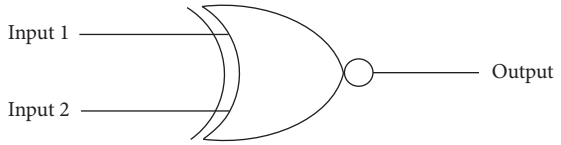



Figure 23: Distributions of the Hz field within the structure with input ports of (a) OFF and (b) ON.

Table 9: The results for the XOR logic gate.

| Input 1 (port 1) | Input 2 (port 2) | Control (port 3) | Output (port 4) | Transmission threshold | $T$ | CR (dB) | MD (%) | IL (dB) | CL (dB) |
|---|---|---|---|---|---|---|---|---|---|
| OFF | OFF | ON (0°) | OFF | 0.35 | 0.07 | 10.6 | 93.82 | 0.9 | 9.7 |
| OFF | ON | ON (0°) | ON | | 0.81 | | | | |
| ON | OFF | ON (0°) | ON | | 0.81 | | | | |
| ON (180°) | ON (45°) | ON (0°) | OFF | | 0.05 | | | | |




(a)

| Truth Table | | |
|---|---|---|
| Input 1 Port 2 | Input 2 Port 3 | Output Port 4 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

(b)

Figure 24: (a) XNOR logic gate circuit symbol and (b) the truth table. The ports 2 and 3 are considered as input ports. The ports 1 and 4 are assumed to be the control and output ports, respectively.

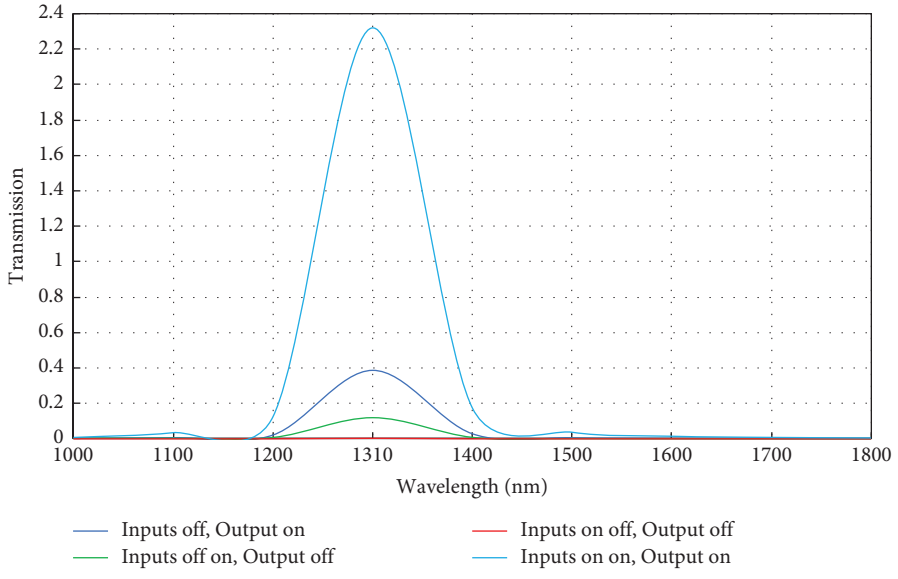



Figure 25: The transmission spectrum for the designed XNOR logic gate.

Table 10: The results for the proposed XNOR logic gate.

| Input 1 (port 2) | Input 2 (port 3) | Control (port 1) | Output (port 4) | Transmission threshold | $T$ | CR (dB) | MD (%) | IL (dB) | CL (dB) |
|---|---|---|---|---|---|---|---|---|---|
| OFF | OFF | ON (180°) | ON | 0.35 | 0.39 | 5.5 | 99.87 | 4.09 | 1.41 |
| OFF | ON(45°) | ON (180°) | OFF | | 0.11 | | | | |
| ON (45°) | OFF | ON (180°) | OFF | | 0.003 | | | | |
| ON (180°) | ON (180°) | ON (180°) | ON | | 2.32 | | | | |

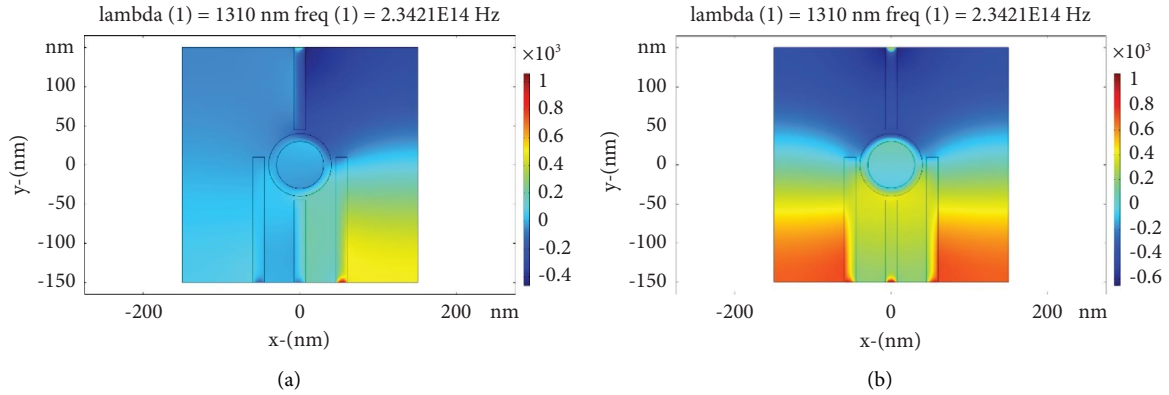



Figure 26: The counter profiles of Hz when the input ports are in (a) OFF and (b) ON states.

between the input ports and control port occurs if both input ports are ON with the same phase of 180°. Therefore, the transmission peak is 2.32, and the output port state is ON.

Figures 26(a) and 26(b) show the $z$ component of the magnetic field distribution, Hz, when the input ports are OFF and ON, respectively.

The results of the XNOR logic gate are provided in Table 10.

The CR of this logic gate is medium, so the gate performance is moderated [49]. Very high MD indicates an excellent design with optimum dimensions [40]. The IL is high, and the CL is very low. According to Tables 2 and 3, the IL and the CL values are acceptable [50].

## 5. The Comparison of the Proposed Design and Some Works

The plasmonic waveguide type, the number of resonators, the number of proposed logic gates, the size, the transmission threshold limit, the performance evaluation, the maximum of transmission, and the complexity in our work are compared with those in other works listed in Table 11.

Table 11: The comparison of the plasmonic waveguide type, the number of resonators, the number of proposed logic gates, the size, the transmission threshold limit, the performance evaluation, the maximum of transmission, and complexity in our work and some other works.

| References | Plasmonic waveguides | Number of resonators | Number of gates | Size | Transmission threshold limit | Performance measured | $T_{max}$ | Complexity |
|---|---|---|---|---|---|---|---|---|
| [5] | DMD | Two | All seven logic gates | 400 nm × 400 nm | 0.25 | $T$, CR | 175% | More |
| [34] | DMD | Two | One | 350 nm × 350 nm | 0.5 | $T$ | 72% | More |
| [35] | DMD | Two | Five | 200 nm × 400 nm | 0.3 | $T$, CR | 152% | More |
| [36] | Hybrid DMD | Two | All seven logic gates | 400 nm × 400 nm | 0.3 | $T$, CR, MD, IL | 202% | More |
| [14] | DMD | Four | All seven logic gates | 400 nm × 380 nm | 0.25 | $T$, ER | 900 nm 239% 1330 nm 187% | More |
| [37] | MDM | Two | Four | 1269 nm × 669 nm | AND 0.28 OR 0.2 NOT 0.2 | $T$ | 95% | More |
| [38] | MDM | None | Four | 2 $\mu$m × 1.2 $\mu$m | 0.1 | $T$ | 35% | More |
| [39] | MDM | None | Two | For OR gate 1125 nm × 1000 nm For NOR gate >1125 nm × 1000 nm | 0.3 | $T$, CR | 69% | More |
| [40] | MDM | One | Two | NOT 0.44, 0.47 $\mu$m NOR 0.86, 0.91 $\mu$m | 0.5 | $T$, CR | 82% | More |
| [41] | MDM | One | Five | 600 nm × 600 nm | 0.35 | $T$, CR | 190% | More |
| [42] | MDM | Eight | Six | >1350 nm × 540 nm | Non | $T$ | 97% | More |
| [43] | MDM | Non | Two | In micro meter range | 0.5 | $T$, CR | 90% | More |
| [44] | MDM | Non | Three | 13 $\mu m^2$ | 0.5 | $T$ | 90% | More |
| [44] | MDM | One | Four | About 1.5 $\mu$m × 1 $\mu$m | 0.2 | $T$, CR, gap-threshold ratio (GTR) | 143% | More |
| This work | DMD | One | All seven logic gates | 300 nm × 300 nm | 0.35 | $T$, CR, MD, IL, and CL | 232% | Less |

## 6. Conclusion

In this paper, a new design of seven plasmonic logic gates, NOT, OR, AND, NOR, NAND, XOR, and XNOR, is done. The ultrasmall structure with 300 nm × 300 nm size based on DMD plasmonic waveguides is proposed. The threshold transmission value is assumed to be 0.35 for evaluating the logic state of the output. The *T*, the CR, the MD, the IL, and the CL parameters evaluated all seven logic gates' performance. The maximum transmission ratio is obtained for AND, OR, and XNOR logic gates. Very high MD is calculated for all seven gates. For the NOT gate, maximum values of CR and CL are measured. For the AND gate, a minimum IL value is obtained. The designed logic gates can be employed in all-optical signal-processing nanocircuits and nanophotonics structures.

## Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

## Acknowledgments

This work was done in the Department of Electrical Engineering, Faculty of Engineering, Razi University, Kermanshah 6714414971, Iran.

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