

Research Article

Metallisation and Interconnection of e-Beam Evaporated Polycrystalline Silicon Thin-Film Solar Cells on Glass

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One inherent advantage of thin-film technology is the possibility of using monolithic integration for series interconnection of individual cells within large-area modules. Polycrystalline silicon thin-film solar cells do not rely on transparent conducting oxide layers as the high sheet conductivity of the emitter and BSF layers enables the lateral flow of current from the film to the metal contacts. This paper presents a new method for the fabrication of e-beam evaporated polycrystalline thin-film photovoltaic minimodules on glass. The method involves electrically isolating minicells, by laser scribing, and then forming an isolation layer on each laser scribe. The main advantage of this metallisation is to have a single aluminium evaporation step for the formation of finger and busbar features, as well as for series interconnection.

1. Introduction

Thin-film solar cells are sometimes referred to as “second-generation” solar cells. Thin-film solar cells can be only a few micrometers thick and consist of either no grain structure or very small grains with dimensions on the order of micrometers. The main advantage of thin-film solar cells over conventional silicon wafer-based solar cells is that they combine the advantages of wafer technologies (electronic stability, durability, and established industry) with those of thin-films (less raw materials, large-area compatibility, and reduced energy payback) [1–3].

Polycrystalline silicon (poly-Si) solar cells are one such thin-film material; they use abundant, nontoxic, cheap silicon raw material and utilise well-established semiconductor fabrication technologies. Furthermore, due to the high conductivity when it is highly doped, a transparent conducting oxide (TCO) layer is not necessary for the collection of generated carriers. This is in contrast to other thin-film technologies such as amorphous (a-Si) and microcrystalline ($\mu\text{c-Si}$) solar cell technologies, which generally incorporate TCOs [4, 5]. This allows for metallisation and interconnection schemes to be developed for thin-film poly-Si solar cells without the need for TCOs.

Two different metallisation schemes for poly-Si solar cells in use at the University of New South Wales (UNSW) have been developed by Widenborg and Aberle [6] and Kunz et al. [7]. The former is referred to as “self-aligned metallisation” and the later “aligned metallization.” Of these, aligned metallisation has to be used for e-beam evaporated thin-film poly-Si solar cells because submicron pinholes present in the evaporated material can result in shunting problems [8].

It is in the interest of industry and commercialisation to have metallisation schemes that combine both metallisation and interconnection in the one step. The goal of this paper is to develop an aligned bifacial metallisation and interconnection scheme that is more streamlined to an industrial process. The bifacial scheme discussed in this paper can be used for a wide variety of thin-film technologies, including cadmium telluride (CdTe) [9], micromorph [10], or large grain-sized e-beam crystallised silicon [11]. Here, e-beam evaporated poly-Si films are investigated. Poly-Si films are compatible with bifacial schemes and can also be fabricated on glass superstrates, which makes them suitable for researching light trapping capabilities. Here, a new photolithographical pattern and metallisation scheme is used to interconnect thin-film poly-Si solar cells. In the scheme,

an insulation layer is used to achieve cell interconnection with only one aluminium evaporation step, as opposed to the self-aligned method, which requires two evaporation steps.

In addition, the effect of increasing current via light trapping is investigated. This metallisation scheme is designed for bifacial cells, which allow for illumination from both the cell-side and the glass-side of the device. In the literature, silicon nanowires (SiNW) have been used to increase light absorption. Using SiNWs, absorption enhancements of up to 50% in the infrared spectrum have been reported on e-beam crystallised multicrystalline silicon thin films ($6\ \mu\text{m}$) on glass [12]. Here, a simpler light trapping method using commercial white paint as a BSR is investigated. This is particularly relevant for bifacial poly-Si films on glass, which allows current increases of up to 40% on thin ($1\text{--}2\ \mu\text{m}$) devices [13]. With any thin-film silicon solar cell technology, its compatibility with BSRs such as this is of particular interest.

In this work, a metallisation and interconnection scheme is developed and used to fabricate interconnected minimodules. Power loss equations are used to assist in the layout of the metallisation and the compatibility of the final devices with a BSR is investigated.

2. Method

Amorphous silicon is deposited and then crystallised into poly-Si by the solid phase crystallisation (SPC) [14, 15] method, followed by a dopant activation and defect removal either by rapid temperature annealing (RTA) ($900\text{--}1000^\circ\text{C}$) [16] or laser annealing [17]. Films are then hydrogen-passivated using a remote plasma at $\sim 650^\circ\text{C}$ for ~ 15 min to effectively passivate defects (dangling bonds) [18]. After hydrogen passivation, the open-circuit voltage (V_{oc}) increases by a factor of two [19].

The resulting poly-Si diode structure on glass deposited by e-beam evaporation consists of Borofloat 33 glass from Schott, 3.3 mm; silicon nitride (SiN) barrier and antireflection coating, 75 nm; n^+ emitter layer, ~ 50 nm; n^- or p^- absorber layer, ~ 2000 nm, and p^+ back surface field layer (BSF), ~ 100 nm. Light can be incident either from the glass-side or from the air side.

Prior to investigating the merits of the scheme, the very first step for designing the aligned bifacial interconnected metallisation is to obtain power loss equations for this metallisation. These equations assist in determining the optimal metallisation design of the interdigitated emitter and BSF finger pattern. In this metallisation scheme, the geometry of both the emitter and BSF features are defined by photolithography using a photomask.

The metallisation and interconnection process is listed in Figure 1. Firstly, emitter groove locations are defined by photolithography. Locations where photoresist remain acts as an etching mask for plasma etching (plasma gas SF_6 , ~ 40 Pa), where poly-Si is removed until the ~ 50 nm emitter layer remains. The plasma system used is a house-built RF direct-plasma system and the etching rate is $50\text{--}100$ nm/min.

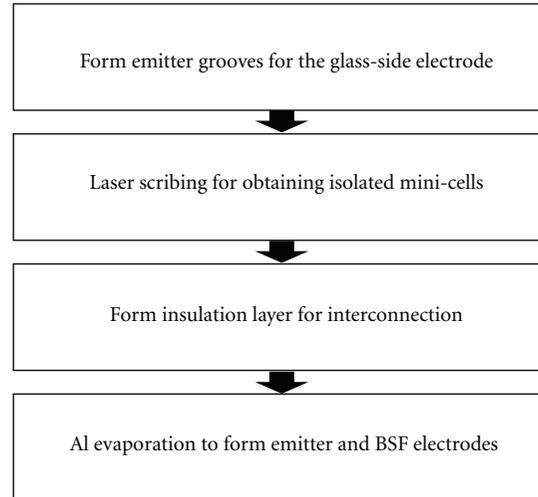


FIGURE 1: Process flow diagram for the aligned bifacial interconnected metallisation.

The second step is to electrically isolate both individual cells and separate minimodules. This isolation is done by scribing through the emitter busbar groove using a pulsed Nd:YAG laser with a 1064 nm wavelength and 2 W power.

The next step involves patterning an insulation layer partially over the laser scribed region. This insulation layer prevents the Al busbar from touching both the emitter and BSF layers during interconnection, which causes shunting. In this work, the suitability of two different insulation layers, MgF_2 and baked photoresist, is examined by both $\text{Suns-}V_{oc}$ and dark lock-in thermography (DLIT) imaging. Both of these materials are investigated as they are easy to deposit accurately and pattern as intended.

After formation of the insulation layer, a film of Al is blanket-evaporated on the BSF of the sample, and the emitter and BSF side electrode are formed via photolithography. This is followed by etching with a diluted phosphoric acid solution ($41\% \text{H}_3\text{PO}_4$) at 65°C to define the busbar and both emitter and BSF fingers. After features have been defined by the phosphoric etch, the metallisation and interconnection process is complete.

Normally, the interconnection of solar cells would need a separate stage such as a further lithography and Al evaporation step, or wire bonding [20]. For this method, however, cell metallisation and interconnection are achieved in a single Al evaporation to form the minimodules. Figure 2(a) shows a cross-sectional schematic of the Al emitter finger in an emitter groove. Figure 2(b) illustrates the comb-like interdigitated emitter and BSF electrode as made by the new metallisation and interconnection scheme.

In order to determine if the new metallisation scheme is compatible with BSRs, as well as to investigate any increases in cell current, commercial white paint (DULUX One Coat ceiling paint) is applied to the BSF side of the devices. Light I - V measurements, both before and after the application of the white paint BSR, are carried out on metallised/interconnected minimodules.

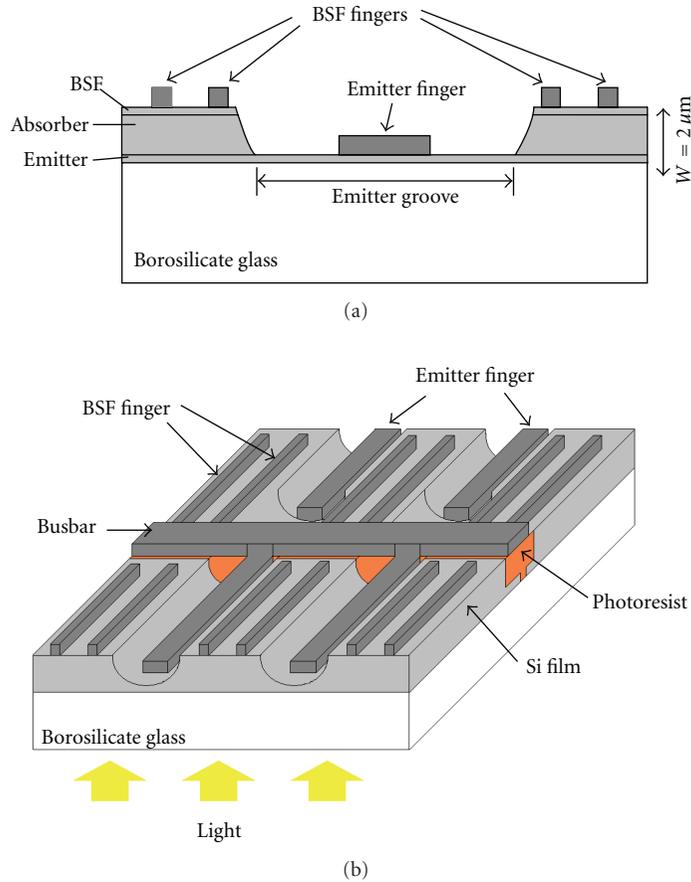


FIGURE 2: (a) Cross-sectional schematic of a poly-Si thin-film solar cell on glass with the aligned bifacial metallisation. (b) Layout of the aligned bifacial interconnected metallisation as processed in this work. In the figure, the photoresist acts as an isolation layer to prevent shunting between adjacent cells (images are not to scale).

3. Results

In order to obtain the interdigitated pattern which minimises the total power loss from the metallisation, power loss modelling for the specific aligned bifacial metallisation is required. Power loss modelling of the self-aligned metallisation, also in use at UNSW and based on the unit cell/fractional power loss approach [21, 22], has been developed by Gress and Varlamov [23]. However, the aligned bifacial metallisation shown in Figure 3(a) has line BSF fingers instead of a blanket BSF electrode, requiring modifications to the power loss formulas. In addition, the emitter fingers do not take up the entire groove width (see Figure 2(a)), which is an assumption in the model designed for self-aligned metallisation.

Therefore, new power loss formulas for the aligned bifacial metallisation need to be derived. Figure 3(b) shows a sample emitter unit cell, and a BSF unit cell is shown in Figure 3(c).

The fractional power losses (power loss divided by power at maximum power point (MPP)) are shown in Table 1. To take into account shadow losses (i.e., the fact that the current flowing towards the metallisation features is not necessarily equal to the cell's MPP current, J_{MP}) a distinction is made

between current normalised to shading percentage (J_d) and current density at MPP (J_{MP}), that is, $J_d = J_{MP}/(1 - P_{sh})$, where P_{sh} is the fractional shading percentage of emitter features.

The cell parameters and corresponding symbols used in the table are unit cell length (C), the centre-to-centre emitter groove spacing (S_E), the distance between busbar and emitter fingers (W_{AE}), the emitter finger width (W_E), and the emitter groove width (W_{FE}). These parameters are as defined in Figure 3.

By minimising the sum of these power loss formulas, the optimal pattern can be found for a given set of cell parameters. As an example, Figure 4(a) shows a graph of total power loss as a function of unit cell length (i.e., length C in Figure 3(b)), where this length has been varied between 0.5 cm and 2 cm.

Here, cell lengths either side of the optimal are selected: 0.9 cm and 1.8 cm as they allow for a 2-cell minimodules ($C = 1.8$ cm) and a 4 cell minimodule ($C = 0.9$ cm) to be fabricated on 5 cm \times 5 cm glass superstrates currently under investigation at UNSW. The design of these layouts is shown in Figure 4(b).

To form the interconnection in this metallisation scheme, an insulation layer is required on the laser scribed busbar.

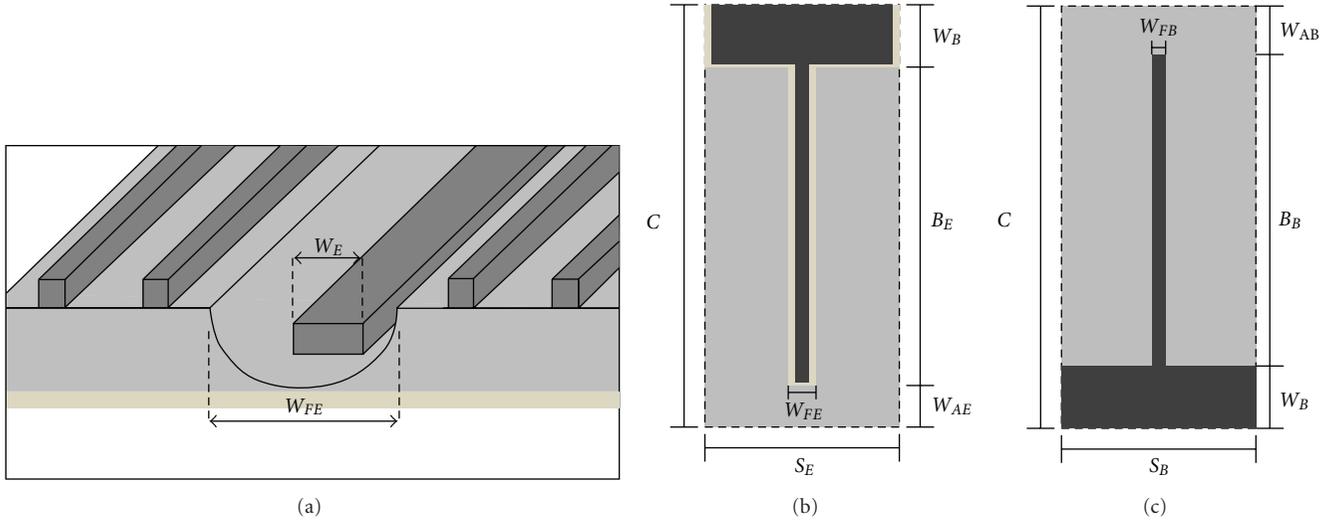


FIGURE 3: (a) Schematic representation of emitter groove and emitter finger (image is not to scale). (b) Sample emitter unit cell with labelling of each parameter. (c) Sample BSF unit cell labelling of each parameter.

TABLE 1: Area and types of power loss with formulas.

Area and types of power loss	Fractional power loss
Resistance loss in emitter layer	$(J_d^2 \rho_{s,em} / J_{MP} V_{MP} 3 B_E C S_E) (B_E + W_{AE})^2 (S_E - W_E)^3$
Resistance loss in BSF layer	$(J_d^2 \rho_{s,BSF} / J_{MP} V_{MP} 3 B_B C S_B) (B_B + W_{AB})^2 (S_B - W_{FB})^3$
Resistance loss in emitter finger	$(J_d^2 B_E \rho_{s,Al} / J_{MP} V_{MP} W_E C S_E) \left[(1/3) B_E^2 (S_E - W_E)^2 + S_E^2 W_{AE}^2 \right]$
Resistance loss in BSF finger	$(J_d^2 B_B \rho_{s,Al} / J_{MP} V_{MP} W_{FB} C S_B) \left[(1/3) B_B^2 (S_B - W_{FB})^2 + S_B^2 W_{AB}^2 \right]$
Resistance loss in busbar	$(J_d^2 A^2 \rho_{s,Al} / J_{MP} V_{MP} 3 C W_E) \left[W_{AE}^2 + B_E^2 (S_E / (S_E + W_E))^2 \right]$
Shading loss (removal of absorber layer) by the emitter groove	$B_E W_{FE} / (S_E (C - W_B))$
Shading loss by busbar	W_B / C
Contact resistance loss between emitter layer and finger	$p_c^* (J_{MP} / V_{MP}) (S_E / W_E)$
Contact resistance loss between BSF layer and finger	$p_c^* (J_{MP} / V_{MP}) (S_B / W_{FB})$

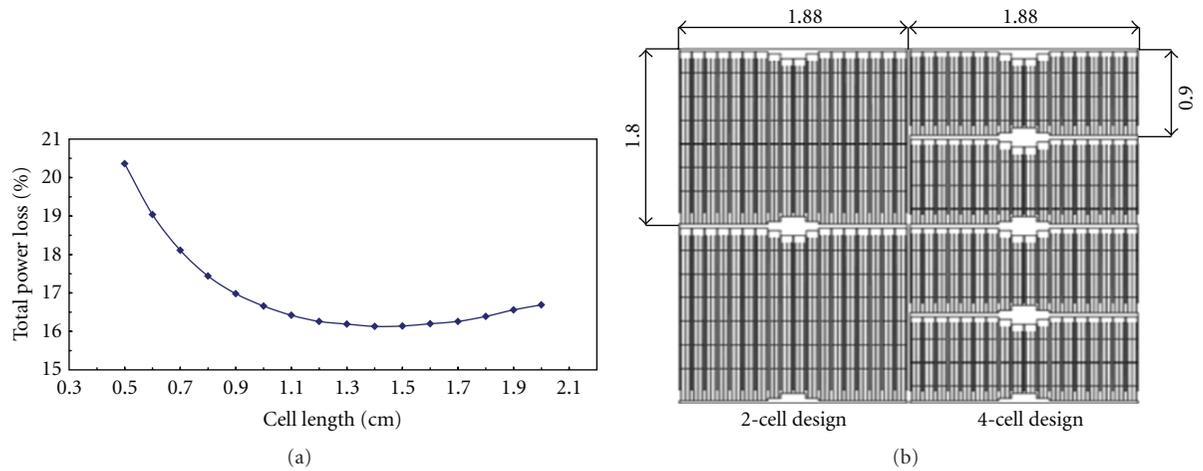


FIGURE 4: (a) Total power loss (%) as a function of cell length from 0.5 to 2 cm when all other parameters such as busbar and finger width are fixed. (b) A metallisation design that patterns the emitter, BSF fingers, and busbar (units in cm).

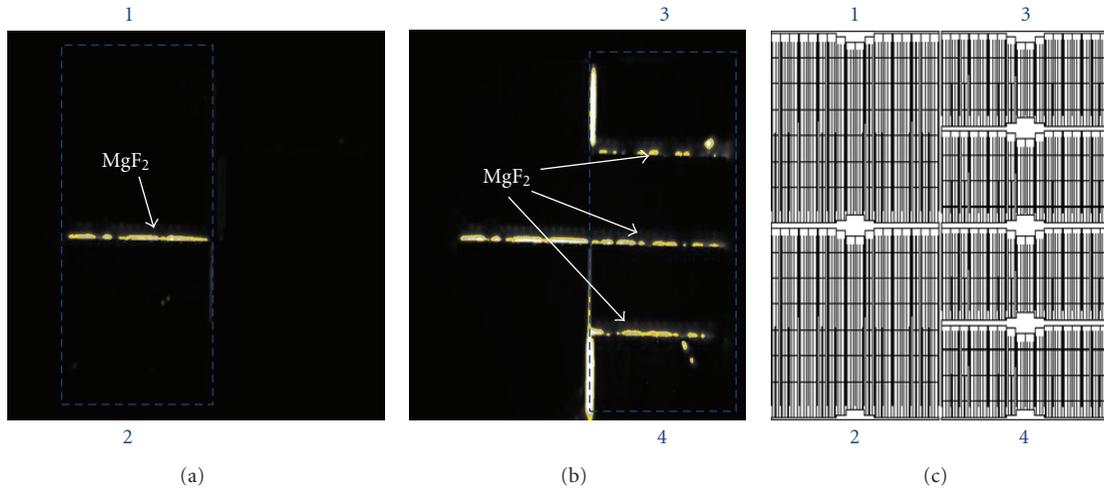


FIGURE 5: DLIT images of the sample from Table 2. (a, b) DLIT images for the cells with MgF_2 as the isolation material taken at the forward bias condition: 400 mV, lock-in frequency: 10 Hz, scale: -0.1 mK to 1 mK; (a) image is for the 2-cell minimodule on the left biased at 1 and 2; (b) image is for the 4-cell minimodule on the right biased at 3 and 4. (c) Schematic of a fully metallised sample.

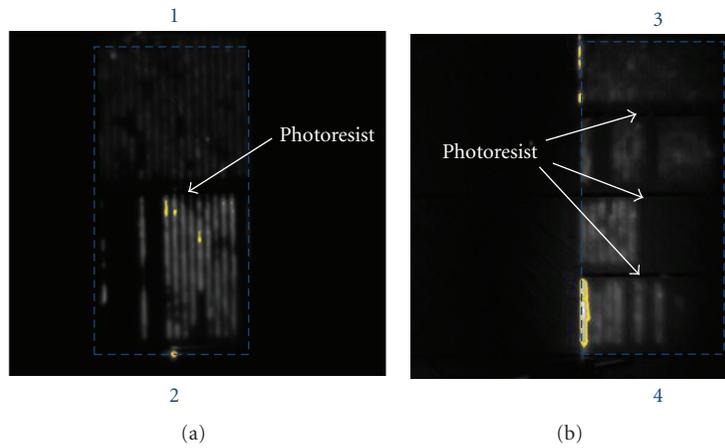


FIGURE 6: DLIT images for the cell with baked photoresist as the isolation material taken at the forward bias condition: 400 mV, lock-in frequency: 10 Hz, scale: -0.1 mK to 1 mK; (a) image is for the 2-cell minimodule on the left biased between points 1 and 2; (b) image is for the 4-cell minimodule on the right biased between points 3 and 4.

TABLE 2: Suns- V_{oc} results of the aligned bifacial interconnected metallisation when MgF_2 is used as an insulation layer.

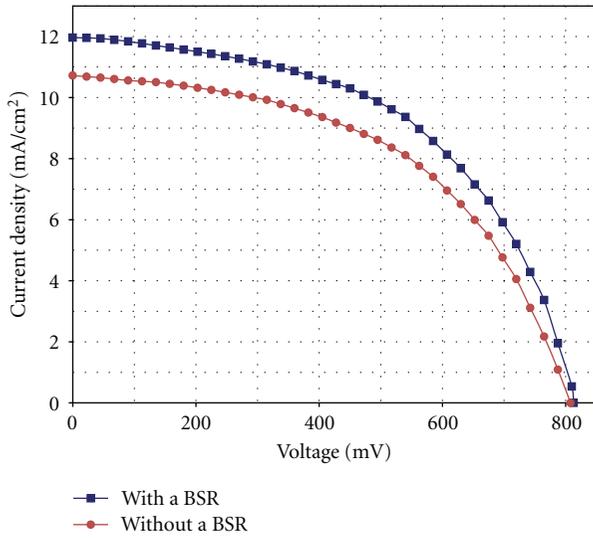
	2-cell mini-module			4-cell mini-module				Total
	Cell A	Cell B	Total	Cell C	Cell D	Cell E	Cell F	
Aperture area (cm^2)	3.4	3.4	6.8	1.7	1.7	1.7	1.7	6.8
V_{oc} (mV)	445.9	402.0	854.9	0	439.4	47.6	442.0	937.0
R_{sh} (Ω)	1388.5	95.0	204.0	Shunted	6883.8	Shunted	8077.6	1174.0

TABLE 3: Suns- V_{oc} results of the aligned bifacial interconnected metallisation when baked photoresist is used as an insulation layer.

	2-cell mini-module			4-cell mini-module				Total
	Cell A	Cell B	Total	Cell C	Cell D	Cell E	Cell F	
Aperture area (cm^2)	3.4	3.4	6.8	1.7	1.7	1.7	1.7	6.8
V_{oc} (mV)	449.3	450.0	899.2	452.4	455.5	457.6	459.2	1824.2
R_{sh} (Ω)	2660.3	1005.6	1473.0	303.7	913.2	5011.7	615.2	1710.0

TABLE 4: J - V results from the two mini-modules with and without the application of a white paint BSR.

Mini-module	Aperture area (cm ²)	V_{oc} (mV)	J_{sc} (mA)	I_{sc} (mA)	FF (%)	η (%)	R_{sh} (Ωcm^2)
Mini-moduleNo BSR	3.4	808.0	10.7	36.3	50.9	2.2	325.0
Mini-moduleBSR	3.4	813.0	11.9	40.4	49.6	2.4	311.0

FIGURE 7: One sun J - V curves from the 2-cell minimodule before (blue) and after (black) the white paint BSR was applied.

Firstly, in order to find a suitable insulation layer, 300 nm of MgF_2 was thermally evaporated onto the laser scribed emitter groove using a shadow mask.

Table 2 shows the Suns- V_{oc} results of both the individual cells and minimodules with MgF_2 as an insulation layer. Shunting is present in some of the cells and it is suspected that this is due to the MgF_2 insulation layer. In addition, cells B, C, and E show a reduction in open-circuit voltage (V_{oc}) from the premetallisation V_{oc} of ~ 440 – 450 mV. To analyse the exact cause of the shunting, DLIT measurements were taken and those are shown in Figures 5(a) and 5(b). Their positions relative to the mask design are shown in Figure 5(c). Cells C and E were heavily shunted and exact resistance (shunt resistance R_{sh}) could not be obtained.

The light areas in Figures 5(a) and 5(b) represent the shunting area—the same location as the MgF_2 insulation layer at the interconnection sites. It is clear that MgF_2 is not a suitable material for forming the insulation layer as shunting occurs along the busbar where the MgF_2 insulation layer was patterned.

An alternative insulating material investigated is positive photoresist (Microposit S1818, 300 nm thickness). Photoresist has the advantage of being easy to apply and pattern, and does not require semivacuum conditions for deposition.

The resulting data from Suns- V_{oc} measurements is summarised in Table 3. It shows that shunting in the insulation layer is not an issue when baked photoresist layer is used. In addition, the open-circuit voltages of all cells are consistent throughout both minimodules and are comparable to their pre-metallisation V_{oc} of ~ 440 – 450 mV.

The lack of shunting can be supported by the DLIT images shown in Figures 6(a) and 6(b). Since there are no shunting sites (yellow colouring) on the busbar area where the photoresist insulating layer is, no shunting at the interconnection sites is occurring. The shunting site in the lower left of Figure 6(b) is due to incomplete isolation between the 2- and 4-cell minimodules and is independent of the insulation layer.

These results show that photoresist is a good candidate as an insulating layer for this metallisation scheme.

It is well known that BSRs can increase the current of thin-film bifacial cells. Here, we investigate the compatibility of photoresist insulation layers with commercial white paint and determine if any increase in current can be obtained.

In order to investigate current gain for cells with a BSR, two adjacent cells of similar J_{sc} values were interconnected in series using this metallisation scheme, and light I - V measurements were taken (approximated AM1.5G spectrum, 100 mW/cm^2 , cell temperature 25°C). Table 4 shows values measured by light I - V of the minimodules before and after a white paint BSR was applied, and Figure 7 shows the J - V curves (current density-voltage curves) from the minimodule before (blue) and after (black) the white paint BSR was applied.

A short-circuit current density (J_{sc}) gain of $\sim 11.2\%$ for the module ($10.7 \text{ mA} : 11.9 \text{ mA}$) was obtained by applying the white paint BSR in Table 4. Both minimodules were apertured to 3.4 cm^2 during the measurements. The fill factor (FF) decreased slightly; however an increase in efficiency of $\sim 9\%$ was obtained.

4. Conclusion

A new aligned bifacial interconnected metallisation scheme that uses a method of interconnecting cells into minimodules with a photoresist insulation layer has been presented. The main advantage of the metallisation is to achieve cell metallisation and interconnection in a single Al evaporation step. The unit cell approach/fractional power loss method is used to find the optimal design with the busbar width and finger spacing being fixed. It is proven from DLIT images that 300 nm of photoresist is a good candidate as an insulating layer for this metallisation scheme. The open-circuit voltage of the minimodules is the sum of each of the individual cells, indicating successful interconnection has taken place. A gain in short-circuit current of over 11% was realised via the application of a white paint BSR.

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