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Research Article

High-Efficiency Si Solar Cell Fabricated by Ion Implantation and Inline Backside Rounding Process

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We introduce a novel, high-throughput processing method to produce high-efficiency solar cells via a backside rounding process and ion implantation. Ion implantation combined with a backside rounding process is investigated. The ion implantation process substituted for thermal $POCl_3$ diffusion performs better R_{sheet} uniformity (<3%). The U-4100 spectrophotometer shows that wafers with backside rounding process perform higher reflectivity at long wavelengths. Industrial screen printed (SP) Al-BSF on different etching depth groups was analyzed. SEMs show that increasing etch depth improves back surface field (BSF). The I-V measurement revealed that etching depths of $6\,\mu m \pm 0.1\,\mu m$ due to having the highest V_{OC} and I_{SC}, it has the best performance. SEMs also show that higher etching depths also produce uniform Al melting and better BSF. This is in agreement with IQE response data at long wavelengths.

1. Introduction

With the issue of global weather increasingly warming, as well as the depletion of resources, renewable energy has become very important. In the face of environmental awareness, many governments have introduced environmental legislation and implemented renewable energy proposals. Solar power, one kind of renewable energy, has grown at least 20% per annum over the past ten years as a result of incentives offered by the government. However, the final purpose of solar electric power is to achieve grid parity. In order to achieve grid parity, lowering manufacturing cost and increasing efficiency are very important ways. Reducing silicon bulk thickness is one solution of lowering manufacturing cost. It will increase the number of wafers per ingot or brick and reduce the price per watt. However, it could cause wafer handling problems. The higher wafer breakage rate during cell and module processing is a trade-off. It is quite obvious that the improvement of solar cell efficiency is very important in the future.

There are many process methods to improve solar cell efficiency, such as metal wrap through (MWT) solar cell [1, 2], emitter wrap through (EWT) cells [3, 4], interdigitated backside contact (IBC) cells [5, 6], laser fired contacts cells [7, 8], ion implanted cells [9, 10], and so forth. Through these methods, ion implantation is one of attractive process with mass production. In this paper, blanket emitter processed by ion implantation combined with a backside rounding process can achieve high efficiency >19%.

2. Experiment

The 6 inch (156 mm × 156 mm, pseudo square-shaped) single crystalline Czochralski silicon wafers (CZ-Si) (Sino-American Silicon Company (SAS)) with a resistivity of 0.5–3 ohm-cm, and a thickness of 180–200 μm was used as the substrate in this study. Figure 1 shows a comparison of the ion implantation process with and without backside rounding. Here, the control group is samples that have undergone ion implantation without the backside rounding process. The experimental group is samples that have undergone ion implantation with the backside rounding process. Firstly, in order to reduce surface stress caused by the wire saw, a saw damage removal step is needed. Wafers were batch dipped

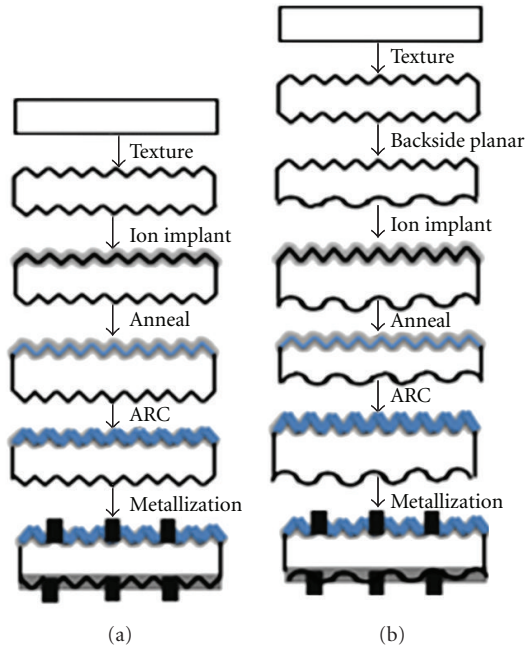

Figure 1: Comparison of ion implantation process with and without backside rounding process flow. (a) Ion implantation process without backside rounding process. (b) Ion implantation process with backside rounding process.

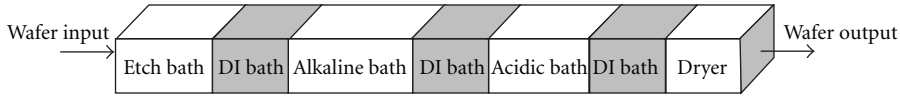

Figure 2: Chemical process steps of an inline roller type machine.

into Teflon tanks full of high KOH concentration (5.04 wt%) without IPA solution mixing as a saw damage removal process step. Then, anisotropic etching with a volume ratio of $KOH : IPA : H_2O = 1 : 1.6 : 34$ produced pyramids on the surface to absorb incoming light and increase the light path in the silicon bulk.

The next step for the experimental group is backside rounding. An inline backside rounding processing system with roller type transportation, InOxSide tool (Rena GmbH), is used to pare back surface pyramids. There are 3 chemical baths and 3 rinse baths in the system. Figure 2 shows the chemical process steps of this inline machine. The first bath is the back surface etching bath with a volume ratio of $H_2O : HF : HNO_3 : H_2SO_4 = 19 : 2 : 11 : 8$. In this bath, there are four chemical reaction steps for isotropic silicon etching, and concave pyramids rounding of the back surface is performed. The steps are: (i) NO_2 formation; (ii) oxidation of silicon by NO_2; (iii) formation of SiO_2; (iv) etching of SiO_2. The formulae are show below [11]:

$$\begin{aligned}
&\text{(i) } HNO_2 + HNO_3 \longrightarrow 2NO_2 + H_2O \\
&\text{(ii) } 2NO_2 + Si \longrightarrow Si_2{}^{+} + 2NO_2{}^{-} \\
&\text{(iii) } Si_2{}^{+} + 2(OH)^{-} \longrightarrow SiO_2 + H_2 \\
&\text{(iv) } SiO_2 + 6HF \longrightarrow H_2SiF_6 + 2H_2O
\end{aligned} \tag{1}$$

H_2SO_4 is used to increase the chemical density and does not react with the other chemical.

There are four different etching depths ED0, ED3, ED6, and ED9 in this study. ED0 signifies an etching depth of 0 μm. ED3, ED6, and ED9 signify etching depths of 3 μm $\pm$ 0.1 μm, 6 μm $\pm$ 0.1 μm, and 9 μm $\pm$ 0.1 μm, respectively. In order to achieve these etching depths, the process temperatures are 10°C, 15°C and 20°C for ED3, ED6, and ED9, respectively. The process roller speed is maintained at 1.2 m/min and the chemical concentration is kept constant. During this etching process step, a byproduct of porous silicon is formed around the wafer. This porous silicon is a recombination center and will decrease carrier lifetime. Therefore, an alkaline bath is needed to clean the porous silicon. 5% KOH was used to clean the porous silicon. Finally, in the third acidic bath, 5% HF is used to clean native oxide.

An inline, high-throughput (>1000 pcs/hr) machine (Varian Semiconductor Equipment Associates (VSEA)) was used to perform ion implantation. Wafers were transferred into a vacuum chamber by a belt transmission system and then the wafer surface was bombarded with ion dopant, which subsequently penetrated into the wafer. In this study, a PH_3 gas as a P^+ ion source, at a low beam energy of 10 keV and a dose of 3.0E15 P^+/cm^2 was selected for implanting onto the surface. However, crystal damage occurred during the ion bombardment procedure. Fortunately, the high-temperature annealing process step can rectify this damage.

In the annealing process step, wafers were vertically placed into a quartz boat and the boat was moved into a quartz tube. Then, dry oxide (O_2) was passed into the tube to activate the dopant. At the same time, a thin silicon oxide layer formed on the wafer surface. The reaction is shown below:

$$\mathrm{Si} + \mathrm{O_2} \longrightarrow \mathrm{SiO_2} \tag{2}$$

The dopant concentration profile will be different from $POCl_3$ after the high-temperature annealing process step [12–15].

After the annealing step, SiNx was deposited on the silicon surface by PECVD. In this study, wafers were automatically placed into a batch type machine (Centrotherm GmbH) and deposition was performed directly by PECVD. The SiNx layer functions as an anti-reflection coating (ARC), which increases the amount of light absorbed by silicon and also passivates the silicon surface. As a result of thin silicon oxide existing on the wafer surface during the annealing process step in the ion implant process flow, the silicon nitride thickness of the implant process is thinner than that of the conventional $POCl_3$ process.

After ARC deposition, a metal contact was formed by a Baccini belt type screen printing system and a Despatch co-firing system. In the screen printing process step, silver (Ag) paste (Heraus 9411) was printed onto the front surface to produce three busbars and 78 finger lines. Backside silver (Ag) paste (Dupont PV-157) and backside Aluminum (Al) paste (Monocrystal 1203) were used.

Single pulse solar simulators from Berger Lichttechnik are used to measure the basic parameters and I-V curves of cells under standard test conditions (STC): irradiance of 1,000 W/m^2, solar spectrum of AM 1.5 and temperature at 25°C. Electrical characteristics including V_{OC}, I_{SC}, FF, Pmax and cell efficiency are obtained from the I-V cure. The shunt resistance R_{SH} was determined by the linear slope of the reverse dark current on each cell. The series resistance R_S is calculated from two I-V curves measured at 1000 W/m^2 and 500 W/m^2, respectively, according to IEC 891.

3. Results and Discussion

400 pieces were textured at the same time to determine process quality. After texturing, we randomly separate these wafers into 4 groups of 100 pieces. Then, we picked 3 groups and performed backside rounding by etching. The remaining group is the control group, which was not backside rounded. We used an InOxSide machine (Rena GmbH) to perform the backside rounding process. In this process, there were 8 tracks for wafer input, and the roller speed was kept at 1.2 m/min for high throughput (>2500 pcs/hr). Here, we use a JSM-6510 SEM (JEOL Ltd.) to analyze the pyramid topology. Figures 3(a) and 3(b) show 1400x and 3000x SEMs of the pyramid topology without backside rounding. As the figures show, the pyramids are fully apparent on the wafer surface. Figures 3(c) and 3(d) show 1400x and 3000x SEMs of the pyramid topology for etching performed to a 3 μm ± 0.1 μm etching depth in the backside rounding process. The chemicals have started to isotropically etch small pyramids surrounded big pyramids. Figures 3(e) and 3(f) show 1400x and 3000x SEMs of the pyramid topology for etching performed to a 6 μ m ± 0.1 μm etching depth in the backside rounding process. The chemicals have started to etch the sides of the big pyramids and bowl shape etching is apparent surrounding the top of the pyramids. Figures 3(g) and 3(h) show 1400x and 3000x SEMs of the pyramid topology for etching performed to a 9 μm ± 0.1 μm etching depth in the backside rounding process. The sides of pyramids have been severely bowl shape etched by isotropic chemical etching.

After backside rounding etching, a U-4100 UV-vis-NIR spectrophotometer (Hitachi) was used to measure the reflectivity. The U-4100 has two light sources, which can measure reflectivity from a wavelength of 240 nm to 2600 nm and an integrating sphere, which can measure the scattering a texturized wafer. We randomly picked 4 pieces of wafer from each group. Every piece was measured at 5 points, and the values were averaged. Figure 4 shows a comparison of the reflectivity of four different etching depths after backside rounding.

As the figure shows, there is no obvious difference in the short and mid wavelength ranges. However, at long wavelengths (>1100 nm), a difference between the samples becomes apparent. As the etching depth increases, the reflectivity increases. The weighted reflectance R_w% is calculated to identify the performance [16]:

$$R_w\% = \frac{\int_{\lambda 1}^{\lambda 2} F_i(\lambda) Q_i(\lambda) R(\lambda) d\lambda}{\int_{\lambda 1}^{\lambda 2} F_i(\lambda) Q_i(\lambda) d\lambda}, \tag{3}$$

where $F_i(\lambda)$ is the photon flux, $Q_i(\lambda)$ is the cell internal quantum efficiency [17, 18]. Table 1 shows a comparison of the R_w% of four different etching depths. The R_w% of ED9 is 14.95%, which is the higher than the other samples. The low value is due to poor response at the long wavelengths.

After backside rounding, ion implantation is performed. Four groups of wafers were automatically transferred into the chamber and the P^+ ion source was implanted onto the wafer surface. In order to activate dopant on the wafer surface, high-temperature (800°C) annealing was performed. A four-point probe (Quatek Co., Ltd.) was used to measure sheet resistance (R_{sheet}). Table 2 shows the R_{sheet} results for different etching depths after annealing. The R_{sheet} values of the four groups have an average 65 ohm/sq and good uniformity (<3%). A thin SiO_2 layer was formed on the wafer surface after annealing, and an ellipsometer (SEMILAB Semiconductor) with a single-wavelength HeNe laser operating at a wavelength of 632.8 nm was used to measure the thickness of SiO_2. Four pieces of wafer from each group were picked at random and the thickness of SiO_2 measured. Each wafer was measured at 9 points and the results averaged. Table 3 shows a comparison of SiO_2 thicknesses and uniformities of four different etching depths. The results show that the thickness of SiO_2 is around 16.5 nm and also had good uniformity (<1%). The R_{sheet} and thickness of SiO_2 are not related to etching depth.

After the annealing process, the anti-reflection coating, SiNx layer, is deposited on top of the SiO_2 in order to minimize reflection from the front surface of the cell. Figure 5

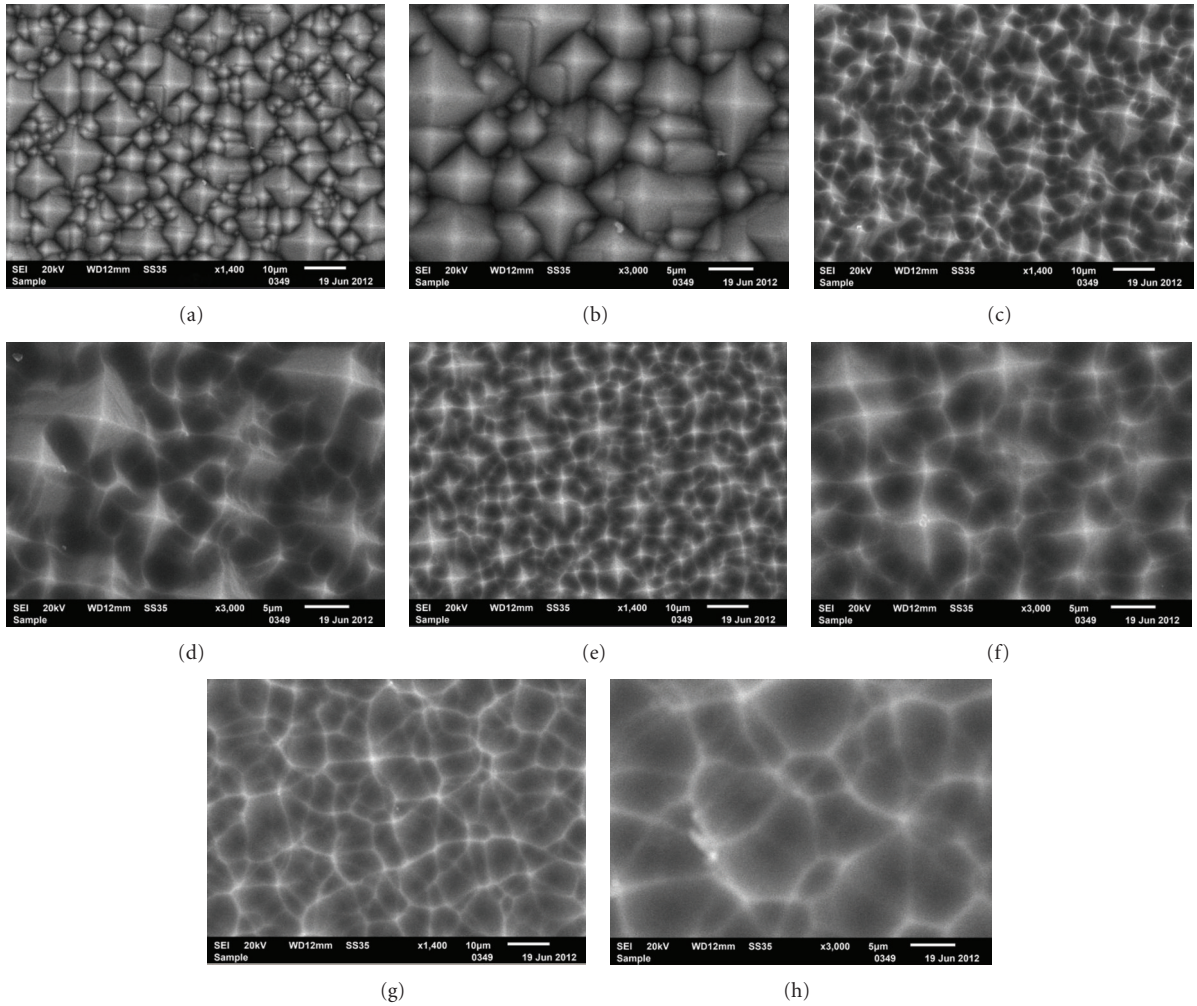

Figure 3: SEMs of pyramids topology: (a) 1400x and (b) 3000x process without backside rounding process. (c) 1400x and (d) 3000x process with backside rounding of ED3. (e) 1400x and (f) 3000x process with backside rounding of ED6. (g) 1400x and (h) 3000x process with backside rounding of ED9.

Table 1: The R_w% comparison of different etching depths.

	ED0	ED3	ED6	ED9
R_w%	14.54	14.71	14.88	14.95

Table 2: R_{sheet} results of different etching depths after annealing.

R_{sheet} [ohm/sq]	Max	Average	Min	Uniformity (%)
ED0	66.58	64.7	63.2	2.61%
ED3	67.31	65.3	63.6	2.84%
ED6	66.78	64.9	63.4	2.60%
ED9	66.77	65.1	63.23	2.72%

Table 3: Comparison of SiO_2 thickness and uniformity of different etching depths.

	ED0	ED3	ED6	ED9
SiO_2 thickness (nm)	16.54	16.49	16.56	16.61
Uniformity (%)	0.79%	0.82%	0.73%	0.67%

Table 4: The R_w% comparison of different etching depths after ARC deposition.

	ED0	ED3	ED6	ED9
R_w%	4.44	4.55	4.62	4.67

shows the reflectivities of the four different etching depths. The profile shows that the reflectivity of ED9 is highest at long wavelengths. Comparing the results after backside rounding, the difference between each group is reduced at longer wavelengths. Table 4 shows the values of R_w% after ARC deposition, and ED9 has the highest R_w% of 4.67%.

Finally, the wafers were screen-printed and cofired. In this study, the relation between four different etching depths and back surface field (BSF) were investigated. Figure 6 shows an SEM cross-sectional comparison of the BSF topology, performed for four different etching depths. The wafer without backside rounding is shown in Figure 6(a). In this

Table 5: The devices characteristic of different etching depths.

Item	V_{OC}(V)	I_{SC} (A)	R_S (mohm)	R_{SH} (ohm)	FF (%)	N_{cell} (%)	I_{rev} (A)
ED0	0.634	8.86	2.39	63.47	79.72	18.74	0.49
ED3	0.636	8.88	2.36	61.21	79.73	18.84	0.52
ED6	0.640	8.93	2.23	59.81	79.75	19.07	0.55
ED9	0.638	8.91	2.37	60.65	79.74	18.97	0.59

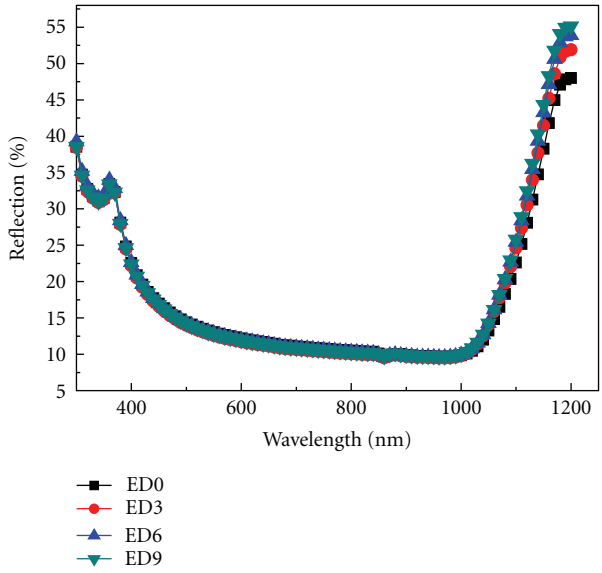

Figure 4: Comparison of reflectivity of four different etching depths after backside planar process.

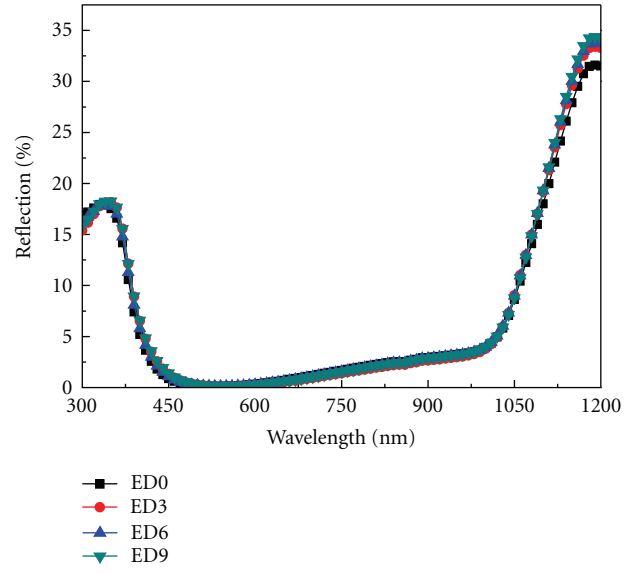

Figure 5: Comparison of reflectivity of four different etching depths after ARC.

figure, disconnection of the BSF layer and poor uniformity of Al-Si alloy layer are evident. Figure 6(b) shows the cross-sectional SEM of ED3, BSF connection is better than that of ED0, but the uniformity of the Al-Si alloy layer is still worse. Figures 6(c) and 6(d) show the cross-sectional SEMs of ED6 and ED9. The figures show that the uniformity of BSF and Al-Si is better than ED0 and ED3. This will result in V_{OC} values of ED6 and ED9 that are better than those of ED0 and ED3.

Figure 7 shows V_{OC} and I_{SC} for four different etching depths. The figure shows that V_{OC} and I_{SC} increase with increasing etching depth. Higher V_{OC} and I_{SC} are due to higher carrier lifetimes after backside rounding process. This result is accordant with the BSF performance in Figure 6. Better uniformity of BSF and Al-Si alloy will reduce the dangling bonds and surface defect states density, which result in lower back surface recombination velocity [19]. The I_{SC} of ED9 is lower than that of ED6. This is due to the reflectance of ED9 being higher than that of ED6. Figure 8 shows the R_S and FF of four different etching depths and that they are independent of it. Figure 9 shows the efficiency of four different etching depths. The best performance is obtained for the conditions of ED6. All the electric characteristics are shown in Table 5. The results show that the best average efficiency is 19.07%. Higher efficiency is due to higher V_{OC} and I_{SC}, which is caused by better BSF performance.

QEX10 system (PV Measurement Inc.) is used to measure quantum efficiencies. The QEX10 system uses a xenon arc lamp source, monochromator, filters and reflective optics to provide stable monochromatic light for device testing. Broadband bias light also illuminates the test device to simulate end-use conditions. Figure 10 shows the internal quantum efficiency (IQE) response of four different etching depths. In the mid- and long-wavelength regions, the IQE responses of ED6 and ED9 are higher than ED0 and ED3. The IQE data agree with the BSF performance and measured V_{OC}, revealing that a better IQE response can be obtained by higher fabrication etching depths.

4. Conclusion

In this study, a novel process of ion-implanted emitter formation and backside rounding for high-efficiency solar cells was investigated. This innovative process raised cell efficiency to 19.07% on solar CZ grade wafer. Rounding was performed by a high-throughput (>2500 pcs/hr) tool InOxSide (Rena GmbH). SEMs show that for etching depth

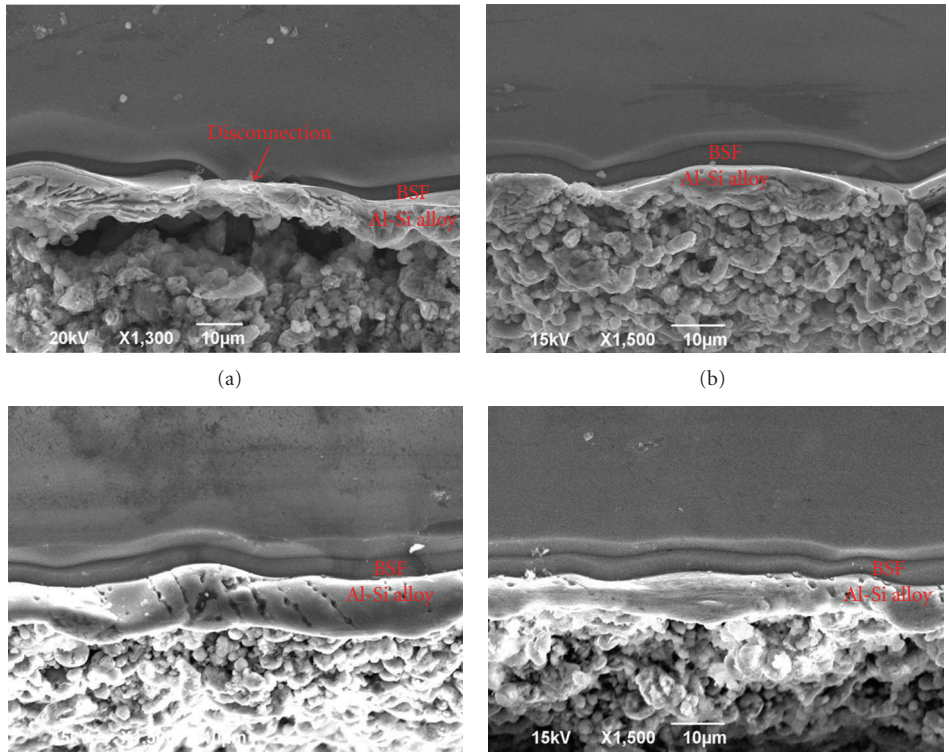

Figure 6: SEM comparison of cross-section of the BSF topology and Al-Si alloy layer of (a) ED0, (b) ED3, (c) ED6, (d) ED9.

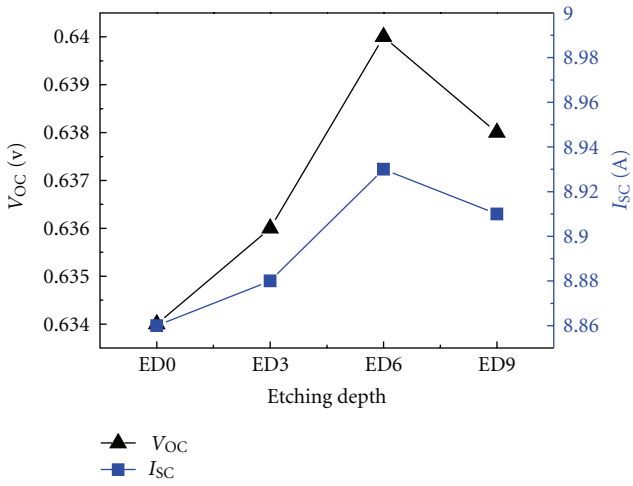

Figure 7: V_{OC} and I_{SC} of four different etching depths.

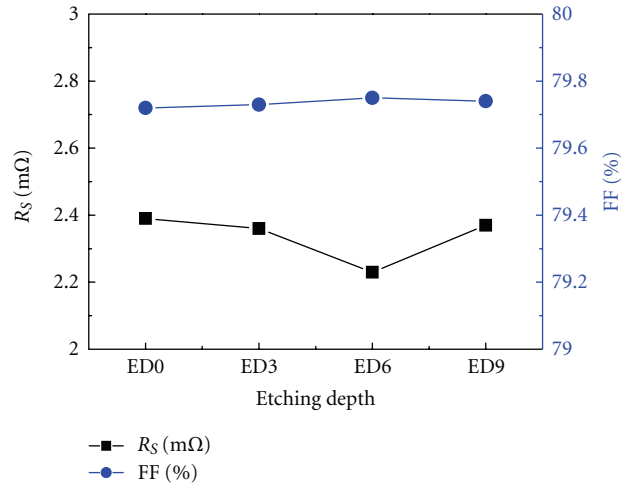

Figure 8: R_S and FF of four different etching depths.

more than 6 μm, the pyramids start to be chemically etched and assume a bowl shaped appearance. The reflectivity profile proves that the higher the etch depth, the higher the reflectivity will be at long wavelengths. After the screen printing and cofiring process, the SEM shows that etching depths of 6 μm $\pm$ 0.1 μm and 9 μm $\pm$ 0.1 μm have better BSF and Al-Si alloy layer uniformities. The internal quantum efficiency (IQE) response also reveals that higher etching depths have better responses at long wavelengths. Finally, the *I-V* tester presents that V_{OC} and I_{SC} of etching depths of 6 μm $\pm$ 0.1 μm is the best. This is due to a higher carrier lifetime contributed to by better long wavelength response.

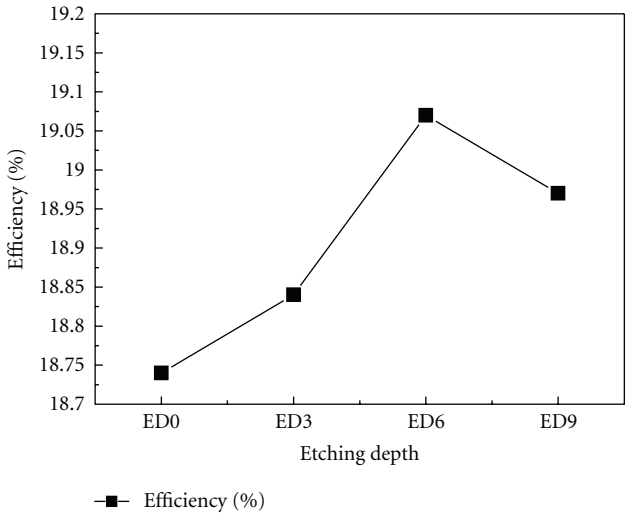

Figure 9: Efficiency of four different etching depths.

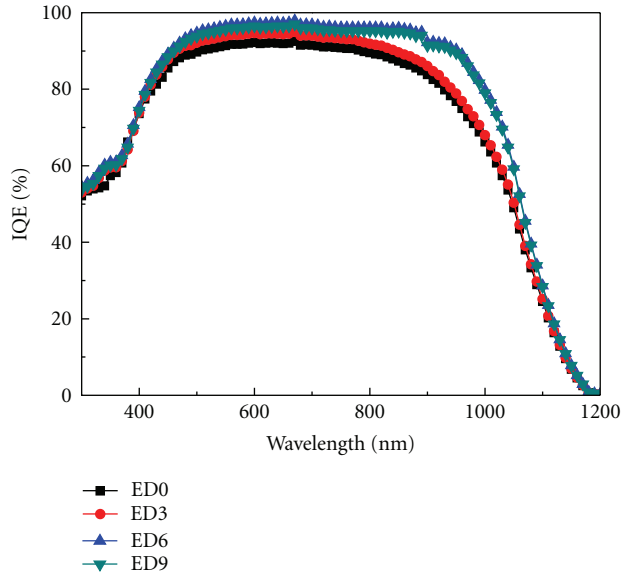

Figure 10: Internal quantum efficiency (IQE) of four different etching depths.

Acknowledgments

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