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Research Article

Quantification of Power Losses of the Interdigitated Metallization of Crystalline Silicon Thin-Film Solar Cells on Glass

Peter J. Gress and Sergey Varlamov

School of Photovoltaic and Renewable Energy Engineering, The University of NSW, Sydney, NSW 2052, Australia

Correspondence should be addressed to Peter J. Gress, p.gress@unsw.edu.au

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The metallization grid pattern is one of the most important design elements for high-efficiency solar cells. This paper presents a model based on the unit cell approach to accurately quantify the power losses of a specialized interdigitated metallization scheme for polycrystalline silicon thin-film solar cells on glass superstrates. The sum of the power losses can be minimized to produce an optimized grid-pattern design for a cell with specific parameters. The model is simulated with the standard parameters of a polycrystalline silicon solar cell, and areas for efficiency improvements are identified, namely, a reduction in emitter finger widths and a shift toward series-interconnected, high-voltage modules with very small cell sizes. Using the model to optimize future grid-pattern designs, higher cell and module efficiencies of such devices can be achieved.

1. Introduction

Solar cells based on very thin layers of crystalline Si promise to significantly reduce the cost of photovoltaic (PV) electricity as compared to traditional Si wafer-based technologies. Such cells use a small fraction of an expensive silicon material and aim to combine the strengths of the Si wafer-based PV with advantages of the thin-film approach [1, 2]. Polycrystalline Si (poly-Si) thin-film solar cells on glass, which are only 2-3 microns thick, are one such technology. Advantages of poly-Si over wafer-based technologies include the potential for cheaper end products, since only a fraction of the silicon material is used, the prospects of monolithic fabrication schemes, and the ability to deposit the films over large areas using glass as a supporting material [2].

The current efficiency record for poly-Si thin-film solar cells stands at 10.5% on small scale (94 cm^2) minimodules produced by CSG Solar [3, 4]. The metallization scheme used to fabricate the minimodule contains etched holes of varying depths that contact the emitter layer and back surface regions of the device. An alternative metallization scheme has also been developed [5] using an interdigitated metallization pattern. This scheme has been used to fabricate 9.3% efficient cells and 8.3% efficient interconnected modules [6], and further efficiency improvements can be achieved upon optimization of the interdigitated metallization.

In this paper, we introduce the concept of flow current and combine this with cell structures unique to thin-film on-glass technologies to quantify the power losses resulting from the interdigitated metallization of such devices. These losses are then normalized to the cell area and summarized. The extent of which the losses are affected by changes in cell parameters is then investigated.

2. Fabrication

The thin-film solar cells under investigation in this paper are deposited and metallized at the Thin-Film Group at the University of New South Wales (UNSW), Sydney, Australia. These are formed by the solid-phase crystallization (SPC) of a-Si:H precursor diodes prepared by plasma-enhanced chemical vapour deposition (PECVD). The device structure consists of Schott Borofloat33 glass, silicon nitride antireflection coating (~70 nm), which also acts as an impurity

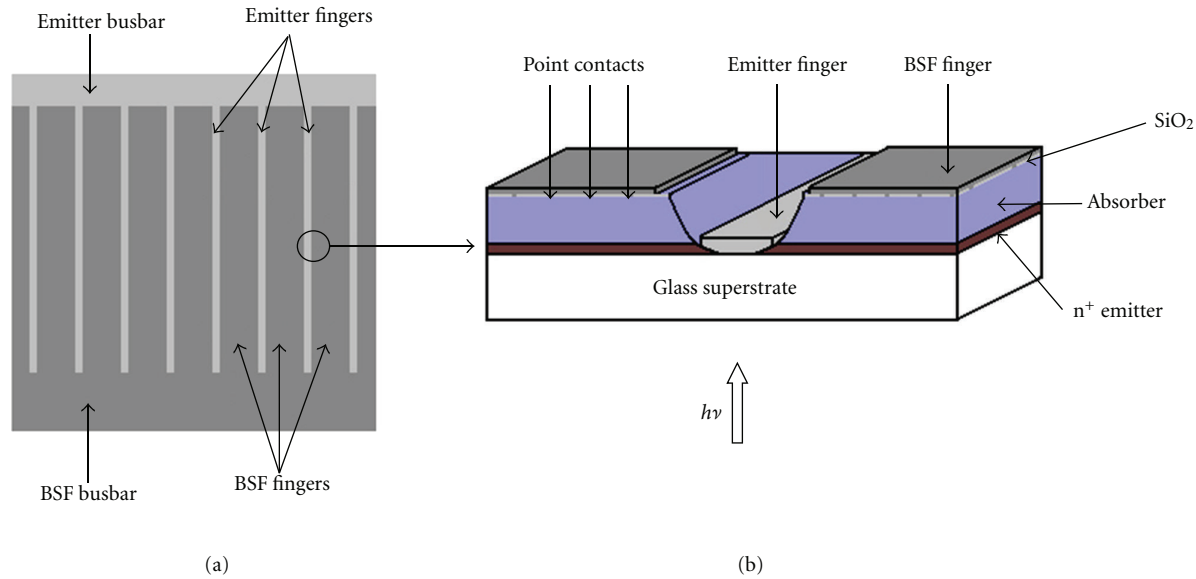

Figure 1: An interdigitated metallization of a poly-Si thin-film solar cell on a glass superstrate. (a) A top-down, "macro" schematic view of a interdigitated-metallized solar cell. The emitter and BSF busbars are used to transport current to an external contact lead, or in the case of series-interconnected modules, to the next cell in the series. (b) An isometric cross-section of an emitter finger, sidewalls, and local BSF finger area. Light (indicated as $h\nu$) enters from the glass side of the cell.

diffusion barrier, n+ emitter (~30 nm, phosphorous 1×10^{20} cm^{-3}), $p-$ absorber (~2 μm, boron 5×10^{16} cm^{-3}), and $p+$ back surface field (BSF, 100 nm, boron 5×10^{19} cm^{-3}). Metallization, also incorporating a light-trapping scheme, begins with the sputtering of a SiO_2 film onto the device, which after combining with an Al layer, acts as a back surface reflector (BSR). Photolithography and a wet etch are used to pattern small (~30 μm diameter, ~150 μm spacing) holes into the SiO_2. An Al film (~1 μm thick) is then deposited via thermal evaporation over the entire device, which later forms the BSF finger and busbar features. Photolithography is used again to define the location of the emitter fingers and busbars, and a phosphoric etch, with the remaining photoresist acting as an etching mask, is used to remove Al from the BSF where emitter features are desired. Exposed SiO_2 remaining on top of the silicon film is removed by a wet etch. The sample then undergoes a dry-etching process in an SF_6 plasma, where the exposed silicon is removed until only glass is remaining. A second Al film is evaporated onto the sample, which forms emitter fingers and busbars. The excess Al that does not contribute to the emitter features as well as the underlying photoresist is removed via liftoff with acetone. The final cell structure is shown in Figures 1 and 2. Figure 1(a) shows the final top-down cell structure with the interdigitated "comb-like" emitter and BSF fingers present. Figure 1(b) shows an isometric cross-section schematic of the region near the emitter finger-BSF finger interface.

Figure 2 shows a focused-ion beam (FIB) cross-sectional image of the sidewall interface between emitter and BSF fingers, roughly corresponding to the right-hand side of Figure 1(b). To create the image, a trench has been milled into the sample and the sample has been tilted 45° so as to view a cross-section of the sidewall. Note that light enters from the glass-side of the device (i.e., in a superstrate configuration). The width and shape of the sidewall (in Figure 2, approximately 4 μm) can be regulated via varying the phosphoric etch and plasma etch conditions, although further details to do with the interdigitated metallization process are beyond the scope of this paper.

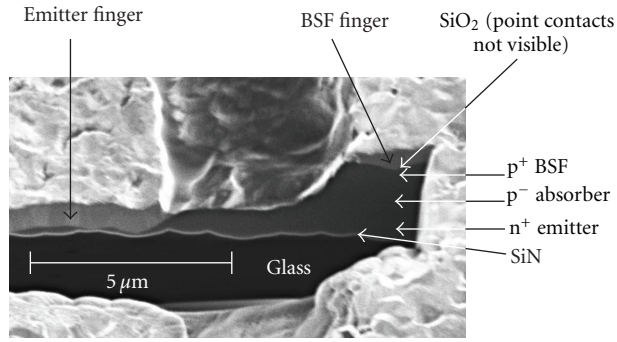

Figure 2: A focused-ion beam (FIB) image of the sidewall cross-section located at the emitter finger-BSF finger interface. A trench has been etched into the cell, and the sample tilted 45° to view the cross-section.

3. Theory

The main differences between this scheme and other interdigitated schemes found in literature are (i) that of the emitter features which lie within the etched grooves of removed silicon, resulting in shadow losses, (ii) the glass superstrate configuration, where light enters from the glass-side of the cell, and (iii) the presence of both emitter and BSF

busbars on the same surface for transferring current to an external contact lead.

There are a number of ways in which power losses due to the metallization can be analyzed and optimized, including the method of "virtual smearing" [7], via the minimization of voltage drops [8], and by maximizing yearly output rather than standard test condition efficiency [9]. However, the applicability of the above approaches for determining power losses in poly-Si on glass devices is limited as they are intended for screen-printed wafer-based solar cell technologies. In this paper, an approach based on the unit cell given by Serreze [10], later summarized by Green [11], will be used. This is required due to the nature of the poly-Si on glass technology, silicon being removed to form an emitter finger "trench," and the presence of a supporting, insulating glass superstrate. This unit cell approach has the advantage of being easy to modify and apply to simple geometric grid patterns, including nonradial-based interdigitated patterns. However, it should be noted that this approach will underestimate the losses associated with concentrator solar cell applications [12].

Figure 3 shows a sample unit cell within an interdigitated thin-film solar cell. This particular highlighted unit cell may be used for calculating the power losses due to current flow along the emitter finger and along the $n+$ emitter layer (i.e., towards the emitter finger), whilst a larger unit cell will be required to calculate the power loss along the busbars towards the contact leads, for instance.

In essence, the unit cell approach consists of calculating the I^2R power loss due to a particular mechanism by integrating the loss and then dividing it by the total power generated in the relevant unit cell to give a *fractional* power loss. This effectively "normalizes" the power loss to per unit area and allows for a fair comparison of loss mechanisms within the metallization.

Firstly, a modified form of maximum power point current will be incorporated, which will be referred to as flow current, J_F. Consider the extreme case of an interdigitated solar cell with a shadow loss of 50% (i.e., an emitter feature coverage of 50%). Should such a cell have a measured maximum power point current density (J_{MP}) of 25 mA/cm^2, it becomes apparent that the actual current density, or flow current, in the device material is double this, 50 mA/cm^2. The counterbalance, of course, is that, for such a large coverage of emitter features, this current would have on average a significantly shorter distance to travel prior to reaching an emitter finger. The inclusion of flow current, as a separate term from maximum power-point current has two advantages: (i) it allows for the exact power losses for nonoptimized interdigitated metallization patterns to be calculated, which generally have a higher emitter-feature coverage fraction (shadow losses) and (ii) gives a more accurate power loss result for optimized patterns, although this effect is reduced as the pattern's shading fraction approaches 0.

Using the cell parameters defined in Figure 3, the flow current is given by

$$J_F = \frac{J_{MP} CS}{SW_A + B(S - W_F)}, \tag{1}$$

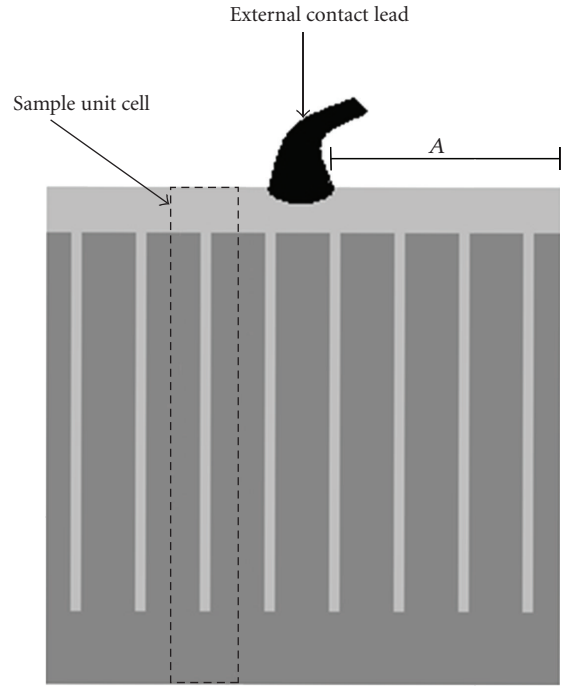

Figure 3: A sample unit cell within an interdigitated thin-film solar cell. The lighter grey areas correspond to emitter (busbar and finger) features, the dark grey areas correspond to BSF features, and the external contact lead is shown in black. A is the distance from the edge of the cell to the external contact lead.

where J_{MP} is the current at the cell's maximum power point and the remaining geometric cell parameters are as given in Figure 4. Alternatively, this equation can be rewritten as $J_F = J_{MP}/(1 - P_{sh})$, where P_{sh} is the fractional shading percentage.

An example derivation for the fractional resistive power loss along the emitter finger is as follows: the resistance in the emitter finger is $dR = (\rho_{s,ef}/W_F)dx$, where $\rho_{s,ef}$ is the sheet resistivity (units commonly $\Omega/\square$) of the emitter fingers and W_F is the finger width.

The current flow at any x along the finger is equal to that of the area bounded by $SW_A(J_F SW_A)$ plus the sum of current generated in the cell to the left and right of the emitter fingers ($J_F x(S - W_F)$). The current is thus $I = J_F x(S - W_F) + J_F(SW_A)$ as x goes from 0 (the tip of the emitter finger) to B, where it joins the emitter busbar.

Integrating to find the sum of power losses along the emitter finger, we have

$$\begin{aligned} P_{L,ef} &= I^2 dR \\ &= \int_0^B [J_F x(S - W_F) + J_F(SW_A)]^2 \frac{\rho_{s,ef}}{W_F} dx \\ &= \frac{B\rho_{s,ef}}{W_F} J_F^2 \left[\frac{1}{3} B^2 (S - W_F)^2 + (SW_A)^2 \right]. \end{aligned} \tag{2}$$

In order to find the fractional power loss, this absolute power loss is divided by the power generated in the unit cell used (here, dimensions of CS as in Figure 3). The power generated

Table 1: Location, loss type, quantified power loss, and unit cell area for the various power loss mechanisms present in interdigitated metallization for poly-Si thin-film solar cells.

Location and loss type	Power loss	Unit cell area
Emitter fingers, resistive loss	$(B\rho_{s,ef}/W_F)J_F^2[(B^2/3)(S-W_F)^2+(SW_A)^2]$	CS
BSF fingers, resistive loss	$(B^3\rho_{s,bf}/3)J_F^2(S-W_F)$	CS
Emitter layer, resistive loss	$(\rho_{s,el}/6)J_F^2[(B/4)(S-W_F)^3+SW_A^3]$	$CS/2$
Emitter busbar, resistive loss	$(A^3/3)J_{MP}^2C^2(\rho_{s,eb}/W_E)$	AC
BSF busbar, resistive loss	$(A^3/3)J_{MP}^2C^2(\rho_{s,ab}/W_A)$	AC
Emitter fingers, shadow loss	$J_{MP}V_{MP}BW_F$	CS
Emitter busbar, shadow loss	$J_{MP}V_{MP}AW_E$	AC

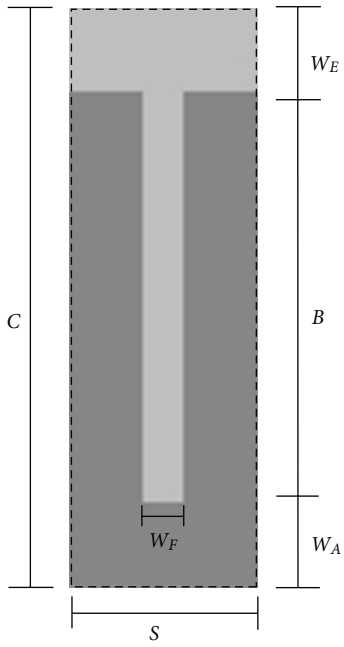

Figure 4: A sample unit cell of an interdigitated thin-film solar cell. C is the total cell width, W_E is the emitter busbar width, B is the emitter/BSF finger length, W_A is the BSF busbar width, S is the (centre-to-centre) emitter finger spacing, and W_F is the emitter finger width.

is thus $J_{MP}V_{MP}CS$, and the fractional resistive power loss along is

$$P_{F,ef}=\frac{B}{CS}\frac{\rho_{s,ef}}{W_F}\frac{J_F^2}{J_{MP}V_{MP}}\left[\frac{B^2}{3}(S-W_F)^2+(SW_A)^2\right]. \quad (3)$$

Derivations generally following the same procedure as above are then carried out for other resistive loss mechanisms in this interdigitated metallization scheme. Shadow power losses are simply proportional to the emitter coverage fraction. The resultant formulae for all power losses derived are given in the next section.

4. Results and Discussion

Tables 1 and 2 show the power losses and fractional power losses, respectively, for the relevant loss mechanisms in the interdigitated metallization. The variables used are as defined in Figures 3 and 4, whilst the various sheet resistivities are linked to their relevant loss type, that is, $\rho_{s,bf}$ for the sheet resistivity of the BSF fingers, $\rho_{s,el}$ for that of the emitter layer, and so on.

Such equations are useful not only to derive the power losses due to metallization of a fabricated cell, but also to produce the optimal interdigitated cell designs. This model can also be used for other thin film on supporting substrate technologies such as CdTe, CIS/CIGS, amorphous (a-Si), and microcrystalline (μc-Si) silicon, provided a similar interdigitated scheme is used.

Cell optimization corresponds to the set of metallization parameters (finger spacing, busbar width, etc.) that produce the minimum total sum of fractional power losses. It is possible to derive analytical solutions for the optimal emitter finger/busbar widths, with some simplifications; for example, by forcing the finger spacing, S, to be constant and using the method of calculus to find the minimum fractional power loss from the sum of the emitter finger resistive and shadow losses. However, due to the large number of interdependencies (the finger spacing, S, e.g., influences six out of the seven loss areas), the only accurate way for optimizing the metallization parameters is through a numerical solving software package, such as Microsoft Excel's Solver tool. By forcing a set of restrictions (minimum finger width, emitter film resistivity, and even cell dimensions), it is possible to solve for the parameters which produce the minimum sum of fractional power losses under a variety of constraints.

Numerically solving for optimized parameters in this way allows for a wide range of graphs relating to optimal parameters and the effect of parameter variation to be generated. Shown below are two example simulations which are of particular interest.

Figure 5 shows the total fractional power loss of an optimal interdigitated pattern as a function of the emitter finger width. For the simulation a cell with an area of 4 cm^2, maximum power-point current density of 25 mA/cm^2 and maximum power point voltage of 400 mV have been used. In addition, the emitter layer sheet resistivity has been set to 400 $\Omega/\square$, which is a typical value for thin-film polycrystalline silicon [13]. Two shaded regions are shown superimposed onto the graph, which correspond to general finger widths routinely achieved with the respective technologies. The large fractional power loss difference between a screen printed

Table 2: Location, loss type, and fractional power loss (i.e., normalized to unit cell area) for the various power loss mechanisms present in interdigitated metallization for poly-Si thin-film solar cells.

Location and loss type	Fractional power loss
Emitter fingers, resistive loss	$(B/CS)(\rho_{s,ef}/W_F)(J_F^2/J_{MP}V_{MP})[(B^2/3)(S-W_F)^2+(SW_A)^2]$
BSF fingers, resistive loss	$(B^3\rho_{s,bf}/3CS)(J_F^2/J_{MP}V_{MP})(S-W_F)$
Emitter layer, resistive loss	$(\rho_{s,el}/3CS)(J_F^2/J_{MP}V_{MP})[(B/4)(S-W_F)^3+SW_A^3]$
Emitter busbar, resistive loss	$(A^2C/3)(J_{MP}/V_{MP})(\rho_{s,eb}/W_E)$
BSF busbar, resistive loss	$(A^2C/3)(J_{MP}/V_{MP})(\rho_{s,ab}/W_A)$
Emitter fingers, shadow loss	BW_F/CS
Emitter busbar, shadow loss	W_E/C

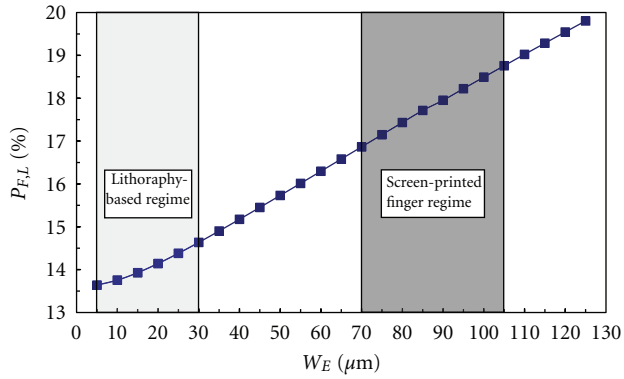

Figure 5: Total fractional (simulated) power loss for an optimized interdigitated thin-film solar cell on glass, as a function of emitter finger width. A cell area of 4 cm^2, maximum power point current density of 25 mA/cm^2, an open-circuit voltage of 400 mV, and an emitter layer sheet resistivity of 400 Ω/□ have been assumed for this example. Shaded overlays of the approximate emitter widths possible with lithography (~5 μm–30 μm) and a screen-printed (~70 μm–110 μm) regime are also included.

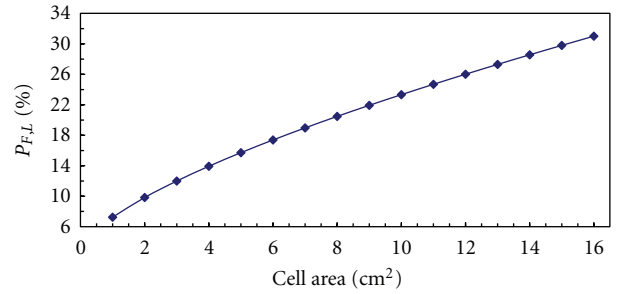

Figure 6: Total fractional (simulated) power loss for an optimized interdigitated thin-film solar cell on glass, as a function of total cell size. The cell dimensions for each cell area datum have also been optimized. A constant minimum emitter finger width of 15 μm, maximum power point current density of 25 mA/cm^2, an open-circuit voltage of 400 mV, and an emitter layer sheet resistivity of 400 Ω/□ have been assumed for this example.

regime (~70 μm fingers, ~16.9% fractional power loss) and a lithography based regime (~10 μm fingers, ~13.8% fractional power loss) highlights the importance of reduced finger widths, particularly with interdigitated schemes for poly-Si thin-film cell applications.

Figure 6 shows the total fraction power loss of an optimized interdigitated pattern as a function of cell size. The cell dimensions have also been individually optimized for each cell area. The width to length ($C:2A$) ratios in this example range from 0.7 to 0.8, although factors such as sheet resistivities and constraints on cell parameters may result in an optimal ratio outside this range. The cell areas used range from 1 cm^2 (i.e., the minimum cell area (1-sun cell) required for inclusion in the solar cell efficiency tables [4]) to 16 cm^2, the largest poly-Si thin-film cell area that can currently be fabricated at the University of NSW.

No one, single power loss mechanism is responsible for the large increase in fractional power losses for larger cell areas. Rather, all losses increase, as can be expected of optimized systems: where one adjusted parameter directly influenced the optimized size or dimensions of another (i.e., larger cell widths require a smaller finger spacing, which corresponds to more fingers per unit cell width and more current flow along each busbar).

The result strongly hints towards the fabrication of series-interconnected, very small area cells (<2 cm^2) to produce high voltage, low current devices as being vital for more efficient thin-film poly-Si minimodules. This is in contrast to the world record 10.5% minimodules reported by CSG Solar (individual cell area 4.7 cm^2) and those currently under investigation in the author's group (4–4.4 cm^2). For large (>1m^2) sized modules of polycrystalline material deposited on glass superstrates, adjusting the individual cell size is a matter regulating the number and location of interconnection points. Measures that aid in the reduction of fractional power losses, including reducing the emitter layer resistivity, fabricating smaller area devices, reducing the *effective* cell length (i.e., distance A in Figure 2) via, for instance, multiple contact leads, and innovative interconnection schemes which do the same, are currently under investigation.

5. Conclusion

A method for quantifying the total and fractional power losses of the interdigitated metallization of poly-Si thin-film solar cells is presented. By numerically minimizing the sum of the fractional power losses present in a metallization

scheme, the optimal grid-pattern can be determined. The importance of reducing both the finger width and total cell size is paramount, and these are two areas where further research and optimization are expected to lead to increased efficiencies of thin-film poly-Si devices.

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