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Research Article

p-Type Quasi-Mono Silicon Solar Cell Fabricated by Ion Implantation

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The p-type quasi-mono wafer is a novel type of silicon material that is processed using a seed directional solidification technique. This material is a promising alternative to traditional high-cost Czochralski (CZ) and float-zone (FZ) material. Here, we evaluate the application of an advanced solar cell process featuring a novel method of ion implantation on p-type quasi-mono silicon wafer. The ion implantation process has simplified the normal industrial process flow by eliminating two process steps: the removal of phosphosilicate glass (PSG) and the junction isolation process that is required after the conventional thermal $POCl_3$ diffusion process. Moreover, the good passivation performance of the ion implantation process improves V_{oc}. Our results show that, after metallization and cofiring, an average cell efficiency of 18.55% can be achieved using 156 × 156 mm p-type quasi-mono silicon wafer. Furthermore, the absolute cell efficiency obtained using this method is 0.47% higher than that for the traditional $POCl_3$ diffusion process.

1. Introduction

The photovoltaic (PV) industry has benefited from the policies of many successive governments that have offered incentives for power projects such as rooftop solar systems. The resulting increase in demand has grown the solar energy market by at least 20% per annum over the past ten years. The final target of the PV industry is the achievement of grid parity, and lowering manufacturing costs and increasing efficiency are very important steps in achieving this target. Reducing silicon bulk thickness and substituting alternative cheap materials are just two options available for lowering the initial cost of materials. In particular, reducing silicon bulk thickness will increase the amount of wafer per ingot or brick, thereby reducing the price per watt. However, this could produce a wafer handling issue, resulting in a higher wafer breakage rate during cell and module processing.

Substituting alternative cheap materials is one solution to reduce cost. Multicrystalline silicon (mc-Si) substrates have traditionally been used in industrial solar cells owing to their relatively low cost, particularly compared to that of Czochralski (CZ) grown monocrystalline material. However, they can suffer from low efficiency due to defects attributed to grain boundaries. In this study, we use a p-type quasi-mono wafer as the starting material. Single-crystal silicon is produced according to a seed directional solidification technique [1] typically used for multicrystalline ingots. The p-type quasi-mono wafer produces higher cell efficiencies than those of multicrystalline silicon material with the same average minority carrier lifetime [1, 2].

Increasing solar cell efficiency will also leverage cost in the solar chain. Solar cell efficiency can be improved by various process methods, including metal-wrap-through (MWT) solar cells [3, 4], emitter-wrap-through (EWT) cells [5, 6], interdigitated backside contact (IBC) cells [7, 8], laser-fired contact cells [9, 10], and ion-implanted cells [11, 12]. Of these methods, ion implantation is one of the most attractive and cost-effective options.

In the present study, we substitute ion implantation for thermal $POCl_3$ diffusion in commercial silicon solar cells,

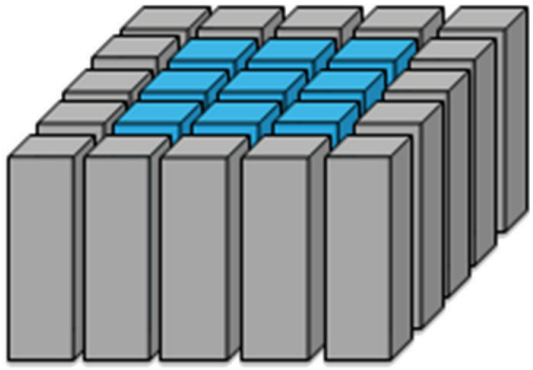

Figure 1: The distribution diagram for the 9 ingots used.

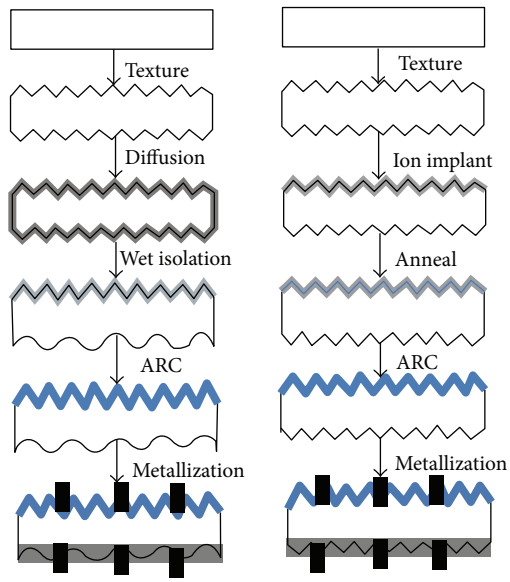

Figure 2: Process flow comparison of conventional and ion-implanted solar cell.

which allows us to eliminate two process steps: (1) phosphosilicate glass (PSG) removal and (2) parasitic junction isolation. In the conventional process, PSG is generated on the surface as a result of the reaction between phosphorous and oxygen during the thermal diffusion step. Accordingly, after thermal $POCl_3$ diffusion, an isolation process is typically required to remove the PSG layer. Moreover, there are two ways to isolate the parasitic junction in the traditional process: wet isolation combined with a PSG clean step and laser isolation. However, both of these isolation processes result in a reduction of the area of the absorption surface; in particular, laser isolation damages the wafer surface and causes lower efficiency.

2. Experiment

Here, we used p-type quasi-mono silicon wafers (GCL-Poly Energy Holdings Limited) with resistivities of 0.5–3 Ωcm, thicknesses of 180–200 μm, and dimensions of 156 × 156 mm. A monocrystalline seed was placed at the bottom of a crucible, and polysilicon was then loaded on top of the seed. The underlying seed allowed quasi-mono silicon ingots to grow in the DS furnace. We selected 9 ingots from the center of the brick for use as starting material. These 9 ingots had more than 90% of their area oriented in the ⟨100⟩ direction and less than 10% in other directions. We sliced the 9 ingots into wafers. Figure 1 illustrates the distribution of these 9 ingots within the brick. Figure 2 presents a comparison of the process flow for conventional thermal $POCl_3$ diffusion with that for ion implantation on quasi-mono silicon wafers. Because the ⟨100⟩ crystalline area constituted more than 90% of ingot area, an alkaline texturing method was used, and processing was conducted using a Rena alkaline machine. First, a saw damage removal step was required in order to reduce surface stress caused by the wire saw used. Wafers were dipped in a batch type system with Teflon material with a high KOH concentration (5.04 wt%) without IPA solution mixing for the saw damage removal process step. Then, anisotropic etching with a KOH : IPA : H_2O volume ratio of 1 : 1.6 : 34 was conducted to produce pyramids on the surface to absorb incoming light and increase the light path in the silicon bulk. In the commercial process, the next step would typically be thermal $POCl_3$ diffusion to form a p-n junction. Here, a diffusion furnace (Tempress Systems, The Netherlands) was used to perform thermal $POCl_3$ diffusion. Also, 400 wafers were placed vertically into a quartz boat; then, the boat was moved into a quartz tube and heated to 840°C. The dopant gas reacted with the silicon surface in the presence of O_2 at high temperature, with the following reactions taking place:

$$POCl_3 + O_2 \longrightarrow P_2O_5 + Cl_2 \quad (1)$$

$$P_2O_5 + Si \longrightarrow SiO_2 + P \quad (2)$$

In the ion implantation process, an inline high-throughput machine (>1000 pcs/hr) from Varian Semiconductor Equipment Associates (VSEA) was used to perform ion implantation. Ion dopant bombarded the wafer surface, subsequently penetrating into the wafer. We selected PH_3 gas as the P^+ ion source for implantation on the surface, with a low beam energy of 10 keV and a dose of 3.0×10^{15} P^+/cm^2. However, crystal damage occurred during the ion bombardment procedure. Inclusion of a high-temperature annealing process step can recover this damage. A furnace tube from Tempress Systems was used for thermal annealing. In the annealing step, wafers were placed vertically into a quartz boat, and the boat was moved into a quartz tube. Dry oxide (O_2) was passed into the tube, activating the dopant. Simultaneously, a thinner silicon oxide formed on the wafer surface according to the following reaction:

$$Si + O_2 \longrightarrow SiO_2 \quad (3)$$

The dry oxide annealing step was conducted to activate the dopant and fabricate the junction. After annealing, the dopant concentration profile was different from that for $POCl_3$ diffusion [13–16]. According to previous studies, the doping concentration profile of $POCl_3$ typically ranges from

Figure 3: The appearance of quasi-mono silicon after texturing.

an error function complement (erfc) to a Gaussian distribution, with the peak dopant concentration occurring at the surface. Conversely, the profile for ion implantation occurs at a specific depth below the surface. Detailed discussions of these profiles can be found in previous studies [13–16].

After emitter formation, an isolation process was conducted to remove the parasitic junction caused by $POCl_3$ diffusion during the industrial process flow. A chemical isolation process was performed with an inline roller type transportation system using the InOxSide instrument from Rena GmbH. In this process step, the parasitic junction was removed in an etching bath with $H_2O : HF : HNO_3 : H_2SO_4$ volume ratio of 19 : 2 : 11 : 8.

After the isolation/annealing step, SiN_x layer was applied to act as an antireflection coating (ARC). Wafers were automatically placed into a batch type system machine from Centrotherm, and the layer was applied by direct plasma deposition. The SiN_x layer not only absorbs more light into silicon, but also passivates the silicon surface. Moreover, the thickness of silicon nitride used in the implantation process in the present study was thinner than that for the conventional $POCl_3$ process owing to the thinner silicon oxide layer formed on the wafer surface during the annealing step in the ion implantation process.

After ARC deposition, a metal contact was formed by a Baccini belt type screen printing system and a Despatch cofiring system. During the screen printing process, frontside silver (Ag) paste, Dupont 17F, was printed on the frontside surface to form three bus bars and 83 finger lines. Dupont PV-157 was used as the backside Ag paste and Monocrystal RX-1203 as the backside aluminum (Al) paste.

Berger Lichttechnik single-pulse solar simulators were used to measure the basic parameters and I-V curves of cells under standard test conditions (STCs): irradiance of 1000 W/m^2, the AM 1.5 solar spectrum, and temperature of 25°C. Electrical characteristics (including V_{oc}, I_{sc}, FF, P_{max}, and cell efficiency) were obtained from the I-V curves. The shunt resistance R_{sh} was determined from the linear slope of the reverse dark current for each cell. The series resistance R_s was calculated from two I-V curves measured at 1000 W/m^2 and 500 W/m^2, according to IEC 891.

3. Results and Discussion

Here, we textured 2000 samples of p-type quasi-mono silicon simultaneously. Figure 3 shows the appearance of the quasi-mono silicon after texturing, illustrating the many different grains that appear on the surface. Figure 4 illustrates the pyramid topology revealed at different locations within the wafer for 30x (Figure 4(a)) and 550x (Figure 4(b)) SEM at the upper right of the wafer. Three different pyramid orientations are shown. Figures 4(c) and 4(d) also illustrate the pyramid topology for 95x and 350x SEM at the upper right of the wafer, respectively; these are clearly different from Figures 4(a) and 4(b). The figure indicates that quasi-mono silicon wafer exhibits a planar area after alkaline texturing. Figures 4(e) and 4(f) illustrate the pyramid topology for 30x and 550x SEM at the upper left of the wafer and indicate that scrapes have appeared on the quasi-mono silicon wafer. Such differences in topology can be seen clearly after alkaline texturing and are likely due to differences in grain boundaries.

After texturing, a Hitachi U-4100 UV-Vis-NIR spectrophotometer was used to measure the reflection. U-4100 has two light sources that can measure reflection at wavelengths of 240–2600 nm and an integrating sphere that can measure textured wafer. We selected 4 wafers randomly from each group and measured 5 points at 5 different locations within each wafer. Figure 5 illustrates a comparison of the reflection from these different locations after the alkaline texturing process.

As the figure shows, there are small differences in reflections between locations. This is likely due to the different pyramid topologies caused by different grain boundaries. To quantify the performance, we calculated the weighted reflectance R_w% based on a previously published study [17] as follows:

$$R_w\% = \frac{\int_{\lambda 1}^{\lambda 2} F_i(\lambda)\, Q_i(\lambda)\, R(\lambda)\, d\lambda}{\int_{\lambda 1}^{\lambda 2} F_i(\lambda)\, Q_i(\lambda)\, d\lambda}, \quad (4)$$

where $F_i(\lambda)$ is the photon flux and $Q_i(\lambda)$ is the cell internal quantum efficiency [18, 19]. Table 1 presents a comparison of R_w% for 5 different locations within the wafers and indicates that R_w% is highest for the upper right location at 13.92%. This corresponds to an area with a shiny appearance caused by a different pyramid orientation and planar topology. Conversely, the lowest R_w% (12.94%) was found for the center location and is thought to be due to the single-crystalline structure in the center.

After texturing, the next step in the ion implantation process was ion implantation itself. For this, 1600 wafers were automatically transferred into the chamber, and P^+ ion sources were implanted onto the wafer surface from the ion source. Then, we divided the 1600 wafers into 4 groups, each with 400 wafers.

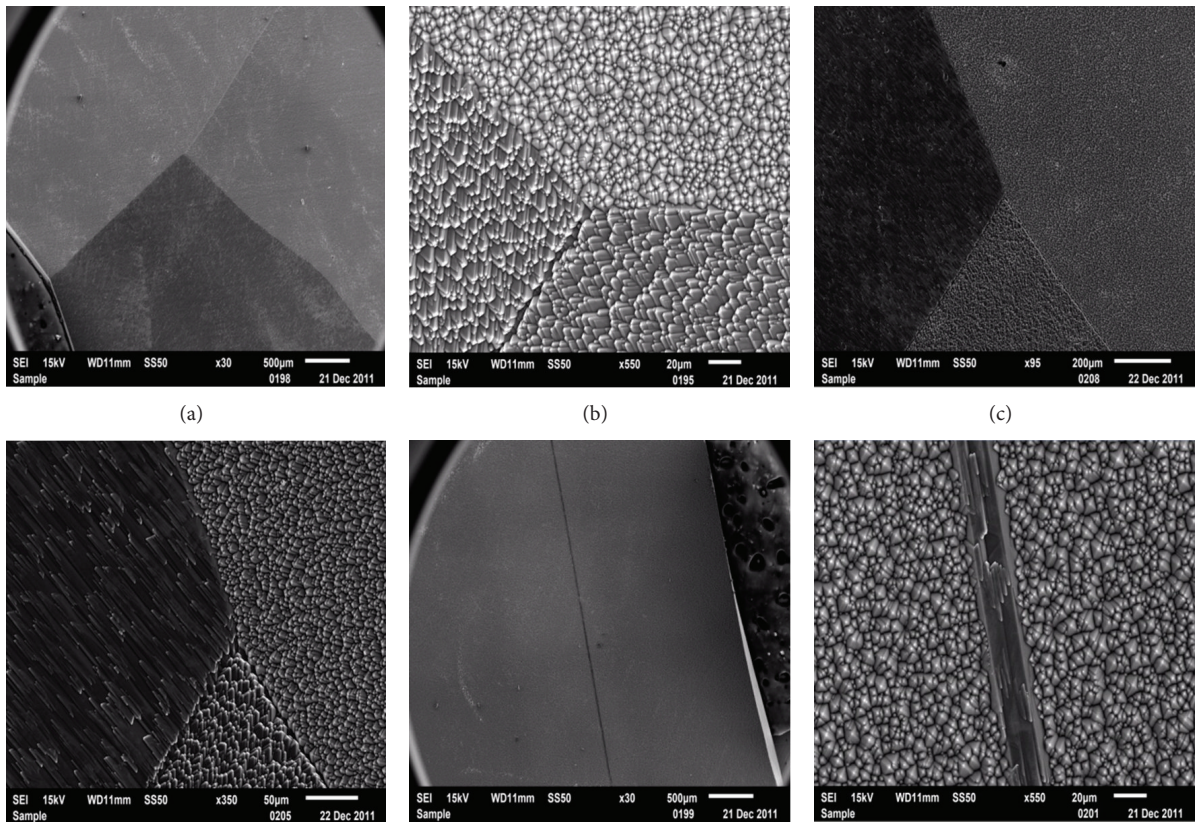

Figure 4: The pyramid topology shown by SEM at different locations within the wafer.

Table 1: Comparison of R_w% of five different locations within the wafer.

Location	Centre	Upper right	Lower right	Upper left	Lower left
R_w%	12.94	13.92	13.88	13.87	13.71

Table 2: Comparison of R_{sheet} and uniformity between $POCl_3$ diffusion and 4 different anneal processes.

R_{sheet} (ohm/sq)	Ave	MAX	MIN	Uniformity
$POCL_3$	64.68	67.53	61.32	4.80%
Anneal_810	70.02	73.08	68.96	2.94%
Anneal_840	65.47	67.14	63.31	2.93%
Anneal_870	61.39	63.07	59.65	2.79%
Anneal_900	57.13	59.41	56.98	2.13%

These 4 groups were processed at peak temperatures of 810, 840, 870, and 900°C during the subsequent annealing step. A four-point probe was used to measure the sheet resistance (R_{sheet}). Table 2 presents a comparison of R_{sheet} and uniformity for $POCl_3$ diffusion and the 4 different annealing processes; in particular, the table indicates that R_{sheet} decreased when the peak temperature was 810–900°C and the baseline R_{sheet} for the $POCl_3$ diffusion process was 64.68 Ω/sq. The R_{sheet} uniformity for thermal $POCl_3$ diffusion was 4.80%, which was worse than that for the implantation process. In fact, the uniformity of the implantation process was below 3%, likely owing to the precise

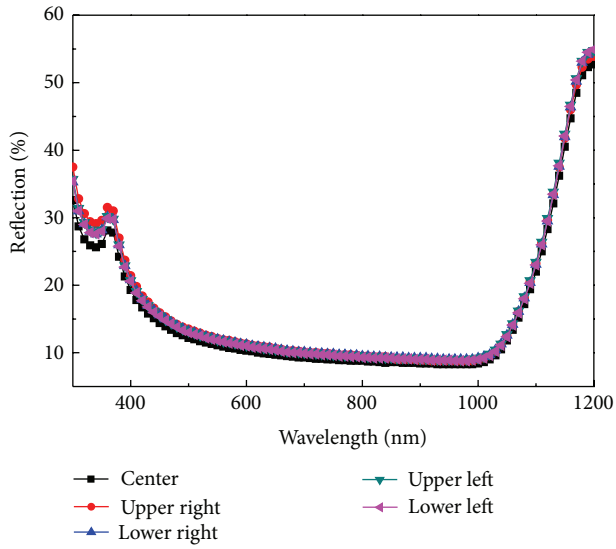

Figure 5: A comparison of the reflection at five different locations within the wafers after the alkaline texturing process.

control exercised over the dose amount by the emitter in the ion implantation apparatus. The good R_{sheet} uniformity and precise control also enabled a repeatable process for fabrication of lightly doped emitter regions [20–22].

In order to obtain the best performance from the annealing step, 5 p-type quasi-mono wafers, implanted with 2.0×10^{15} dopant ions at a beam energy of 10 keV on both faces of the wafer, were used to monitor the implied V_{oc} and carrier lifetime [23] for each condition. The WCT-120 tool from Sinton Instruments uses a quasi-steady-state photoconductance (QSSPC) method to measure implied V_{oc} and lifetime [24]. Table 3 presents the average implied V_{oc} and lifetime for each condition. The implied V_{oc} for wafers doped by thermal $POCl_3$ diffusion was found to be 0.625 V at 1 sun. However, the implied V_{oc} after high-temperature annealing at 900°C was 0.620 V, the worst among all conditions studied. This was likely because high-temperature annealing can degrade the lifetime and reduce the V_{oc}. When the annealing temperature was decreased to 840°C, the implied V_{oc} reached 0.640 V; this higher implied V_{oc} was likely due to better surface passivation.

In the annealing step, a thinner SiO_2 layer was grown on the wafer surface, and the ion-implanted dopant was activated. The thickness of the SiO_2 was measured by a SemiLab LE-100PV ellipsometer. A single laser wavelength from a 632.8 nm He-Ne laser incident on the wafer surface was used to measure the refractive index and thickness of the dielectric layer. In this study, the ⟨111⟩ silicon polished wafer with a dose of 3.2×10^{15} implanted and a beam energy of 10 keV on its surface was used as the control wafer. During the annealing process, control wafers were processed simultaneously with the experimental p-type quasi-mono silicon wafers in the same tube. Table 4 shows the resulting SiO_2 thickness and uniformity for each condition. The thickness of SiO_2 was found to be around 17 nm and was very similar for all the different conditions. Moreover, the uniformity of SiO_2 was improved at higher annealing temperatures, and we found good SiO_2 thickness uniformity (below 1.3% for each annealing condition).

After the junction formation step, SiN_x was deposited on the silicon surface by PECVD. In contrast to the industrial process, the thickness of the silicon nitride must be modulated during this process owing to the thinner oxide on the surface. In order to minimize the reflection from the frontside of the cell, a 57 nm SiN_x layer was deposited on top of the SiO_2. We selected 4 wafers for each condition after the ARC process and measured 5 points at different ⟨100⟩ locations within each p-type quasi-mono wafer. Figure 6 illustrates the comparison of average reflection between $POCl_3$ diffusion and the ion implantation process after deposition of the ARC. At short wavelengths, the reflection from samples treated by $POCl_3$ diffusion was lower than that of samples treated by ion implantation. According to the Schuster diagram [25], the optimum refractive index of the inner n_1 and outer n_2 layers of the silicon substrate can be calculated as follows for zero reflection:

$$\frac{AB}{CD} > 0, \tag{5}$$

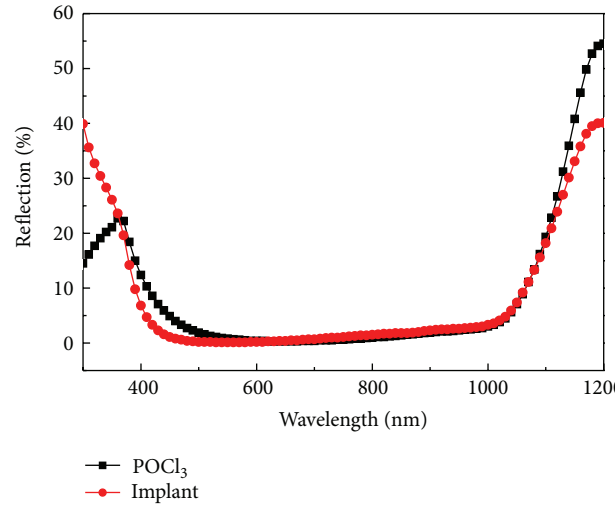

Figure 6: The average reflection for the $POCl_3$ diffusion and implantation process after SiN_x deposition.

where

$$A = n_o - n_s, \quad B = n_o n_2^2 - n_s n_1^2,$$
$$C = n_o n_s - n_2^2, \quad D = n_1^2 - n_s n_o. \tag{6}$$

As explained previously, based on detailed calculations [25], better optical performance can be achieved by using a low-high refractive index design, in which the outer layer has a low refractive index and the inner layer has a high refractive index, on the silicon substrate. However, the design of the ARC in our ion implantation process displayed the opposite characteristics; the outer SiN_x and inner SiO_2 layers had refractive indexes of 2.03 and 1.46, respectively. Such high-low design tends to cause higher reflection at short wavelengths. In the long-wavelength range, the reflection following implantation was lower than that following $POCl_3$ diffusion, because the wafer had a planar backside surface owing to the wet chemical isolation process that used HNO_3 and HF to remove the backside p-n junction after $POCl_3$ diffusion. Table 5 presents a comparison of R_w% between $POCl_3$ diffusion and ion implantation after SiN_x deposition. It is clear that R_w% resulting from implantation was 4.64%, which is better than that from the $POCl_3$ process (which was 5.51% after deposition of the ARC).

After ARC deposition, the wafers were subjected to screen printing and cofiring processes. Figure 7 illustrates a comparison of V_{oc} and I_{sc} between $POCl_3$ diffusion and the implantation process for each condition and indicates that higher annealing temperatures resulted in lower V_{oc} and I_{sc}. The V_{oc} for the implantation process with an annealing temperature of 900°C was the lowest of all, likely because high-temperature annealing can degrade carrier lifetime and V_{oc}; this is in accordance with the results of the WCT-120 measurements. Based on the heavy doping produced by high-temperature annealing, I_{sc} was lowest following high-temperature annealing at 900°C. When the annealing temperature was reduced to 870°C, V_{oc} reached 0.623 V,

Table 3: Implied V_{oc} and lifetime.

	$POCl_3$	Anneal_900	Anneal_870	Anneal_840	Anneal_810
Implied V_{oc} (V)	0.625	0.620	0.624	0.64	0.638
Lifetime (μs)	30.24	24.67	29.43	53.44	50.73

Table 4: The results of SiO_2 thickness and uniformity.

	$POCl_3$	Anneal_900	Anneal_870	Anneal_840	Anneal_810
SiO_2 thickness (nm)	x	17.63	17.56	17.21	17.02
Uniformity (%)	x	0.81%	0.92%	1.05%	1.21%

Table 5: Comparison of R_w% between $POCl_3$ diffusion and implantation after ARC deposition.

	$POCl_3$	Implant
R_w%	5.51%	4.64%

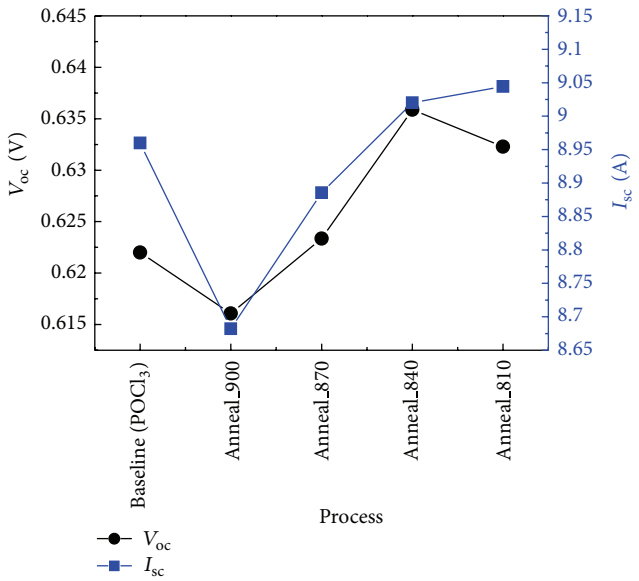

Figure 7: V_{oc} and I_{sc} for the $POCl_3$ diffusion and implantation processes.

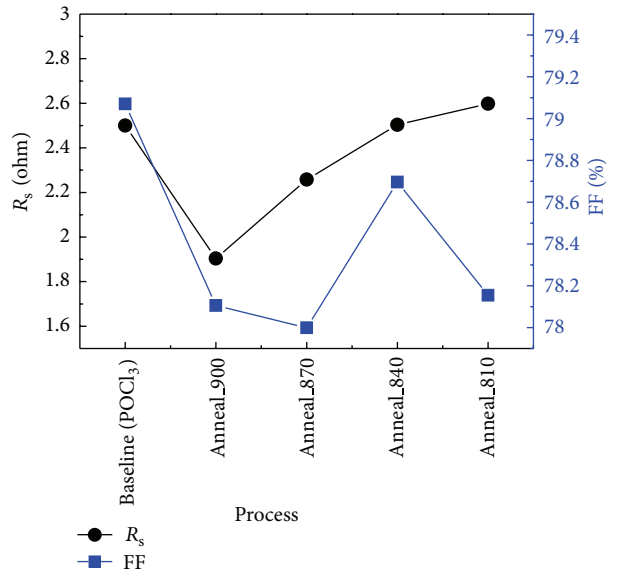

Figure 8: R_s and FF for the $POCl_3$ diffusion and implantation processes.

which was higher than that for the $POCl_3$ diffusion process. However, I_{sc} was still lower than that for $POCl_3$diffusion owing to the lower R_{sheet} of 61.36 Ω/sq. As the annealing temperature reached 840°C, V_{oc} reached its highest value of 0.636 V. As shown in Figure 8, R_s was highest for the implantation process with an annealing temperature of 810°C, likely because the highest sheet resistance (70.02 Ω/sq) would have produced the worst metal contact. Besides the condition of annealing temperature at 810°C, the R_s of the implantation process is lower than that of $POCl_3$ diffusion process. This was likely due to good R_{sheet} uniformity caused by precise doping control by the ion implantation instrument. Moreover, higher annealing temperatures can achieve heavy doping and result in good contact with metal. As shown in Figure 9, the higher annealing temperature also caused a lower R_{shunt}, because a higher annealing temperature degrades the bulk lifetime, which lowers R_{shunt}. The FF of the implantation process was highest for an annealing temperature of 840°C owing to the lower R_s and higher R_{shunt} performances. Moreover, the best average efficiency of 18.55% was found for the implantation process with an annealing temperature of 840°C (Figure 10). All electrical characteristics are presented in Table 6. In general, higher efficiency was found to result from higher V_{oc} and I_{sc}. Therefore, our results indicate that quasi-mono silicon wafer produced by ion implantation can improve photovoltaic cell efficiency. Table 7 presents the cell conversion cost per watt for traditional and implant processes for the quasi-mono wafer substrate. It is clear that the cost of the traditional process (0.1664 USD) was much higher than that of the implant process (0.1617 USD).

4. Conclusions

In this study, we investigated a novel type of silicon material, the quasi-mono wafer, for use in high-efficiency solar cells. We produced this material by ion-implanted emitter formation and were able to raise the absolute cell efficiency of a

Table 6: Characteristics of $POCl_3$ diffusion and implantation processes.

	U_{oc}	I_{sc}	R_s	R_{sh}	FF	N_{Cell}	I_{revl}
Baseline ($POCl_3$)	0.622	8.96	2.50	756	79.07	18.08	0.03
Anneal_900	0.616	8.68	1.90	59.82	78.11	17.17	0.47
Anneal_870	0.623	8.89	2.26	42.71	78.00	17.76	0.65
Anneal_840	0.636	9.02	2.50	86.34	78.70	18.55	0.52
Anneal_810	0.632	9.04	2.60	83.43	78.15	18.37	0.55

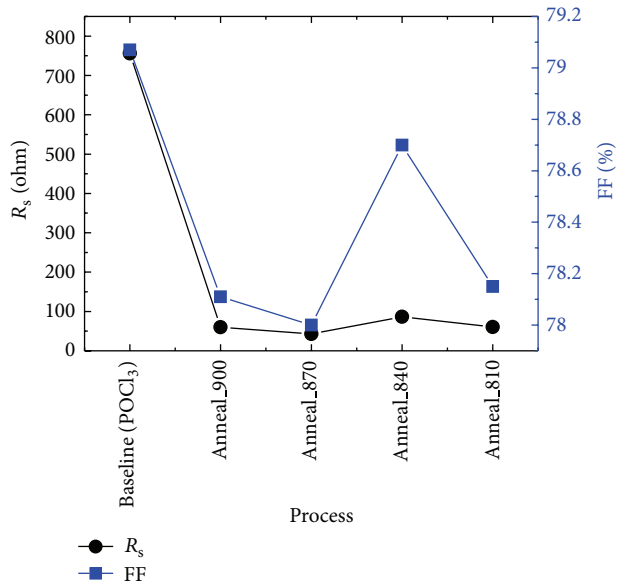

Figure 9: R_{shunt} and FF for the $POCl_3$ diffusion and implantation processes.

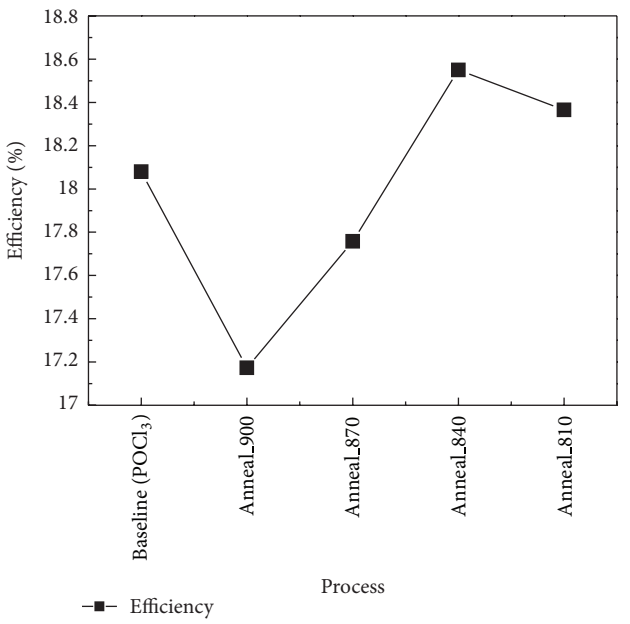

Figure 10: Efficiency for the $POCl_3$ diffusion and implantation processes.

Table 7: The cell conversion cost per watt of traditional and implant processes on quasi-mono wafer substrate.

Station/process	Traditional process	Implant process
Texturing (USD)	0.07	0.07
Implant (USD)		0.08
Anneal (USD)		0.05
Diffusion (USD)	0.068	
PSG clean (USD)	0.033	
Wet isolation (USD)	0.036	
SiN (USD)	0.075	0.08
Screen printing (USD)	0.45	0.45
Conversion cost (USD)	0.732	0.73
Cell efficiency (%)	18.08%	18.55%
Wafer area (m^2)	0.024336	0.024336
Watts/wafer	4.40	4.51
Cell conversion cost Per watt (USD)	0.1664	0.1617

quasi-mono silicon wafer by 0.47% by following a simplified process flow that eliminates the PSG strip and junction isolation steps. The R_{sheet} uniformity from implantation was found to be better than that from the $POCl_3$ diffusion process owing to the precise dopant control exercised by the ion implantation instrument. After activation by an annealing process, the implied V_{oc} from the implantation process with an annealing temperature less than 900°C was found to be better than that from the $POCl_3$ diffusion process; this was likely due to the good surface passivation caused by the implantation and annealing processes. However, owing to the thinner SiO_2 formed on the surface by the annealing process, the thickness of the silicon nitride should be modified to minimize R_w%. After metallization, we achieved an average cell efficiency of 18.55%.

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