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Research Article

Influence of Surface Morphology on the Effective Lifetime and Performance of Silicon Heterojunction Solar Cell

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Different etching times are used to etch silicon wafers. Effects of surface morphology on wafer minority carrier lifetime, passivation quality, and heterojunction solar cell (HJ) performance are investigated. The numbers of mountains and valleys, defined as turning points, on wafer surfaces are used to explain the minority carrier lifetime variations. For a wafer with a smaller amount of turning points, hydrogenated amorphous silicon (a-Si:H) passivation quality can be comparable to ideal iodine-ethanol solution passivation. If the wafer has a notable amount of turning points, the carrier lifetime decreases as the a-Si:H layer will not be able to be well-deposited on turning points. Furthermore, the PC1D simulation indicates that an optimal device conversion efficiency of 21.94% can be achieved at an etching time of 60 min, where a best combination of short-circuit current and open-circuit voltage is obtained.

1. Introduction

In recent years, heterojunction (HJ) silicon solar cells have been drawing increasing attention owing to their high conversion efficiency (up to 24.7%) [1–3], low fabrication temperature [4], low temperature-conversion efficiency dependence [5], and shorter fabrication time. The HJ cells make use of the large band gap of hydrogenated amorphous silicon (a-Si:H) as an emitter with silicon wafer, and the electrons or holes can move in one direction only due to the large band offset. However, dangling bonds on the wafer surfaces serve as recombination centers for the carriers. Such recombination losses will mainly affect the device open-circuit voltage (V_{oc}), the resistance losses that affect the fill factor (FF), and the optical losses which have direct impact to the short-circuit current density (J_{sc}). Several improvements have been reported. One of the most important approaches is the insertion of intrinsic (i-) a-Si:H at the interface between a-Si:H emitter and wafer to passive dangling bonds on wafer surfaces, thus reducing recombination losses [6]. Another concern is the reflection losses at the front surface due to the large refractive index of a-Si:H. To reduce the optical losses two practical methods have been used, (i) using an antireflection coating [7] and (ii) texturing the wafer surface [8–10]. Currently, wet etching by an alkaline solution is the standard process for industrial solar cell texturing. The most widely used etching solution is a low concentration potassium hydroxide (KOH) or sodium hydroxide (NaOH) solution in water with the addition of isopropyl alcohol (IPA) to achieve good lateral uniformity of pyramidal structures across the Si wafer surface by modifying the surface wettability [11, 12]. The wet etching process not only roughens wafer surfaces but also removes sawing damage simultaneously. However, only few groups have achieved high efficiency HJ solar cells [13, 14] because the wet etching texturization can have significant influences on carrier lifetime. Iencinella et al. [15] reported

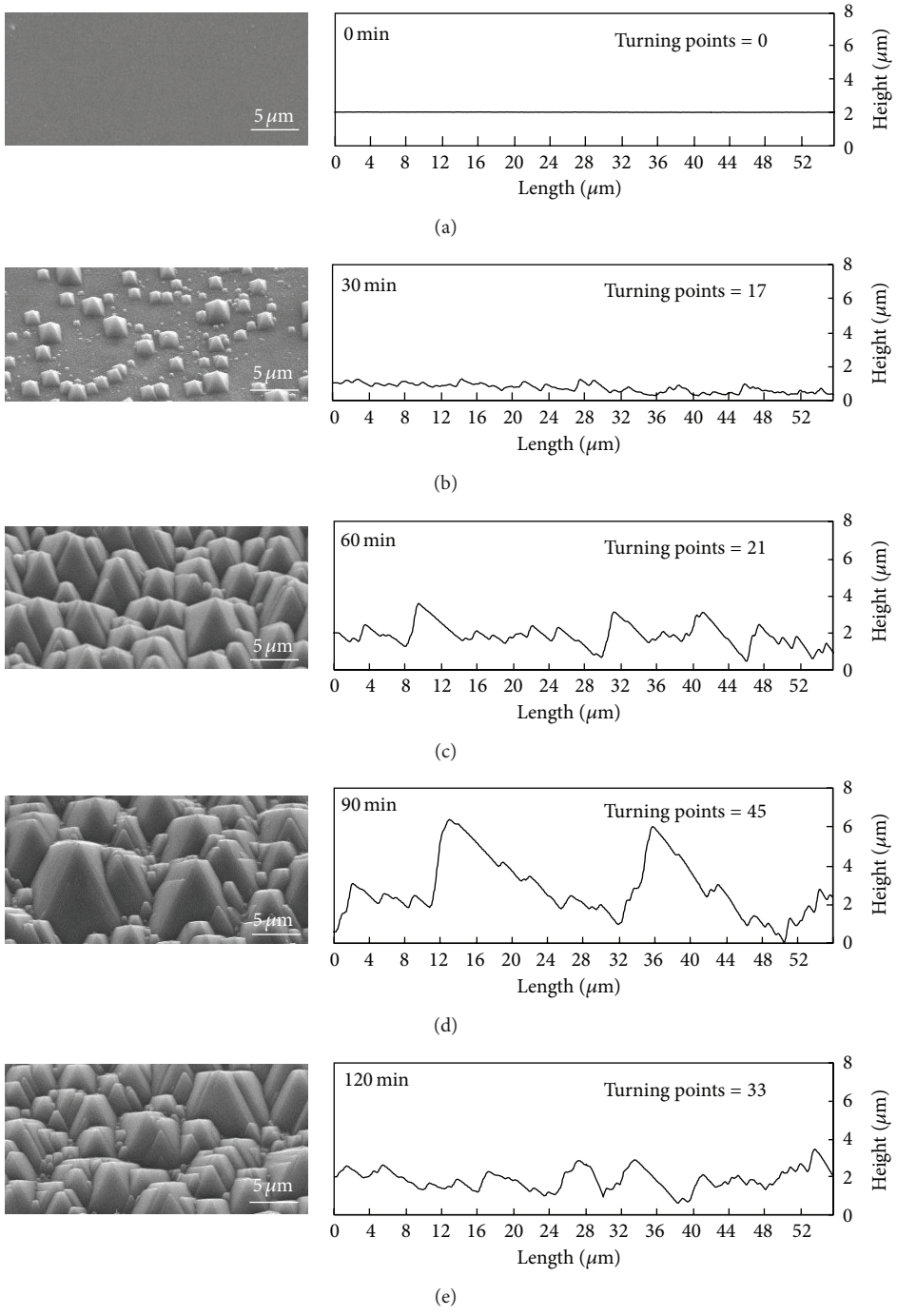

Figure 1: The SEM micrographs and corresponding surface profiles for the wafers with an etching time of (a) 0, (b) 30, (c) 60, (d) 90, and (e) 120 min.

that the K^+ and Na^+ released from etching solutions are extremely fast-diffusing alkali metal ions that can possibly cause contamination of wafers and limit carrier lifetime. Furthermore, IPA is highly volatile so that its fraction in the etching solution is not easy to remain constant. Several methods have been proposed in an attempt to improve the texturization. Stegemann et al. and Kegel et al. [16, 17] indicated that a-Si:H/c-Si solar cells fabricated on IPA-free textured wafers conversion efficiencies above 20% were achieved by quantitative evaluation and optimization of the texture and interface passivation. Deligiannis et al. [18] used repeated cycles of nitride acid oxidation procedure to remove contamination and nanoscale roughness on the facets of pyramidal structures to improve passivation quality. Li et al. [19] used NaClO to produce smaller pyramids than that created by KOH or NaOH, and the small pyramids can lead to

better coverage and contact between a-Si:H and wafer. Some groups also used dry etching techniques [20], but so far they have no reports of a HJ solar cell with a conversion efficiency higher than 17%.

In this study, we adopt industrial standard texturization using KOH and IPA mixed solution. Different etching times are used to etch silicon wafers so as to remove saw damage and produce rough surfaces. The impact of etching times and resultant surface morphologies on carrier lifetime and surface passivation quality are investigated. Furthermore, simulation was carried out to evaluate the cell characteristics.

2. Experimental

Single polished, p-type, ⟨100⟩ single-crystal silicon wafers with thickness of 250 μm, resistivity of 1–10 Ω-cm, and area of $15.6 \times 15.6\,\text{cm}^2$ were used as substrates. Wafers were cleaned and then dipped in a 2% HF solution for 30 s to remove native oxide, prior to the etching process. Pyramidal texturization was carried out in a 5 wt.% KOH solution with 2 wt.% IPA at 85°C for different etching time (from 0 to 120 min). The alkaline solution can cause pyramidal structures on the wafer surface because of the difference in etching rates of (100) and (111) planes. The involved chemical reactions can be found in [21]. During etching, hydrogen bubbles are created, and IPA is used for removal of the bubbles, so that the better lateral uniformity of the pyramids across the wafer surface can be achieved. After etching, an RCA2 clean, consisting of a solution of $6:1:1\ H_2O:HCl:H_2O_2$, was performed at 80°C for 5 min to remove metal ions that might possibly remain on the wafer surface. The passivation of the wafer surface dangling bonds was done by two methods, iodine-ethanol solution passivation and a-Si:H passivation. The a-Si:H was deposited by PECVD, and the detailed deposition conditions can be found in [22].

For HJ solar cell simulation, the device structure was indium tin oxide (ITO)/(n) a-Si/(i) a-Si/(p) c-Si/Al back surface field (Al-BSF). The main properties of the layers in the device structure were obtained by experimental characterization of each layer. The (i) and (n) a-Si:H thicknesses were 5 and 10 nm, respectively. ITO film with a thickness of 90 nm was deposited using electron-gun evaporation in order to enhance the lateral conductivity and minimize reflection losses. Al film with a thickness of 5 μm was sputtered on the wafer backside and annealed at 800°C for 30 s.

The film thickness was evaluated by using an alpha-step profiler. The wafer minority carrier lifetime was measured using quasi-steady-state photoconductance (QSSPC) system. The texture morphologies were observed by scanning electron microscopy (SEM) and high resolution transmission electron microscopy (HRTEM).

3. Results and Discussion

Figure 1 shows the SEM micrographs and surface profiles of the wafers etched for 0–120 min. Pyramids are formed as the etching rate in a ⟨100⟩ orientation is far higher than that in a ⟨111⟩ orientation [23, 24]. The pyramids size increases with

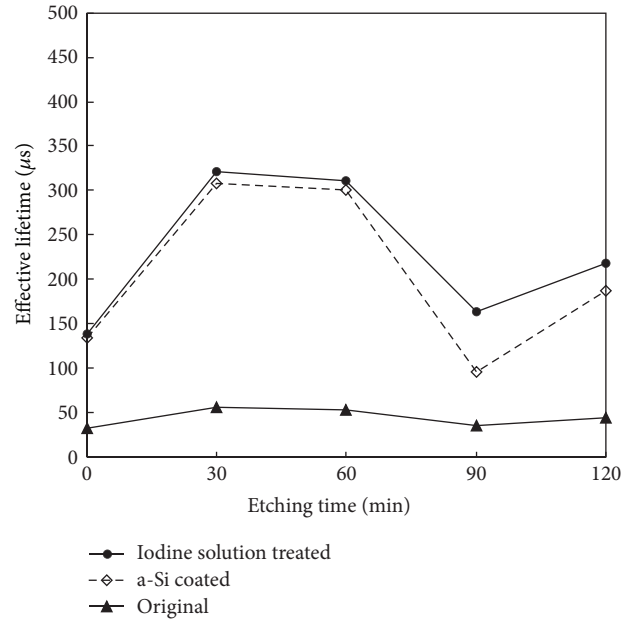

Figure 2: Effective minority carrier lifetime of wafers with different etching time and different passivation methods.

increasing the etching time and seems to reach the maximum at 90 min. Further increasing of the etching time to 120 min leads to overetching which reduces the pyramids size. It is worth noticing that, from the surface profiles, the edges of the pyramids are not smooth but rather contain several smaller subpyramids. We define a "turning point" as the point at the mountain or the valley of a pyramid with a base width larger than 1 μm. The numbers of the counted turning points, which are also labeled in the figure, are 0, 17, 21, 45, and 33 for the wafers etched for 0, 30, 60, 90, and 120 min, respectively. Note that the 90 min etched wafers thus have not only the highest surface roughness but also the largest number of turning points.

Figure 2 shows the carrier lifetime of the wafers with different etching times and passivation methods. In particular, the a-Si:H passivation is compared to the iodine-ethanol solution passivation, which is generally used to evaluate the optimal passivation conditions. It can be seen that, without any passivation, all the carrier lifetimes of the wafers are low, in the range of 25–50 μs, due to high amount of surface dangling bonds. The effect of the etching time is thus covered. Considering the wafers with iodine-ethanol solution passivation, the lifetime is significantly higher than that of the unpassivated wafers and increases from 148 through 325, 321, and 153 to 225 μs when the etching time increases from 0 to 120 min. The low values of the nonetched wafers result from the lack of saw damage removal, while the lifetime variation between the etched wafers could be related to increased surface defect states due to expanded surface area and decreased mobility due to the increased roughness [25]. The lifetimes of the wafers with a-Si:H thin-film passivation are similar to the wafers with iodine-ethanol solution passivation at the etching time of 0, 30,

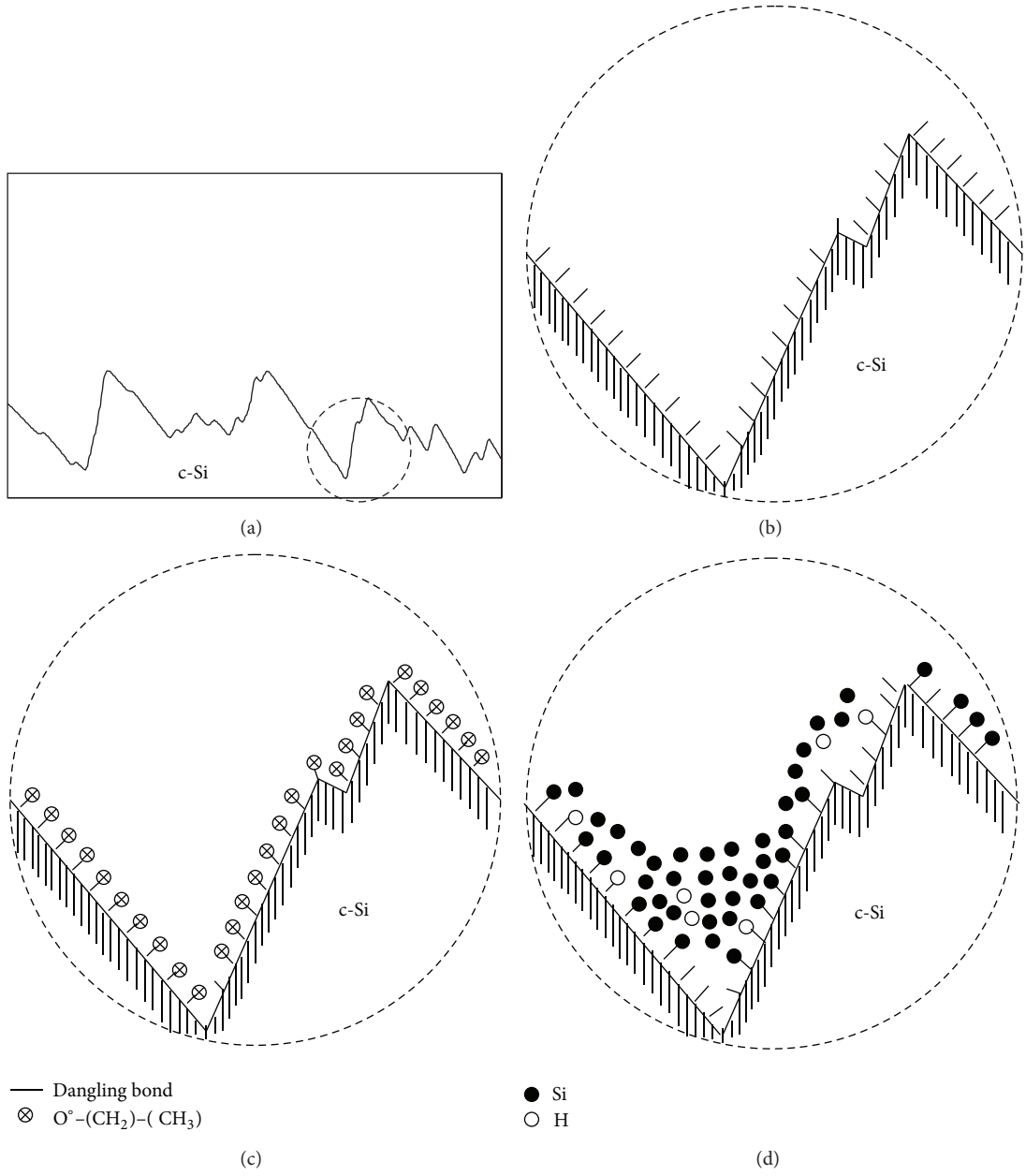

Figure 3: (a) Surface profile of the 90 min etched wafer and schematic diagrams of the wafer surface dangling bonds (b) without passivation, (c) passivated by iodine-ethanol solution and (d) a-Si:H.

and 60 min, and this implies the high passivation quality of our a-Si:H films. Nevertheless, the difference of the lifetimes between the wafers with the two passivation methods at 90 min becomes larger, suggesting a significantly weakened passivation capability of a-Si:H compared to iodine-ethanol solution passivation.

Figure 3 shows schematic diagrams of surface passivation using iodine-ethanol solution and a-Si:H thin-film. As shown in Figure 3(b), a large number of dangling bonds exist on the surface of a wafer. During the iodine-ethanol solution passivation process, the surface dangling bonds (Si°) are removed, according to

$$Si^{\circ} + (OH)\text{–}(CH_2)\text{–}(CH_3) + \frac{1}{2}I_2 \longrightarrow Si\text{–}O\text{–}(CH_2)\text{–}(CH_3) + H^{+} + I^{-} \quad (1)$$

Detailed information can be found in [26]. Since ethanol is liquid phase, it could uniformly contact with wafer surfaces and provide great passivation quality, as shown in Figure 3(c). On the other hand, silicon and hydrogen atoms are solid phase, so that they might irregularly deposit on the wafer surfaces, as is shown in Figure 3(d). The passivation quality especially at the mountain and valley regions is expected to be reduced. In other words, a-Si:H is assumed to have a lower

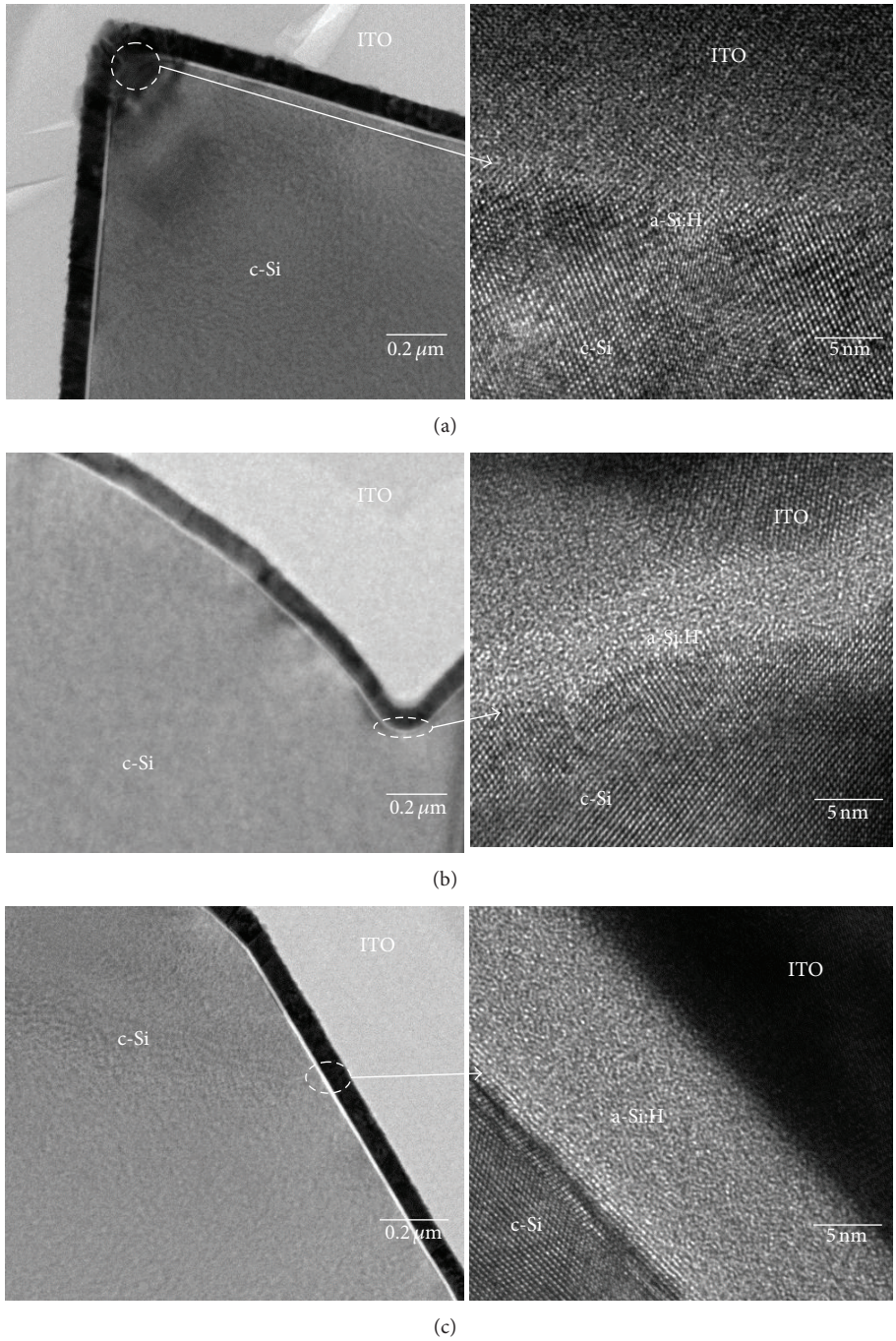

Figure 4: HRTEM cross-sectional micrographs of (a) peak, (b) valley, and (c) hillside of a pyramid of the 90 min etched wafer passivated by a-Si:H.

passivation capability for a wafer having more mountains or valleys (i.e., more turning points). Therefore, this possibly explains the lower lifetime of the 90 min etched wafer with a-Si:H passivation as compared to that with iodine-ethanol passivation.

The cross-sectional morphologies of the etched wafers are investigated, and they show similar results without distinguishable difference. As a representative, Figure 4 shows the TEM cross-sectional images of a pyramid on surfaces of the 90 min etched wafer with a-Si:H passivation. Figures 4(a) and 4(b) confirm (i) difficulty of deposition of a-Si:H on the mountain and valley regions, where the interfaces between a-Si:H and wafer are deteriorate, and (ii) nonuniform thickness, which can be a severe problem for a HJ solar cell since the a-Si:H layer is typically very thin. Even small thickness variation may result in large deviation from the optimal passivation condition. In addition, a-Si:H deposited at the mountains and valleys can possibly have low film properties, which

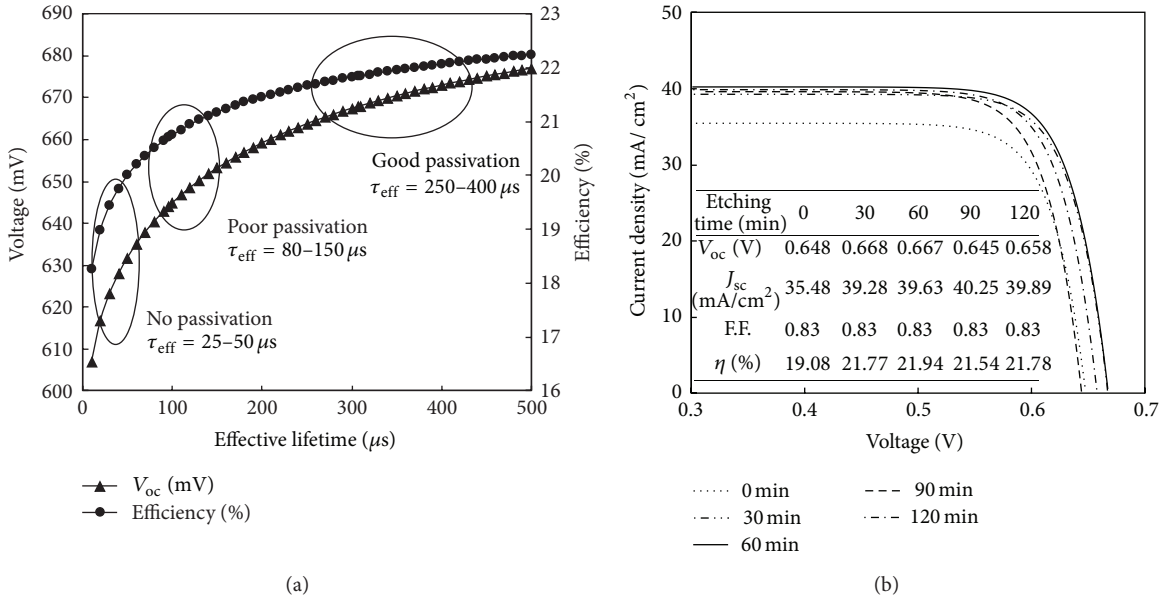

Figure 5: (a) Simulated open-circuit voltage and conversion efficiency as a function of minor carrier lifetimes. (b) Simulated J-V curves of HJ solar cell with different etching times.

Table 1: Simulation parameters for HJ silicon solar cells.

Device parameter	Value				
Device area (cm^2)	1				
Emitter contact resistance (Ω)	6×10^{-3}				
Base contact resistance (Ω)	5×10^{-3}				
Internal conductance (S)	3×10^{-3}				
Device structure	n-Si/i-Si/c-Si/Al-BSF				
Rear reflectance (%)	90				
Light source	One sun (AM 1.5 G, 100 mW/cm^2, 25°C)				
Layer parameter	a-Si:H (n)	a-Si:H (i)		c-Si (p)	Al-BSF
Thickness (μm)	0.01	0.005		250	5
Band gap (eV)	1.92	1.7		1.12	1.12
Dielectric constant	11.9	11.9		11.9	11.7
Doping concentration (cm^{-3})	1×10^{19}	—		1×10^{16}	1×10^{19}
Etching time (min)	0	30	60	90	120
*Wafer effective lifetime (μs)	133.81	307.45	300.12	95.81	187.16
*Wafer front reflectance (%)	38.67	22.67	12.66	11.06	14.69
*Device front reflectance with ITO (%)	13.36	4.95	2.60	2.71	3.02

*Measured from experimental data.

is reported to be detrimental to final device performance [27]. On the contrary, the hillside region shows a clear interface between wafer and a-Si:H, as shown in Figure 4(c). Therefore, these TEM images support the mechanism of a-Si:H passivation proposed previously.

The experimental values of the carrier lifetimes of the wafers with different etching times and with a-Si:H passivation were input to the one-dimensional simulation software PC1D [28, 29] to provide theoretical analysis about the cell performance. The main parameters are summarized in Table 1. The simulation result of V_{oc}, which is the mostly affected, and the conversion efficiency (η) of the HJ solar cells as function of the carrier lifetime are plotted in Figure 5(a). Generally, an increased carrier lifetime will lead to a reduced diode dark current and thus improve V_{oc}, according to [30]

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{J_{sc}}{J_0}\right), \quad (2)$$

where kT/q is the thermal voltage and J_0 is the diode dark current. In order to exclude variables other than the lifetime, the reflectance was kept to a constant value of 5%, so that J_{sc}

in (2) would be influenced mainly by carrier lifetime as given by [31]

$$J_{sc} = qG\sqrt{D_p}\tau_p + \sqrt{D_n\tau_n}, \quad (3)$$

where G is the carrier generation rate, D_p (D_n) is the diffusion coefficient of holes (electrons), and τ_p (τ_n) is the lifetime of holes (electrons). Three regions are divided for discussion. Firstly, the wafer lifetimes ranging from 25 to 50 μs correspond to the wafers without passivation, so that J_0 is large due to huge amount of surface dangling bonds. In this region, V_{oc} is less than 630 mV and η is lower than 20%. Secondly, the lifetimes in the range of 80–150 μs result from the wafers having saw damage or considerable turning points, leading to poor a-Si:H passivation quality. The intermediate V_{oc} of about 640–650 mV and η of 20.5%–21% are observed. Thirdly, high lifetime regions of 250–400 μs can correspond to a wafer with little turning points and a good a-Si:H passivation close to the ideal passivation conditions. The resultant V_{oc} and η can be higher than 660 mV and 22%, respectively.

Figure 5(b) shows the I-V characteristics and external parameters of the HJ solar cells with different wafer etching times. Note that the effect of light reflection caused by surface roughness of the etched wafers was taken into account by inputting the experimental front reflectance values of the fabricated devices with ITO. The ITO acts as not only front electrode but also antireflective layer, so that the device reflection is significantly lower than that of the wafers. The device reflectance values are 13.36%, 4.95%, 2.60%, 2.71%, and 3.02% for the etching times of 0, 30, 60, 90, and 120 min, respectively. V_{oc} values still match well the result shown in Figure 5(a), in which the poor passivation region corresponds to the 0, 90, and 120 min etching times, while the good passivation region corresponds to the 30 and 60 min etching times. The trend of J_{sc} is mainly determined by the device reflectance and the carrier lifetime, shown in (3). The former has much larger dependence on J_{sc}. FF does not change significantly as the wafer etching time varies. It should be noted that the optimal η is determined by a trade-off between V_{oc} and J_{sc}. These two parameters increase for the early etching stage (0–40 min). However, when the etching time increases, J_{sc} remains increasing until the etching time exceeds 90 min, while V_{oc} decreases due to the notable amount of turning points produced. Overall, the maximum η of 21.94% occurs at the etching time of 60 min.

4. Conclusions

This study investigates the influence of the etching time on a-Si:H passivation capability, wafer carrier lifetime, and HJ solar cell performance. It is found that different etching time will greatly affect the a-Si:H passivation capability according to the produced turning points. A small number of the turning points lead to good a-Si:H passivation capability which can even be comparable to the ideal iodine-ethanol solution passivation. However, a wafer with high turning points may lead to poor a-Si:H passivation which greatly reduces the carrier lifetime. The a-Si:H layer is found to be difficultly well-deposited at the turning points as evidenced by the fact that the interfaces between the a-Si:H and wafer surface are deteriorate. Finally, with different etching time, there is a trade-off between V_{oc} and J_{sc} to obtain the optimal conversion efficiency. In this case, the maximum conversion efficiency is 21.94% for a HJ solar cell with a wafer etching time of 60 min.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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References

[1] M. Taguchi, A. Yano, S. Tohoda et al., "24.7% record efficiency HIT solar cell on thin silicon wafer," *IEEE Journal of Photovoltaics*, vol. 4, no. 1, pp. 96–99, 2014.

[2] T. Mishima, M. Taguchi, H. Sakata, and E. Maruyama, "Development status of high-efficiency HIT solar cells," *Solar Energy Materials & Solar Cells*, vol. 95, no. 1, pp. 18–21, 2011.

[3] Y. Tsunomura, Y. Yoshimine, M. Taguchi et al., "Twenty-two percent efficiency HIT solar cell," *Solar Energy Materials & Solar Cells*, vol. 93, no. 6-7, pp. 670–673, 2009.

[4] L. Korte, E. Conrad, H. Angermann, R. Stangl, and M. Schmidt, "Advances in a-Si:H/c-Si heterojunction solar cell fabrication and characterization," *Solar Energy Materials and Solar Cells*, vol. 93, no. 6-7, pp. 905–910, 2009.

[5] S. Tohoda, D. Fujishima, A. Yano et al., "Future directions for higher-efficiency HIT solar cells using a thin silicon wafer," *Journal of Non-Crystalline Solids*, vol. 358, no. 17, pp. 2219–2222, 2012.

[6] A. Datta, M. Rahmouni, M. Nath et al., "Insights gained from computer modeling of heterojunction with instrinsic thin layer "HIT" solar cells," *Solar Energy Materials & Solar Cells*, vol. 94, no. 9, pp. 1457–1462, 2010.

[7] D. Zhang, A. Tavakoliyaraki, Y. Wu, R. A. C. M. M. van Swaaij, and M. Zemana, "Influence of ITO deposition and post annealing on HIT solar cell structures," *Energy Procedia*, vol. 8, pp. 207–213, 2011.

[8] M. Edwards, S. Bowden, U. Das, and M. Burrows, "Effect of texturing and surface preparation on lifetime and cell performance in heterojunction silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 92, no. 11, pp. 1373–1377, 2008.

[9] M. Rosa, M. Allegrezza, M. Canino, C. Summonte, and A. Desalvo, "TMAH-textured, a-Si/c-Si, heterojunction solar cells with 10% reflectance," *Solar Energy Materials & Solar Cells*, vol. 95, no. 11, pp. 2987–2993, 2011.

[10] Y. Yang, M. A. Green, A. Ho-Baillie, H. Kampwerth, S. Pillai, and H. Mehrvarz, "Characterization of 2-D reflection pattern from textured front surfaces of silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 115, pp. 42–51, 2013.

[11] P. K. Basu, D. Sarangi, K. D. Shetty, and M. B. Boreland, "Liquid silicate additive for alkaline texturing of mono-Si wafers to

improve process bath lifetime and reduce IPA consumption," *Solar Energy Materials and Solar Cells*, vol. 113, pp. 37–43, 2013.

[12] H. Park, S. Kwon, J. S. Lee, H. J. Lim, S. Yoon, and D. Kim, "Improvement on surface texturing of single crystalline silicon for solar cells by saw-damage etching using an acidic solution," *Solar Energy Materials & Solar Cells*, vol. 93, no. 10, pp. 1773–1778, 2009.

[13] M. Schmidt, L. Korte, A. Laades et al., "Physical aspects of a-Si:H/c-Si hetero-junction solar cells," *Thin Solid Films*, vol. 515, no. 19, pp. 7475–7480, 2007.

[14] M. R. Page, E. Iwaniczko, Y. Xu et al., "Well passivated a-Si:H back contacts for double-heterojunction silicon solar cells," in *Proceedings of the 4th IEEE World Conference on Photovoltaic Energy Conversion*, vol. 2, pp. 1485–1488, Waikoloa, Hawaii, USA, May 2006.

[15] D. Iencinella, E. Centurioni, R. Rizzoli, and F. Zignani, "An optimized texturing process for silicon solar cell substrates using TMAH," *Solar Energy Materials & Solar Cells*, vol. 87, pp. 725–732, 2005.

[16] B. Stegemann, J. Kegel, M. Mews et al., "Evolution of the charge carrier lifetime characteristics in crystalline silicon wafers during processing of heterojunction solar cells," *Energy Procedia*, vol. 55, pp. 219–228, 2014.

[17] J. Kegel, H. Angermann, U. Stürzebecher et al., "Over 20% conversion efficiency on silicon heterojunction solar cells by IPA-free substrate texturization," *Applied Surface Science*, vol. 301, pp. 56–62, 2014.

[18] D. Deligiannis, S. Alivizatos, A. Ingenito et al., "Wet-chemical treatment for improved surface passivation of textured silicon heterojunction solar cells," *Energy Procedia*, vol. 55, pp. 197–202, 2014.

[19] G. Li, Y. Zhou, and F. Liu, "Influence of textured c-Si surface morphology on the interfacial properties of heterojunction silicon solar cells," *Journal of Non-Crystalline Solids*, vol. 358, no. 17, pp. 2223–2226, 2012.

[20] D. Murias, C. Reyes-Betanzo, M. Moreno et al., "Black Silicon formation using dry etching for solar cells applications," *Materials Science and Engineering B*, vol. 177, no. 16, pp. 1509–1513, 2012.

[21] H. Park, S. Kwon, J. S. Lee, H. J. Lim, S. Yoon, and D. Kim, "Improvement on surface texturing of single crystalline silicon for solar cells by saw-damage etching using an acidic solution," *Solar Energy Materials and Solar Cells*, vol. 93, no. 10, pp. 1773–1778, 2009.

[22] S.-Y. Lien, Y.-C. Chang, Y.-S. Cho, Y.-Y. Chang, and S.-J. Lee, "Deposition and characterization of high-efficiency silicon thin-film solar cells by HF-PECVD and OES technology," *IEEE Transactions on Electron Devices*, vol. 59, no. 5, pp. 1245–1254, 2012.

[23] L. Wang, F. Wang, X. Zhang et al., "Improving efficiency of silicon heterojunction solar cells by surface texturing of silicon wafers using tetramethylammonium hydroxide," *Journal of Power Sources*, vol. 268, pp. 619–624, 2014.

[24] U. K. Das, M. Z. Burrows, M. Lu, S. Bowden, and R. W. Birkmire, "Surface passivation and heterojunction cells on Si (100) and (111) wafers using dc and rf plasma deposited Si:H thin films," *Applied Physics Letters*, vol. 92, no. 6, Article ID 063504, 2008.

[25] H. Yan, S. Swaraj, C. Wang et al., "Influence of annealing and interfacial roughness on the performance of bilayer donor/acceptor polymer photovoltaic devices," *Advanced Functional Materials*, vol. 20, no. 24, pp. 4329–4337, 2010.

[26] B. Sopori, P. Rupnowski, J. Appel, and D. Guhabiswas, "Light-induced passivation of Si by iodine ethanol solution," in *Proceedings of the Materials Research Society (MRS) Fall Meeting*, NREL/CP-520-44999, 2009.

[27] S. Kim, V. A. Dao, C. Shin et al., "Low defect interface study of intrinsic layer for c-Si surface passivation in a-Si:H/c-Si heterojunction solar cells," *Thin Solid Films*, vol. 521, pp. 45–49, 2012.

[28] J. Coignusa, M. Baudrita, J. Singer, R. Lachaume, D. Muñoz, and P. Thony, "Key issues for accurate simulation of a-Si:H/c-Si heterojunction solar cells," *Energy Procedia*, vol. 8, pp. 174–179, 2011.

[29] L. Zhao, H. L. Li, C. L. Zhou, H. W. Diao, and W. J. Wang, "Optimized resistivity of p-type Si substrate for HIT solar cell with Al back surface field by computer simulation," *Solar Energy*, vol. 83, no. 6, pp. 812–816, 2009.

[30] M. H. Vishkasougheh and B. Tunaboylu, "Simulation of high efficiency silicon solar cells with a hetero-junction microcrystalline intrinsic thin layer," *Energy Conversion and Management*, vol. 72, pp. 141–146, 2013.

[31] J.-Y. Jung, Z. Guo, S.-W. Jee et al., "A waferscale Si wire solar cell using radial and bulk p-n junctions," *Nanotechnology*, vol. 21, no. 44, Article ID 445303, 2010.