

Research Article

Correlation of Interfacial Transportation Properties of CdS/CdTe Heterojunction and Performance of CdTe Polycrystalline Thin-Film Solar Cells

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The light and dark output performances of CdS/CdTe solar cells made by close-spaced sublimation (CSS) were investigated to elucidate the transportation properties of carriers at CdS/CdTe heterojunction interface. It has been found that the interfacial transportation properties were relatively sensitive to variations of the characteristics of heterojunction due to the series resistance and shunting effects. For the high quality cell with 12.1% efficiency, narrow depletion region of ~ 1.1 microns and large electric field intensity of ~ 1.3 V/ μm allow the sufficient energy-band bending close to CdS layer at CdS/CdTe heterojunction, which changes the carrier transportation mechanism from emission to diffusion and leads to the optimal rectifying characteristics with small dark saturation current density $\sim 6.4 \times 10^{-10}$ A/cm². As a result, the schematic diagram of heterojunction band structure corresponding to various performances of solar cells has also been presented.

1. Introduction

CdS/CdTe solar cell with the typical structure of glass/TCO/n-CdS/p-CdTe/back contact layer/back electrode has received widespread attention due to the high theoretical conversion efficiency ($\sim 29\%$) and simple fabrication process [1–3]. Based on this structure, many research groups have been engaged in the improvement of the cell efficiency through improving device fabrication process, optimizing the cell structure, and further analyzing the various physical mechanisms in cells [4–6]. So far, First Solar has manufactured the highest conversion efficiency that exceeded 20% of single-junction CdTe thin-film solar cell [7]. As the key part of CdTe solar cell, the characteristics of CdS/CdTe heterojunction are associated with the fabrication condition of CdS and CdTe, posttreatment of CdTe, the type of dopant, and so forth [8–11]. As we know, even in the same deposition process, the interfacial characteristic of CdS/CdTe will be probably different due to the nonuniform thickness distribution of CdS and CdTe. Notably, the properties of CdS/CdTe heterojunction can be optimized after CdCl₂

annealing, which is attributed to improvement of charge carrier density by Cl⁻¹ dopant, elimination of pinholes and shorts by grain growth and grain boundary passivation, and reduction in the interfacial state by interdiffusion of S and Te at the interface of CdS/CdTe [12–16]. However, the initial nonuniformity at the CdS/CdTe interface may increase after annealing. For example, the CdS/CdTe heterojunction may be destructed by localized-consumption of CdS with nonuniform thickness distribution. This is detrimental to the junction properties, including the considerable nonuniform distribution of depletion region width, contact potential difference, and electric field intensity, which further affects the generation, separation, and transportation of electron-hole pairs at interface [9, 10, 14, 16–18]. Moreover, CdTe polycrystalline film with mixing orientations always has a lot of grain boundaries, which is very different from single crystalline semiconductors [19]. A large amount of defects, for example, the shorts, generated at grain boundaries during the fabrication process of cell will also have considerable impacts on the rectifying characteristics of heterojunction, thereby also affecting the transportation of carriers. These

TABLE I: Summarized relevant parameters for CdTe cells.

Samples	R_{sh}/Ω	R_s/Ω	FF/%	J_{sc}/mAcm^{-2}	V_{oc}/mV	$\eta/\%$	$J_0/\text{Acm}^{-2} (\times 10^{-9})$	A	$N_D/\text{cm}^{-3} (\times 10^{13})$	V_D/V	$X_D/\mu\text{m}$	$\epsilon_m/\text{V}/\mu\text{m}$
1	1668	251	42.9	11.8	517	2.3	11	3.0	6.5	1.05	4.2	0.5
2	1179	238	38.6	20.1	600	4.0	3.3	2.3	3.7	0.76	4.7	0.3
3	1117	190	40.7	22.8	739	6.1	3.3	2.1	8.7	0.81	3.2	0.5
4	1962	159	48.4	25.1	752	8.2	1.8	1.9	16.1	0.75	2.2	0.7
5	3910	123	57.3	26.4	757	10.2	1.1	1.9	25.0	0.75	1.8	0.8
6	7858	86	65.8	26.8	776	12.1	0.64	1.9	63.4	0.70	1.1	1.3

variations in transportation properties of heterojunction will inevitably be reflected on the devices performance [9, 10]. So, it is believed that an inherent correlation of interfacial characteristics of CdS/CdTe heterojunction and performance of cell should be associated with generation and transportation properties of electron-hole pairs (carriers). Specifically, an efficient transportation of carriers in junction interface is an indispensable electrical element to attain a high efficiency in CdTe solar cell. Motivated by this, we have measured a set of cells with different performance and calculated the relevant parameters of heterojunction characteristics, such as diode ideality factor A , reverse dark saturation density J_0 , doping concentration N_D , depletion region width X_D , contact potential difference V_D , and electric field intensity ϵ_m , and then investigated the effect of these interfacial parameters on the performances of CdS/CdTe thin-film solar cells. Based on these results, we present the schematic diagram of energy band to qualitatively simulate the interfacial transportation properties of CdS/CdTe heterojunction.

2. Experiments

In this work, a set of CdS/CdTe polycrystalline thin-film solar cells (each cell area is 0.07 cm^2) with the same structure of glass/ITO/CdS (CBD: $\sim 100 \text{ nm}$)/CdTe (CSS: $\sim 3.5 \mu\text{m}$)/ZnTe:Cu/Au has been fabricated in the same experimental conditions depicted in [20]. Cells with a conversion efficiency interval of $\sim 2\%$ were selected for analysis as summarized in Table I. Photocurrent density versus voltage J - V curve was measured under an AM1.5 spectrum at $100 \text{ mW}/\text{cm}^2$ using I - V characteristics of solar cell test system. Dark current density versus voltage curve was also measured at the bias range of -1.5 V to 2.5 V using the Agilent 4155C semiconductor characteristics tester. Spectral response SR was measured by WDP500-E automatic scanning monochromator. Capacitance versus voltage C - V curve was measured at a frequency of 200 KHz using the Agilent 4155C semiconductor characteristics tester at the bias range from -1.5 V to 2.5 V in the dark. Additionally, the performance of CdS/CdTe cells was mainly analyzed at a small forward bias $< 0.75 \text{ V}$ dominated by heterojunction, and all the measurements were carried out at room temperature 25°C .

3. Results and Discussion

Photocurrent density versus voltage J - V is plotted in Figure 1(a) and the relevant parameters are listed in Table I. With the continued increase of the conversion efficiency from

$\sim 6\%$, the series resistance R_s and the shunt resistance R_{sh} have obviously changed while the open circuit voltage V_{oc} remains $\sim 750 \text{ mV}$. R_s of sample 6 decreases by $\sim 54.7\%$, while R_{sh} dramatically increases by $\sim 603.5\%$ compared to sample 3. As known from the equivalent circuit of the solar cell [21], the output performance of cells is subject to two key parameters: R_s and R_{sh} , which arises easily from the resistance and current flow of the cell materials and arises from leakage of the cell, respectively.

Figure 1(b) shows the dark current versus bias curves. Under the reverse bias or a small forward bias, the current is very small and relatively insensitive to variation in bias. However, an exponential increase in current can be clearly observed at the large forward bias, and the difference in the magnitude of current increase of each cell is clearly visible under the same bias, especially for samples 1, 2, and 3. The $\ln I$ versus bias curves derived from Figure 1(b) are depicted in Figure 1(c) for further quantifying the dark current output properties. Meanwhile, ideal dark current ($R_s \sim 0$, $R_{sh} \sim \infty$, and $A = 2$) versus bias (dashed line) is also shown in Figure 1(c) for comparison. Inset of Figure 1(c) plots the change of diode ideality factor A with the bias. All the values of A in region 2 are also listed in Table I. A of poor performance cells like sample 1 is ~ 3.0 , while it decreases to ~ 1.9 with respect to the good performance cells with efficiency larger than $\sim 8\%$.

As we know, the CdS/CdTe heterojunction current is described as follows [21, 22]:

$$I = I_0 \left(e^{q(V-IR_s)/AKT} - 1 \right) + \frac{V - IR_s}{R_{sh}}, \quad (1)$$

where I_0 is dark reverse saturation current, K is Boltzmann's constant, and in this work T is 298 K and A is defined as the diode ideality factor representing the diffusion and recombination current components. Although the drift movement in the boundary of depletion region increases with the reverse bias, the amount of minority carriers is very small, resulting from a simplified formula (1) $I \sim I_0$, corresponding to the dark reverse saturation current density J_0 listed in Table I. Notably, while conversion efficiency of cell increases from $\sim 2.3\%$ to $\sim 12.1\%$, J_0 decreases more than an order magnitude from $J_{0,\eta=2.3\%} \sim 1.1 \times 10^{-8} \text{ Acm}^{-2}$ to $J_{0,\eta=12.1\%} \sim 6.4 \times 10^{-10} \text{ Acm}^{-2}$. Moreover, the decrease of J_0 with increasing shunt resistance R_{sh} calculated from formula (1) reveals the evolution of shunting effect in the CdS/CdTe heterojunction.

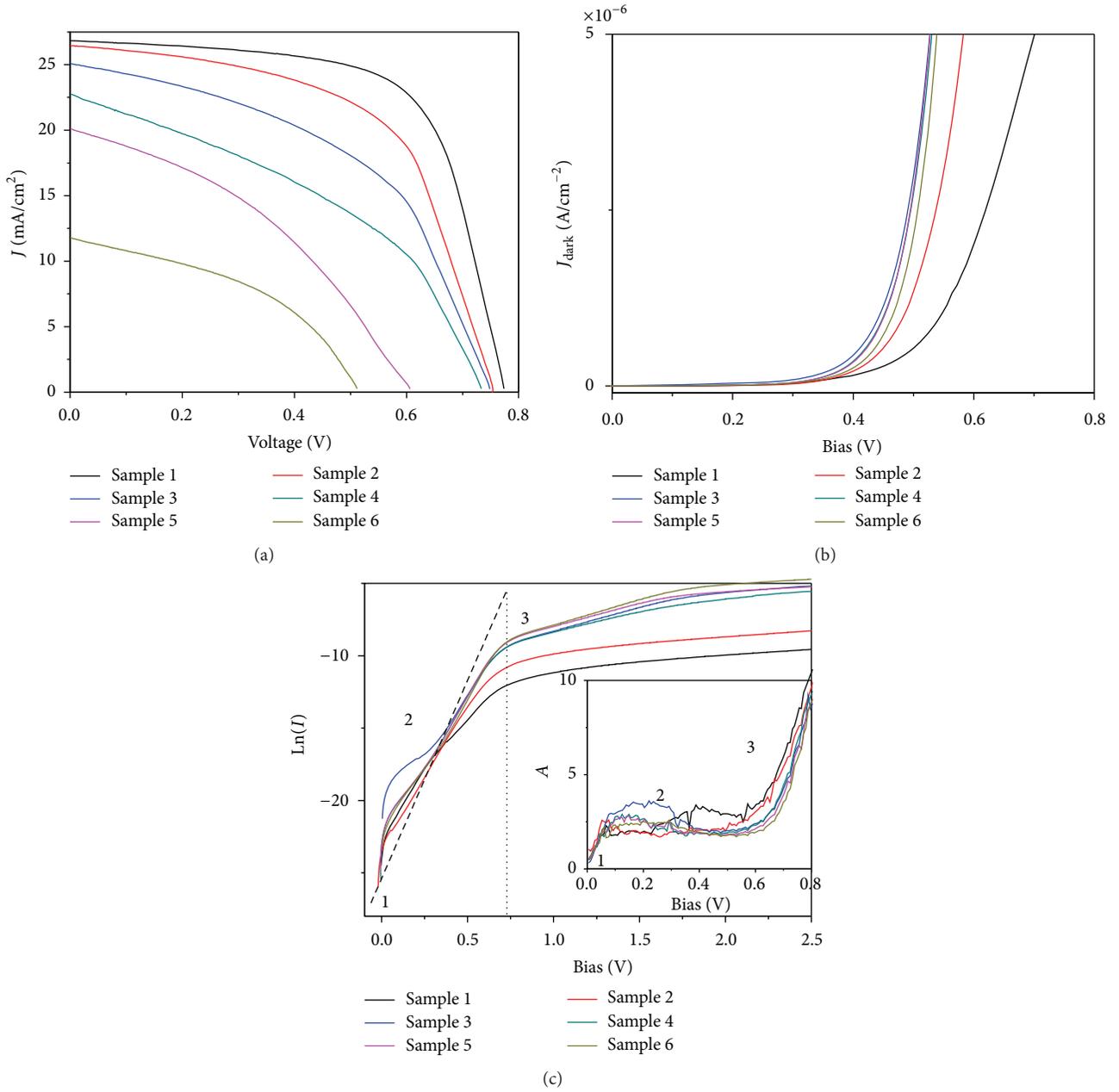


FIGURE 1: Plots of photocurrent (a) and dark current (b) versus bias of CdS/CdTe cells. (c) Plots of $\ln I$ versus V for all cells. Inset showing the variation in diode ideality factor at different bias.

At the forward bias $\exp((qV - IR_s)/Ak_0T) \gg 1$, formula (1) can be simplified as follows:

$$I = I_0 e^{q(V - IR_s)/AKT}. \quad (2)$$

Taking the logarithm of formula (2) generates the following formula:

$$\ln(I) = \ln(I_0) + \frac{q(V - IR_s)}{AKT}. \quad (3)$$

When $IR_s \ll V \ll AkT/q$, the movement of drift will reduce but diffusion will increase due to the narrower depletion region, resulting in the nonlinear increase in current

defined as $\ln I = \ln I_0 + \ln(qV/AkT)$ shown in region 1 from 0 V to ~ 0.01 V. The actual current increases faster than the ideal current in this region that may be attributed to a very small A caused by the predominant diffusion current. As the forward bias continues to increase from ~ 0.01 V to ~ 0.75 V, the current simplified as $\ln I = \ln I_0 + qV/AkT$ increases linearly in region 2. However, the rate of current increase is different, which is attributed to varying barrier height at the interface of cells to be discussed later in this paper. In this region the current consists of predominant recombination current corresponding to the slight change of diode ideality factor $A \sim 2$ listed in Table 1. According to

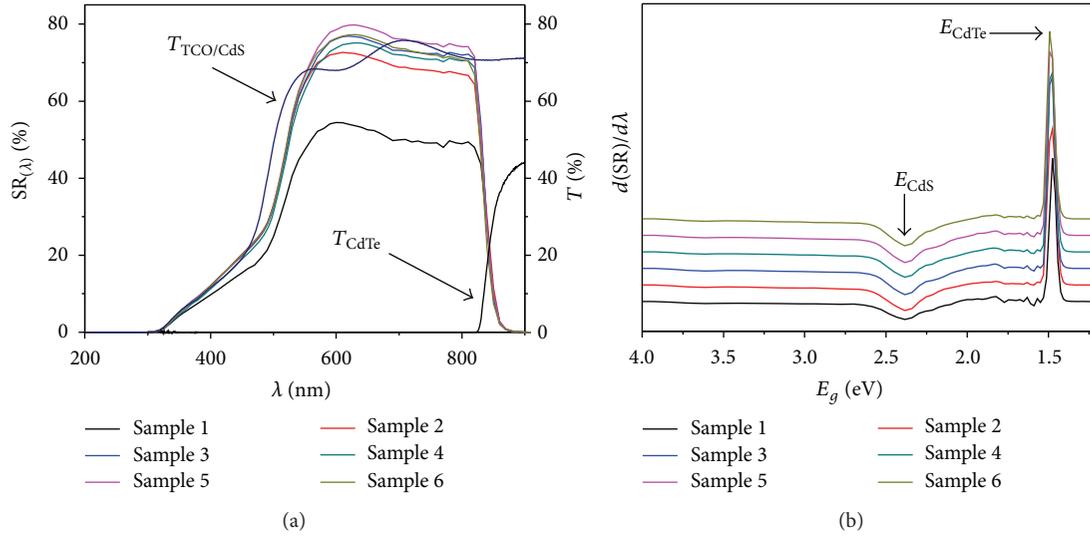


FIGURE 2: (a) SR of cells. For comparison, $T_{\text{ITO/CdS}}$ and T_{CdTe} are listed in this figure, respectively. (b) Plots of $d(\text{SR})/dE$ versus E for cells, photon energy E is obtained by $E = 1240/\lambda$, and E_g of CdS and CdTe is also marked in this figure.

Sah-Noyce-Shockley theory, the lower diode ideality factor ~ 1.9 of samples 4–6 indicates a larger recombination current compared to other samples in this paper [23, 24]. As the bias further increases, a turning point at ~ 0.75 V is clearly observed in region 3 where current is defined as $\ln I = \ln I_0 + q(V - IR_s)/AkT$, indicating a contribution of additional resistance R_s causing a phenomenon of “roll-over” [25]. This turning point demonstrates the change in current component from recombination to thermionic emission in region 3, resulting in a pronounced reduction of current increase [26].

Figure 2(a) shows the spectral response SR of the same set of devices depicted in Figure 1. Additionally, the transmittance T of ITO/CdS composite film ($T_{\text{ITO/CdS}}$) and CdTe film (T_{CdTe}) is also listed in Figure 2(a) for analysis. As can be seen, most photons which can generate photogenerated carriers are located between the lower right of $T_{\text{ITO/CdS}}$ and the left front of T_{CdTe} . This demonstrates that carriers are generated in CdTe absorbed layer whether poor or good samples. Meanwhile, the fluctuation of SR of each cell is visible, which is accompanied by a maximum response point at 620 nm corresponding to photon energy of 2.0 eV. Moreover, the area surrounded by SR curve gradually decreases with the degradation of cell performance which is consistent with the variation in the short circuit current density J_{sc} . It is well known that not only the collection but also the generation and transportation of carriers have significant impacts on the J_{sc} [23].

According to the absorption coefficient and length distribution in CdTe [27, 28], CdTe with a thickness of $3.5 \mu\text{m}$ in this work can absorb all the visible light and convert the light into electricity, indicating that all the cells seem to have the same ability to generate the carriers. As shown in Figure 2(a), the absorption position of photons with energy higher than 2 eV is closer to the CdS/CdTe interface where the existence of high interface state is particularly detrimental

to the transportation of the carrier, resulting in a decrease of visible absorption in SR. Furthermore, for the photons with energy less than 2.0 eV, their absorption length will increase and the absorption position will deeply extend into the depletion region, in which the existence of various defects and deep centers has also adverse impact on the transportation of electron-hole pairs, which further reduces the spectral response [29]. Finally, the reduction in SR of poor performance of samples can be perceived pronouncedly, especially for sample 1.

By identifying the wavelength of cutoff side in SR, band gap E_g of CdTe and CdS can be obtained as shown in Figure 2(b) [27]. Each CdTe has almost the same $E_g \sim 1.47$ eV that is lower than that of CdTe thin film (1.50 eV) deposited by CSS [20], demonstrating the existence of $\text{CdS}_x\text{Te}_{1-x}$ ternary alloy formed by diffusion of S and Te during the deposition and annealing processes [30]. Value of x in $\text{CdS}_x\text{Te}_{1-x}$ can be obtained according to the formula [27]: $E_g(x) = 1.74x^2 - 1.01x + 1.51$. However, the value of x for all samples is very small of $3.6 \times 10^{-2} \sim 4.8 \times 10^{-2}$, indicating a negligible correlation of the change in band gap and S level of CdTe and the variation in cell performance.

The capacitance C versus bias V shown in Figure 3(a) has been characterized for further investigating the interfacial characteristics of CdS/CdTe heterojunction. When the cell is under the reverse bias, the capacitance of each cell is very small and changes slightly, which indicates that the majority carriers of cell are depleted [31]. Moreover, when cells are under the forward bias, a significant difference in capacitance of each cell can be observed. As we known, the capacitance C and the depletion region width X_D have the following relationship: $C = \epsilon_r \epsilon_0 A / X_D$, where A is the cell area. Furthermore, studies have shown that the capacitance is also related to the distribution of doping concentration

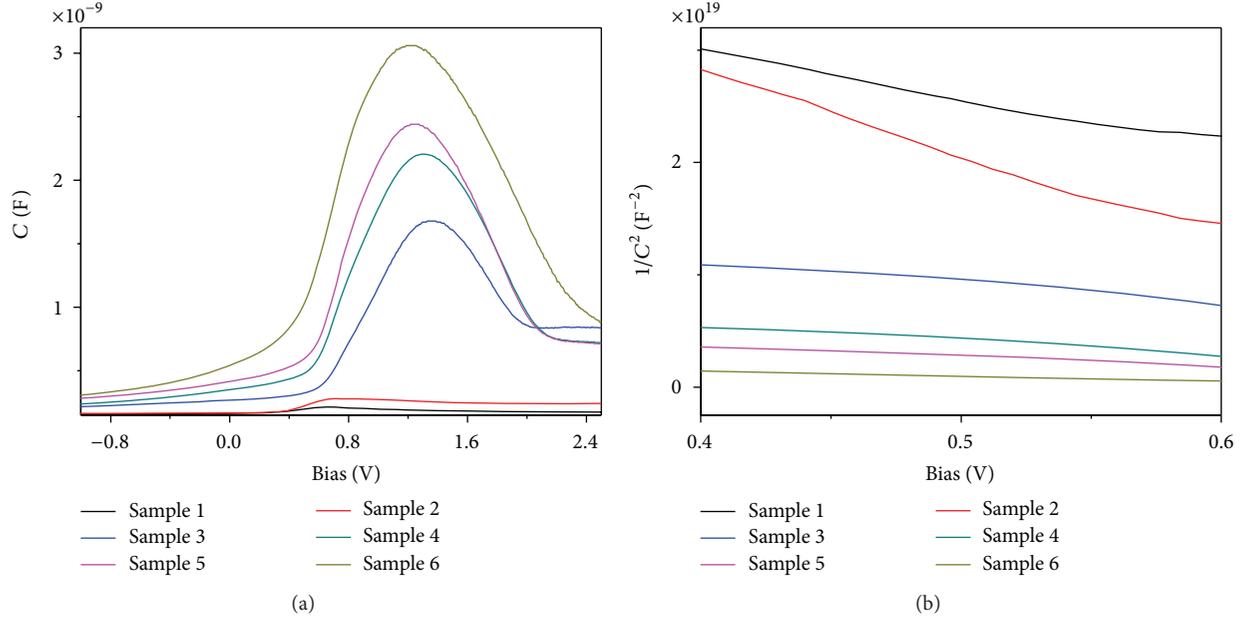


FIGURE 3: (a) C versus V curves for cells. (b) Plots of C^{-2} versus V under the range of 0.4 V–0.6 V with CdS/CdTe junction conforming depletion layer approximation and processed according to unilateral abrupt junction.

N_D and contact potential difference V_D at heterojunction as depicted in formula (4) [13, 32]. The variation in C^{-2} as a function of bias for all cells under the bias range of 0.4 V–0.6 V has been plotted in Figure 3(b).

The value of N_D and V_D can be obtained by fitting the straight line portion of C^{-2} versus V curve. Meanwhile, X_D can be also obtained by formula (5):

$$\frac{1}{C_T^2} = \frac{2V_D}{A^2 \epsilon_r \epsilon_0 q N_D} - \frac{2V}{A^2 \epsilon_r \epsilon_0 q N_D}, \quad (4)$$

$$X_D = \sqrt{\frac{2\epsilon_r \epsilon_0 V_D}{q N_D}}. \quad (5)$$

Moreover, the correlation of V_D and electric field intensity ϵ_m is as follows: $V_D = (-\epsilon_m X_D)/2$, which represents the degree of energy-band bending which consequently determines the current transportation mechanism in interface [21, 22]. All the above-calculated parameters are summarized in Table 1. These parameters corresponding to the poor performance of solar cells have been found considerably different from their good performance counterparts. To further analyze the current transportation properties at heterojunction interface, we also propose the schematic diagram of energy band for CdS/CdTe heterojunction in Figure 4 [33–36].

As listed in Table 1, the depletion region width of sample 1 ($\sim 4.2 \mu\text{m}$) and sample 2 ($\sim 4.7 \mu\text{m}$) is not only larger than that of other samples but also larger than the $\sim 3.5 \mu\text{m}$ thick CdTe, which means that the conduction band of these two samples is higher than that of other samples. Meanwhile, because the V_D is up to ~ 1.05 V, especially for sample 1, only a few electrons with the kinetic energy higher than the barrier height have the ability to surmount the interface into CdS

layer by thermionic-emission mechanism [37]. Furthermore, their electric field intensity is very small $\sim 0.5 \text{ V}/\mu\text{m}$, indicating a slight energy-band bending near the back contact due to Fermi-level pinning as shown in Figures 4(a) and 4(b), which suggests that photogenerated carriers can easily be recombined during the transportation process. As a result, sample 1 shows a low short circuit current density of $\sim 11.8 \text{ mA}/\text{cm}^2$ with a low doping density of $\sim 6.5 \times 10^{13} \text{ cm}^{-3}$. This further demonstrates the obvious series resistance and shunting effects at the interface of CdS/CdTe heterojunction [38], which is in good agreement with the results obtained in the previous sections. As the lower V_D of samples 3 and 4 compared to sample 1, more electrons move through a diffusive process. Meanwhile, energy-band bending at the interface increases and gradually moves close to CdS layer shown in Figures 4(c) and 4(d) due to the reduction of depletion region width and the increase of electric field intensity, which is beneficial to improve the carrier transportation in the junction region. However, since their depletion region widths are $\sim 3.2 \mu\text{m}$ and $2.2 \mu\text{m}$, respectively, which are still larger than half CdTe thickness, the carriers are still easily recombined during the transportation process when the electric field intensity increases slightly from $0.5 \text{ V}/\mu\text{m}$ to $0.7 \text{ V}/\mu\text{m}$. But for sample 5 and sample 6, especially for sample 6, owing to the small $V_D \sim 0.7$ V, the electrons transport at interface mainly by diffusion mechanism, leading to a significant reduction in series resistance. Meanwhile, the energy band is sufficiently bent close to CdS with the narrow depletion region of $\sim 1.1 \mu\text{m}$ and the large electric field intensity of $\sim 1.3 \text{ V}/\mu\text{m}$, meaning a high quality transportation accompanying a large J_{sc} exceeding $26 \text{ mA}/\text{cm}^2$ with a high doping concentration of $\sim 6.3 \times 10^{14} \text{ cm}^{-3}$, further exposing an optimal shunting effect at interface [33, 37, 39].

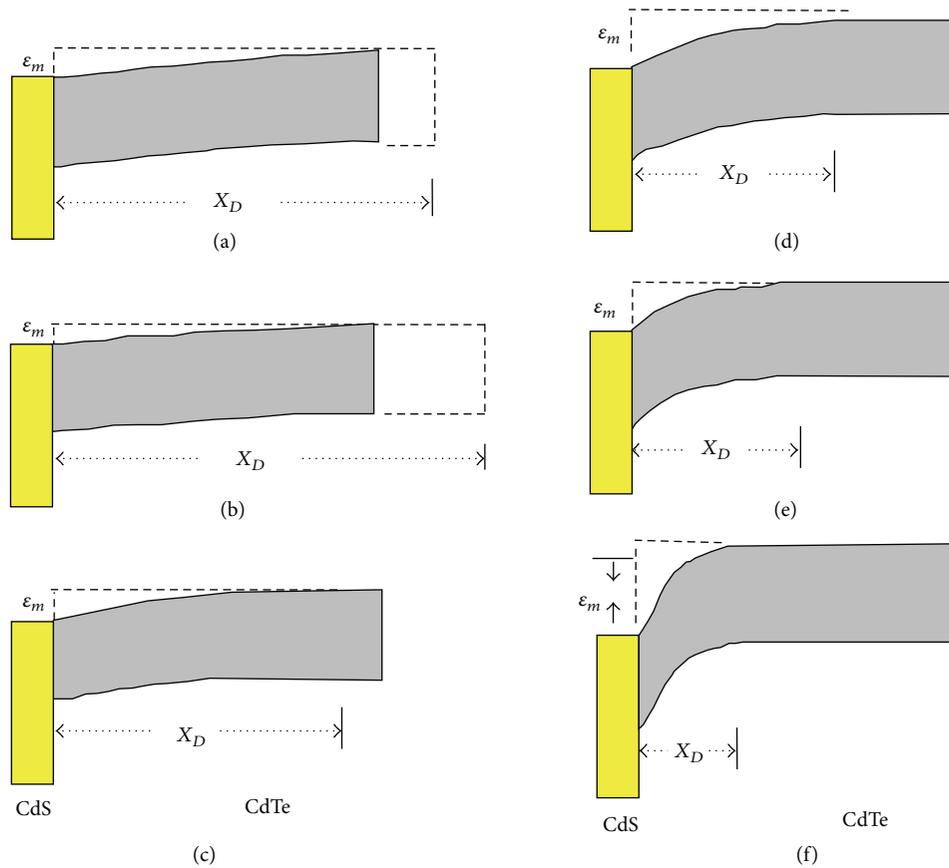


FIGURE 4: Schematic diagram of energy band for CdS/CdTe heterojunction. ((a)–(f)) Corresponding to samples 1–6, respectively.

4. Conclusions

We systematically studied the interfacial properties of CdS/CdTe heterojunction with variation in the performance of CdS/CdTe thin-film solar cells. The results further demonstrated the critical role of carrier transportation. For example, the mechanism of carrier transportation for the poor performance of CdS/CdTe cells was basically emission mechanism, and it was found to change to predominant diffusion mechanism for good performance of cells. By analyzing the interfacial properties of heterojunction well, the degradation in the cell performance was associated with the serious series resistance and shunting effects, suggesting a strong correlation between the output performance of CdS/CdTe solar cell and its interfacial transportation physical properties (contact potential difference, depletion region width and electric field intensity, and further energy-band bending). Our findings are beneficial to not only improving the uniformity of cell performance but also controlling the fabrication conditions for reproducibility of CdS/CdTe thin-film solar cells.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

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