Research Article

Study on the Stability of Unpackaged CdS/CdTe Solar Cells with Different Structures

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In this work, the stability of unpackaged CdTe solar cells with different configurations was investigated according to the International Electrotechnical Commission IEC 61215-2016. The measurements of thermal cycling from -40°C to $+85^{\circ}\text{C}$ and 24-hour temperature cycling from -40°C to $+85^{\circ}\text{C}$ withstanding the effects of 20-hour penetration of 85°C were carried out in CdS/CdTe solar cells with structures of FTO/CdS/CdTe/Au, FTO/CdS/CdTe/back contact/Au, and FTO/MZO/CdS/CdTe/back contact/Au, respectively. The performances of these cells before and after the thermal aging experiments were investigated by using light and dark I - V together with C - V . The results reveal varied performance degradation before and after thermal aging in the cells with different structures. Among these, the most deteriorated device is the one without back contact (BC), whose efficiency decreased by 25.12% after thermal cycling accompanying an obvious roll-over phenomenon when forward bias was greater than open circuit voltage. On the contrary, the reduction in the efficiency was about 16.80% in the case cells with BC, and the roll-over phenomenon was not so significant. Furthermore, for the devices with optimized front contact of FTO/MZO, the thermal stability was improved obviously. Interestingly, short-circuit current density associated with the carrier concentration of cells remained relatively small variations compared with the change of V_{oc} and fill factor. All the results indicated that an efficient back contact layer and an optimized front electrode were the indispensable structural elements to attain high stabilization in the CdS/CdTe solar cells.

1. Introduction

The research on weather resistance of a solar cell is always time-consuming, expensive, and thus complicated. Therefore, it is necessary to accelerate the test process to study the stability and failure mechanism of the solar cell under thermal cycling, which is supposed to predict the actual evolution of solar cell performance without too long duration. This technique is of great importance in providing reliable indications for the device design and stability optimization of the solar cell. At present, the qualification tests of the International Electrotechnical Commission IEC 61215-2016 and IEC 61583 [1], such as visual inspection and thermal cycling test, are applied to all terrestrial flat plate module materials

such as crystalline silicon and thin-film modules. The literature survey on degradation rates reported by Jordan et al. indicated that the qualification tests have been quite successful in identifying and eliminating module types that suffer high degradation rates early in their lifetime [2]. However, stability test experiments showed that standard device test results cannot be used to predict the service life of cell products [3]. Therefore, it is necessary to prioritize studying the factors that cause aging acceleration of a specific freshly fabricated cell in a lab.

A CdTe thin-film solar cell has attracted intensive research interests because CdTe has a direct band gap of 1.46 eV matching the energy of a solar spectrum and an absorption coefficient as high as 10^{-5} cm^{-1} meaning 90% of

visible light can be absorbed by CdTe with a thickness of 1 micron [4]. Although the CdTe solar cell with a new world conversion efficiency record of 22.1% has been fabricated successfully [5], there are still some key issues that need to be understood with respect to the changes in device performance operated in general open-air conditions, as defined in IEC 60721-2-1. Generally, the failure causes of the CdTe solar cell mainly come from the functional materials and device configuration, especially in thickness, grain boundaries, and internal defects of films [6–9]. On the other hand, the performance of a solar cell is closely related to the properties of the package process as well as the materials. For example, one representative packaging material, adhesive EVA (Ethylene+Vinyl+Acetate), is supposed to be corresponding to the possible failures that include delamination, air leakages, insulation failure, and package damage [10]. The manufacture of the CdS/CdTe solar cell includes at least 4 different processes, specifically including a high temperature process of cadmium telluride preparation, which means that the control of the quality of each layer and the characteristics of the interface is critical [11, 12]. Therefore, through in-depth study on the correlation between the aforementioned factors and the device performance in a certain duration under designated conditions, the degradation mechanisms of devices might be clarified effectively [11]. Currently, various methods have been developed to study the stability of the cadmium telluride solar cell, including theoretical simulations and practical tests [13–15]. For example, the stabilization was achieved to varying degrees using either light-soaking or dark-bias methods, and the existing IEC 61646 light-soaking interval might be appropriate for CdTe modules [16].

Current standard tests were employed to simulate the degradation properties of modules under outdoor operation conditions. However, the decomposed analysis after the stability test on packaged modules will be extremely difficult. Therefore, it is important to develop short-term experimental methods to verify the changes in the outdoor performance of devices without the package, and the conditions of these methods need to be adjusted accordingly to avoid unnecessary damages, such as humidity and insulation testing. So far, little research was involved in the stability of the CdTe solar cell under thermal cycling. With the change of thermal cycling from -40°C to $+85^{\circ}\text{C}$, the cell will be repeatedly frosted and thawed, resulting in some complicated effects of thermal shock on the cell chip. For study on the stability of unpackaged devices by selecting the terms of the standard test, there should be targeted trade-offs to avoid introducing more uncertainties. In previous studies, we found that IEC thermal cycling test conditions were applicable to the unpackaged CdTe solar cell to a certain extent.

Based on the above analysis, the stabilization of CdS/CdTe solar cells with different structures was analyzed according to the International Standard IEC 61215-2016 test specifications in this work. These structures were depicted as the following: FTO/CdS/CdTe/Au corresponding to sample 1, FTO/CdS/CdTe/BC/Au corresponding to sample 2, and FTO/MZO/CdS/CdTe/BC/Au corresponding to sample 3, respectively. All the CdS/CdTe solar cells were subjected to the thermal cycling tests from $-40^{\circ}\text{C} \pm 2^{\circ}\text{C}$ to $+85^{\circ}\text{C} \pm 2^{\circ}\text{C}$

FIGURE 1: The structure of sample 3.

and 24-hour temperature cycle test with only 1 cycle from $-40^{\circ}\text{C} \pm 2^{\circ}\text{C}$ to $+85^{\circ}\text{C} \pm 2^{\circ}\text{C}$ under a constant relative humidity of 85%. The stability of cells with different structures has been investigated after thermal experiments by using the light and dark I - V and C - V test methods.

2. Experimental Procedure

In this work, CdS/CdTe heterojunction thin-film solar cells with different structures were fabricated as follows: the $\text{SnO}_2:\text{F}$ (FTO) films coated on commercial glasses commonly used in our laboratory were selected as substrate, and $\text{ZnO}:\text{Mg}$ was prepared by using magnetron sputtering technology as an optional buffer layer between FTO and CdS. A 50 nm thick CdS thin film was deposited by using the chemical bath deposition (CBD) technique at about 85°C , followed by the deposition of the CdTe film ($\sim 5\mu\text{m}$) by using the close-space sublimation (CSS) method for 4 minutes. The CSS chamber was initially evacuated to a pressure of 5×10^{-2} Pa, and a mixture of 99.999% pure argon and 99.999% oxygen (the oxygen partial pressure was 8%) was then charged into the chamber to maintain a pressure of 1 kPa. The space from substrate to source was 2 mm, and the source and substrate were simultaneously heated to about 650°C and 550°C , respectively. Afterwards, CdTe films were annealed for 30 minutes with a CdCl_2 source in a tube furnace preheated to 380°C under 1 atmospheric pressure of mixed N_2+O_2 gas (volume ratio 4:1). And then, $\text{ZnTe}:\text{Cu}$ as the back contact layer was deposited by using the vacuum thermal evaporation technique after the CdTe film was etched by bromine methanol solution with a bromine concentration of 0.2% for 4 s. The ZnTe and Cu powders with high purity (99.999%) were used as evaporation sources with separate crucibles. Two quartz crystal monitors were employed to monitor the deposition rates of ZnTe and Cu on-line, respectively. Finally, unit cells with areas of 0.5 cm^2 were achieved by depositing a 100 nm thick gold electrode with a shadow mask. The structure schematic diagram of sample 3 was shown in Figure 1.

Aging tests including thermal cycling (from -40°C to $+85^{\circ}\text{C}$ with different cycles) and 24-hour temperature cycle with 1 cycle from -40°C to $+85^{\circ}\text{C}$ as shown in Figure 2 were carried out according to IEC 61215-2016 by using a climatic chamber produced by Hong Zhan Technology Co., Ltd. with a programmable temperature controller having an accuracy

FIGURE 2: The profile of one cycle time: (a) thermal cycling and (b) 24-hour temperature cycle.

FIGURE 3: The visual inspection of front (a) and back (b) sides of cells (the view of the right area observed through convex lens) under 1000 lux of fluorescent light.

of $\pm 2.0^{\circ}\text{C}$ attached with a suitable temperature sensor to the front of the representative cell near the middle with means for circulating the air inside to improve the uniformity of the temperature field and minimize condensation on the devices during the test. Light I - V characteristics of CdTe solar cells were carried out by using a Solar Cell Tester (Gsol XJCM-9) under AM1.5 with light intensity of 1000 W/m^2 and temperature of 25°C according to IEC 60904-1 and IEC TS 61836, and dark I - V characteristics of all solar cells were performed at room temperature by Agilent 4155C. Meanwhile, C - V curves were obtained at room temperature via an Agilent 4155A with a test frequency of 1 MHz and scan bias range from -1 V to $+1.5\text{ V}$.

3. Results and Discussion

3.1. Thermal Cycling

3.1.1. Visual Inspection. In this section, the inspection was focused on the visual defects, such as warping, delamination, bubbles, scratches, and stains in cells under an illumination of no less than 1000 lux as defined in IEC 61215-1. Figure 3 shows the implementation of inspection. Before the demonstration of device performance, a laser was employed to etch and remove the films at the edge of the electrode to eliminate bypass collection of devices. Because of a relatively weak adhesion between the gold electrode and the ZnTe:Cu films, a peeling off at the edge of the back electrode usually occurred during the etching process, which was marked with a red circle in Figure 3(a). This defect seriously affected the current

collection of the back electrode and cannot meet the specification of the test standard, so in the later device test, cells with partial electrode peeling off have been ignored. No other defects as mentioned above were found in the electrode of other cells. Figure 3(b) displays the back of cells through the glass side, and a uniform and dark black colour with no red or yellow spot, no scratch, or no damage can be observed, meaning that a uniform and complete cathode in the cell has been obtained.

3.1.2. Light I - V Characteristics. The accelerated thermal cycle tests were conducted on 16 unit cells with designated structures fabricated from one batch to determine the ability of them to withstand thermal mismatch, fatigue, and other stresses caused by repeated changes of temperature, as shown in Figure 3. After 100 thermal cycles, 5 cells from sample 1 failed and the reasons of the failure included the aforementioned electrode peeling off. As for the cells from sample 2 and sample 3, 2 cells of each group failed. The I - V curves of the representative cells before and after thermal cycling were shown in Figure 4. Note that for the cells that underwent thermal cycling, the I - V measurement was carried out after 1 hours' recovery time at 23°C .

From Figure 4, a roll-over phenomenon of current-voltage characteristics near the open circuit voltage of sample 1 can be observed obviously, which was due to a metal-semiconductor barrier caused by a nonohmic contact between CdTe and Au because of the work function of CdTe $\sim 5.5\text{ eV}$ greater than that of most metals, including gold $\sim 5.1\text{ eV}$ as the back electrode in this work [17]. As the number of thermal cycles increased, the fill factor (FF), short-circuit current (J_{sc}), and open circuit voltage (V_{oc}) of sample 1 kept declining. After 100 thermal cycles, FF, J_{sc} , and V_{oc} of cells from sample 1 decreased by 10.11%, 5.90%, and 11.48%, respectively, eventually resulting in a degradation in conversion efficiency (η) of 25.13% compared with the initial η as shown in Figure 5. No roll-over phenomenon near V_{oc} of sample 2 and sample 3 was perceived in Figures 4(b) and 4(c) under illumination. After 100 thermal cycles, FF, J_{sc} , and V_{oc} of sample 2 decreased by 8.2%, 4.1%, and 5.6%, respectively, resulting in a degradation in η of 16.80% as compared with the initial η while the corresponding parameters of sample 3 reduced by 6.2%, 7.1%, and 0.1%, respectively, accompanied by a 10.6%

FIGURE 4: Comparison of light J - V curves of (a) sample 1, (b) sample 2, and (c) sample 3 before and after different cycles of thermal cycling.

FIGURE 5: The photovoltaic parameters of cells as a function of thermal cycling numbers: (a) η and FF; (b) J_{sc} and V_{oc} .

reduction in conversion efficiency. The above changes in performances of sample 2 and sample 3, especially in series resistance, should be attributed to a good back contact ZnTe:Cu between CdTe and Au which can effectively reduce the contact barrier and eliminate the influence of the Schottky junction [18]. As MZO layer was introduced between FTO and CdS, the initial performance of sample 3 was lower than that of sample 2.

In our other work, the CdTe cell with conversion efficiency exceeding 16% has been achieved when introducing MZO as an optimized buffer layer [19]. In Kephart et al.'s report, MZO has completely replaced the window layer CdS with a further optimized structure [20]. However, in this work, in order to compare the stability of devices with different configurations, the thicknesses of the functional layers were kept the same and the device performance was therefore not optimized. Interestingly, the stability of sample 3 was superior, especially reflected by the almost unchanged V_{oc} after 100 thermal cycles. However, J_{sc} degradation of sample 3 was more severe close to 7.1% as compared to that of sample 2. This indicated that the MZO absorbed some of the photons which were supposed to be entering CdS/CdTe het-

erojunction and induced an extra barrier between FTO and CdS, which resulted in an increased electron reflection.

Meanwhile, the fluctuation of J_{sc} was much smaller than that of other parameters of all the samples. During the thermal cycling, the cooling process will cause obvious decrease in the minority carrier concentration, while as temperature increases, the short-circuit current increases moderately owing to an improvement of contact performance by alleviating the residual stress between the layers in the cell and an increase in lifetime and diffusion coefficient of photogenerated carriers. Furthermore, the reverse saturation current I_0 increased greatly with an increase of thermal cycling numbers as analyzed later, revealing that after a thermal cycle, the change of the carrier was irreversible. Therefore, a shift in the current-voltage curve of the cell was negligible, where the degradation in η of all cells exceeding 10% was not only related to the influence of the grain boundary on the diffusion of dopants, impurities, electromigration of charged atoms, and self-compensation effect during thermal cycling but also related to the water vapor in the environment that will enter the interior of unpackaged cells causing a considerable damage to CdS/CdTe heterojunction [12].

FIGURE 6: Comparison of C - V and C^{-2} - V curves before and after different cycles of thermal cycling: (a) sample 1, (b) sample 2, and (c) sample 3.

3.1.3. C - V Characteristics. As shown in Figure 6, the capacitance of the cell with the nonlinear characteristic increased obviously when forward bias was greater than 0.3 V, while the capacitance decreased when bias increased in the vicinity of V_{oc} (0.8 V), which correspond to an inversion region. The capacitance tended to be saturated when bias was less than 0.3 V, especially in reverse bias, assigned to an accumulation region. As the number of thermal cycles increased, the capacitance variation of sample 1 and sample 2 became significantly larger than that of sample 3, which was closely related to the change of the p - n junction region. The structure of the CdTe thin-film solar cell can be equated to a plate capacitor, and its physical properties such as doping concentration N_D , depletion region width X_D , and built-in electric field V_D can be explained by the C - V characteristic [21, 22].

Under the condition of depletion layer approximation, the barrier capacitance C_T of CdTe/CdS considered as an abrupt heterojunction is depicted as the following:

$$C_T = \frac{A\epsilon_r\epsilon_0}{X_D}, \quad (1)$$

$$C_T = A\sqrt{\frac{\epsilon_r\epsilon_0qN_D}{2(V_D - V)}},$$

where A is the cell area, the relative dielectric constant ϵ_r of CdTe is about 9, and the vacuum permittivity ϵ_0 is 8.85×10^{-12} F/m. Simply change the above formula to get the following formula:

$$\frac{1}{C_T^2} = \frac{2V_D}{A^2\epsilon_r\epsilon_0qN_D} - \frac{2V}{A^2\epsilon_r\epsilon_0qN_D}. \quad (2)$$

Then, differentiate the above formula:

$$\frac{d(1/C_T^2)}{dV} = \frac{2}{A^2\epsilon_r\epsilon_0qN_D}. \quad (3)$$

N_D and V_D can be obtained from the slope and intercept by fitting the straight line portion of the $1/C^2 \sim V$ relationship curve plotted in Figure 6 under a bias range of 0.4 V~0.6 V, respectively. All the values of X_D , N_D , and V_D were listed in Table 1.

These parameters of sample 1 and sample 2 were considerably different from those of sample 3. Taking the change of X_D at a forward bias of 0.6 V as an example, X_D of sample 1 increased by 45.45%, 23.63%, and 40.00% after 25, 50, and 100 cycles, respectively. Meanwhile, X_D of sample 2 and sample 3 increased by 7.69%, 27.69%, and 35.38% and -8.77%, 3.50%, and 3.50%, respectively. It was worth noting that N_D and V_D of the samples decreased as X_D increased after thermal cycles, and the change trend of N_D and V_D was basically the same as that of J_{sc} and V_{oc} described above, respectively, which means that the thermal shock has a significant effect on the minority carrier concentration and electric field strength inside p - n heterojunction.

3.1.4. Dark I - V Characteristics. Dark current was very small and relatively insensitive to variation at a bias less than 0.4 V, especially under reverse bias, while dark current increased exponentially as forward bias exceeding 0.4 V as depicted in Figure 7. However, significant differences in dark current variations of cells with different configurations can be observed clearly as a function of thermal cycling numbers. When forward bias was greater than 0.4 V, dark current of sample 1 rose rapidly with an inflection point defined as roll-over phenomenon at a bias around 0.6 V. As the number of thermal cycles increased, roll-over phenomenon became more obvious. However, the change of dark current of sample 2 was still small at a bias closed to 0.6 V, and no roll-over phenomenon of current can be observed even when bias increased to 0.8 V. For sample 3, its current had risen by a certain amplitude near 0.6 V, but a very small inflection point can be perceived at a bias exceeding 0.7 V. Furthermore, a relatively obvious roll-over phenomenon was presented after the number of thermal cycles increased to 100 times.

TABLE 1: Dark I - V and C - V parameters of samples before and after thermal cycling.

Sample	Experimental condition	A	J_0 (mA/cm ²)	X_D (μ)	N_D (10 ¹⁴ cm ⁻³)	V_D (V)
1	Initial	2.10	2.59×10^{-11}	0.65	1.36	0.65
	After 25 temperature cycles	2.34	4.05×10^{-11}	0.70	1.29	0.60
	After 50 temperature cycles	3.01	1.786×10^{-10}	0.83	1.22	0.66
	After 100 temperature cycles	5.76	1.85×10^{-8}	0.88	1.28	0.66
2	Initial	1.98	8.55×10^{-12}	0.55	1.30	0.60
	After 25 temperature cycles	2.20	2.09×10^{-11}	0.80	1.24	0.74
	After 50 temperature cycles	2.22	4.7×10^{-11}	0.68	1.14	0.59
	After 100 temperature cycles	2.20	3.6×10^{-11}	0.77	1.24	0.68
3	Initial	2.12	3.52×10^{-11}	0.57	1.37	0.56
	After 25 temperature cycles	2.10	2.54×10^{-11}	0.52	1.32	0.52
	After 50 temperature cycles	2.14	3.84×10^{-11}	0.59	1.24	0.51
	After 100 temperature cycles	2.36	4.54×10^{-11}	0.59	1.27	0.53

FIGURE 7: Comparison of dark current-voltage curves before and after different cycles of thermal cycling: (a) sample 1, (b) sample 2, and (c) sample 3.

The above changes might be analyzed by using the current-voltage equation of ideal p - n junction in the dark state described as follows:

$$I = I_0 \left(e^{q(V-IR_s)/AKT} - 1 \right) + \frac{V - IR_s}{R_{sh}}, \quad (4)$$

where I_0 is dark reverse saturation current, K is Boltzmann's constant, A is defined as the diode ideality factor representing the diffusion and recombination current components, R_s is series resistance, R_{sh} is shunt resistance, and in this work T is 298 K. Before thermal cycling, A of all samples was around 2.0 as listed in Table 1, indicating that the junction current was mainly composed of recombination current [23, 24]. After 100 cycles of thermal cycling, A of sample 1 increased to 5.76, indicating that the carrier transport has changed to the hot-electron emission mechanism. The dark reverse satu-

ration current density J_0 of sample 1 increased by 3 orders of magnitude while that of sample 2 and sample 3 increased by 321% and 29%, respectively, meaning CdS/CdTe heterojunction was destroyed to some extent. The evolution of dark current was attributed to varying barrier height exposed by the change of R_s at the interface of the cell [25]. In this case, carriers needed extra energy to "climb" the barrier, resulting in a significant decrease in the amount of electrons which arrived at the back electrode by the hot-electron emission mechanism. Furthermore, when a back contact layer was introduced into devices, as shown in Figure 7(b), the roll-over phenomenon of sample 2 was well suppressed. While MZO was introduced as a buffer layer between FTO and CdS, J_0 of sample 3 remained a relatively small variation as the number of thermal cycling cycles increased, but a slight roll-over phenomenon can be perceived, which was due to an increase of R_s caused by MZO. These conclusions were consistent with the results discussed above.

TABLE 2: Light I - V parameters of samples before and after the 24-hour thermal cycle.

Sample	Experimental condition	η (%)	FF (%)	J_{sc} (mA/cm ²)	V_{oc} (mV)
1	Before	10.10	59.01	23.60	725
	After	8.41	55.34	23.16	656
2	Before	11.60	63.44	24.12	758
	After	10.21	59.59	23.81	721
3	Before	10.89	62.62	24.13	721
	After	9.90	59.13	23.80	703

3.2. 24-Hour Temperature Cycle. The 24-hour temperature cycle test (1 cycle from -40°C to $+85^{\circ}\text{C}$) was conducted on samples with the aforementioned structure, named as samples 1, 2, and 3, respectively, and the parameters derived from light I - V curves of these samples were listed in Table 2. After the 24-hour temperature cycle, FF, J_{sc} , V_{oc} , and η of sample 1 decreased by 6.2%, 1.8%, 9.5%, and 16.7%, respectively, and the corresponding parameters of sample 2 and sample 3 decreased by 6.1%, 1.3%, 4.9%, and 12.0% and 5.6%, 1.4%, 2.5%, and 9.1%, respectively. Compared to the change of other parameters of all samples, the variation of J_{sc} was very weak. The parameter variation of sample 3 was consistent with the results of the above thermal cycling experiments. This further verified that a back contact layer was critical to the stability of the CdS/CdTe solar cell, and a composite front electrode was also conducive to potentially improve cell stability.

4. Conclusion

In summary, the effects of thermal shock according to the IEC standard on the stability of the unpackaged CdTe solar cell with different structures were analyzed while the reasons of cell performance degradation were also discussed. The experimental results showed that there were significant differences in the change of parameters of cells under different aging conditions. The main junction CdS/CdTe of the cell was destroyed in the absence of buffer layers close to front and back electrodes. Therefore, the cell with a structure of FTO/MZO/CdS/CdTe/BC/Au demonstrates an optimized stability among solar cells with different configurations, which mean that an efficient back contact layer and a composite front electrode are the indispensable structural element to attain high stability in the CdS/CdTe solar cell. However, the test results also expose that the introduction of the buffer layer between front electrode and CdS is a dialectical consideration. These conclusions not only are conducive to the study on CdTe solar cell stability but also provide a certain experimental basis for standard test and outdoor applications of CdTe solar cell.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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