

Research Article

Efficient Topology for DC-DC Boost Converter Based on Charge Pump Capacitor for Renewable Energy System

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In an attempt to meet the global demand, renewable energy systems (RES) have gained an interest in it due to the availability of the resources, especially solar photovoltaic system that has been an importance since many years because of per watt cost reduction, improvement in efficiency, and abundant availability. Photovoltaic system in remote and rural areas is very useful where a grid supply is unavailable. In this scenario, power electronic converters are an integral part of the renewable energy systems particularly for electronic devices which are operated from renewable energy sources and energy storage system (fuel cell and batteries). In this article, a new topology of charge pump capacitor (CPC) which is based on high voltage gain technique DC-DC boost converter (DCBC) with dynamic modeling is proposed. To testify the efficacy of the introduced topology, a prototype has been developed in a laboratory, where input was given 10VDC and 80VDC output voltage achieved at the load side. Furthermore, the experimental result shows that the voltage stress of MOSFET switches is very less in comparison with the conventional boost converter with the same parameters as the proposed converter.

1. Introduction

Solar photovoltaic (PV) that has a tremendous potential to generate electricity directly from the sunlight is considered as a means of powering the future with clean and environment friendly renewable sources [1–3]. However, photovoltaic panels, batteries, and fuel cell output voltage are less. To overcome this issue, DC-DC boost converter is installed to step up the low input voltage to require higher output voltage gain as depicted in Figure 1 [4]. The world surpasses

in an approximation of 900 million mobile devices with over 500 million users in 2019. With higher energy demand and increasing prices of conventional electricity, it becomes a challenge for the telecommunication service providers to maintain their existing infrastructure as well as to expand it in many rural locations where access to conventional electricity is not easy due to many reasons. Due to technological development in renewable energy technologies specifically solar and wind, this proved as an economical and reliable sources to power the telecom systems in remote locations

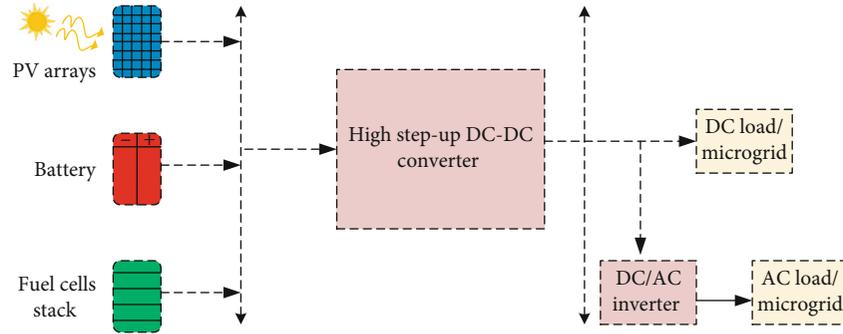


FIGURE 1: Renewable energy system [4].



FIGURE 2: Solar remote power station [5].

where conventional grid access is unavailable or difficult to provide, as well as solar power can provide the protection to the defense communication system from any damage or cyberattack as compared to the electric grid as shown in Figure 2 [5]. Therefore, it is significant to use PV technology (off-grid, on-grid, and remote solar power station). In this scenario, a high step-up boost converter has an important part [6, 7]. In literature, many types of boost converter introduced to attain the step-up voltage at the load [8]. These converters are operated with very high duty cycle which caused to increase the converter losses; also, many circuit components occur to reduce the overall system efficiency [9]. In the high PWM signal, MOSFET switches cause the malfunction because of short conduction time [10, 11]. Compared with a classical buck, boost, and buck-boost circuits, transformer-based converters can achieve higher conversion ratios with lower losses [12, 13]. The same feature applies to converters with coupled inductors [14].

The turn's proportion of the transformer or the coupled inductors helps realize higher stepping ratios [15, 16].

DC to DC boost converter with coupled inductor [17, 18] and active clamp flyback converter in [19], the main limitation of these converters is the problems related to the transformer. The massive turn's ratio and high-voltage isolation requirements increase the leakage inductance and parasitic capacitance of the winding. At switching instants, the transformer parasitic will result in high voltage spikes across the switches [20]. The voltage and current spikes lead to increased losses and reduced reliability and may damage circuit components [21–23]. A study of some DC-DC converter is discussed in detailed [24]. It described that full-bridge converter can be more efficient. The disadvantage of this design is that the soft switchings are hard to achieve. In this con-

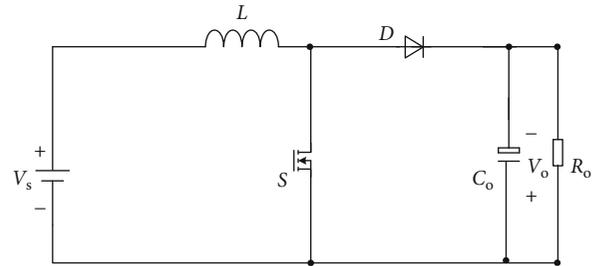


FIGURE 3: Conventional boost converter [27].

verter, there is no suitable value for the snubber capacitors for the whole operation range. Furthermore, in this converter, it needs an output inductor, which can cause voltage spike at diodes. [25].

Finally, DC-DC converter with transformer design is presented in the literature, and the cons of this converter including core losses in the transformer can be significantly high, and the design of winding for transformer is complicated; also, efficiency is low and price is high. Switching semiconductor devices have exacerbated this issue as higher transformer core loss at high switching frequencies make it difficult to size the transformer while simultaneously increasing power density appropriately. Additionally, the inherent mutual coupling effect between adjacent transformer windings makes these topologies less suited to multi-input or multi-output type of applications [26–28]. However, this problem can only be addressed by connecting snubber circuits to the switches or by utilizing the transformer parasitic as a resonant tank and operating these converters as resonant soft-switched converters.

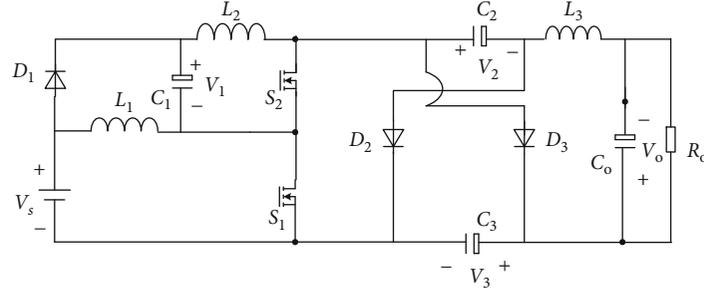


FIGURE 4: Proposed converter.

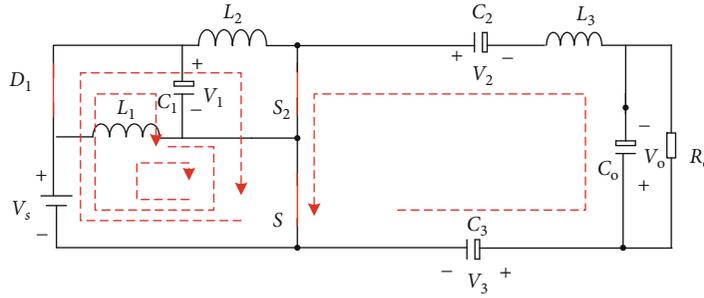


FIGURE 5: State I.

2. Related Work

2.1. The Principle of Boost Converter Circuits. The popular and generally used converters are the conventional DC-DC boost converters. The fundamental thought of these conventional boost converter circuits governed by splitting the input DC voltage with a precise PWM signal to produce an anticipated voltage at the load side. The PWM signal of conventional boost converters generally kept at a constant rate. Figure 3 illustrates the conventional DC-DC boost converter circuit [27]. These circuits are modest in assembly but undergo from some limits avoiding their usage in high-power applications. For the higher DC voltage conversion ratio, conventional converters work with higher duty cycle, which results in increasing the losses in the circuit components and tend to degrade the overall system efficiency [29, 30]. The higher duty cycle may also cause failure in switches due to the short conduction time [31].

$$M = \frac{1}{1-D} V_s, \quad (1)$$

$$V_{S-\text{tress}} = V_o. \quad (2)$$

In Eqs. (1), (2) where D is the duty ratio of the active switch, however, the actual conversion ratio is much lower when the effect of inductor equivalent series resistance R_L , diode forward voltage drop V_D , diode forward resistance R_d , switch on-state resistance R_{on} is accounted [28]. The effect of all these nonidealities is that the voltage gain from input to output is rarely more than 1.5 to 2.

3. The Proposed Method

3.1. The Circuit Description. This paper presents new DC-DC boost converters based on the charge pump capacitor for high voltage gain. The feature combination of CPC-DCBC with voltage multiplier cell (CPC) does not exist in any available high voltage gain topologies of DC-DC converter. The main advantage of the introduced topology is it has the capability to achieve high voltage gain without working at higher duty ratio.

The essential features of the proposed converters are proved experimentally in the laboratory with low switching losses and single stage without high-current chopping. Construction of the recommended converter is given in Figure 4, where V_s is an input voltage, four capacitors (C_1 , C_2 , C_3 , and C_0), two MOSFET switches (S_1 and S_2), inductors (L_1 , L_2 , and L_3), and diodes (D_1 , D_2 , and D_3). The presented topology operates in continuous conduction mode (CCM), where all components work in idle condition.

4. The Operating Principle

4.1. State I (t_0-t_1). In this state, as depicted in Figure 5, when switches S_1 and S_2 are on, diode D_1 works in forward biased, and diodes D_2 and D_3 work in reverse biased, respectively. Inductor L_1 increase by input voltage and inductor current increases linearly at the same time (V_s) established across the inductor L_2 and the inductor current increases linearly, respectively. In this state, capacitors V_{C1} and V_{C2} work in series resultant capacitor voltage of $V_{C1} + V_{C2} = 2V_{C2}$ inductor L_3 decrease by $2V_{C2} - V_o$ and

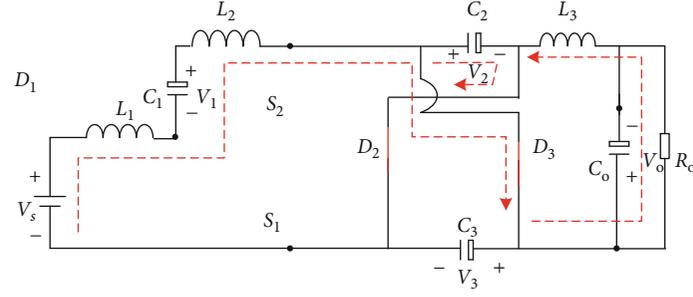


FIGURE 6: State II.

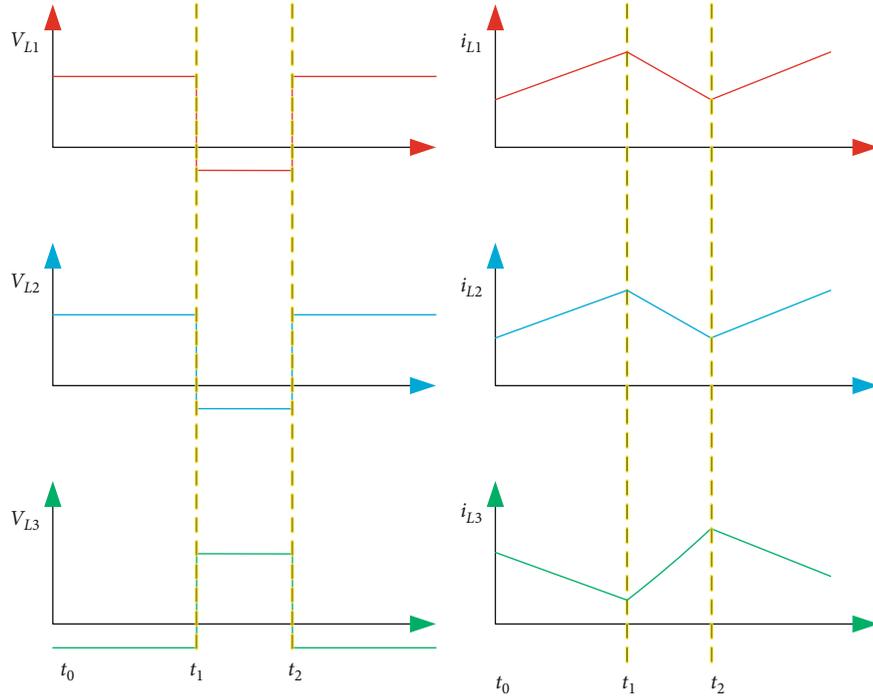


FIGURE 7: Steady state.

their current decrease in this state. This state is derived in Eqs. (3)-(8).

$$V_1 = V_s, \quad (3)$$

$$i_{L1} = i_{L1-t_0} + \frac{V_s}{L_1} t, \quad (4)$$

$$i_{L2} = i_{L2-t_0} + \frac{V_s}{L_2} t \quad (5)$$

$$i_{L3} = i_{L3-t_0} + \frac{2V_{c2} - V_0}{L_3} t, \quad (6)$$

$$i_{Q1,2} = i_{L1} + i_{L2} + i_{L3}, \quad (7)$$

$$i_{in} = i_Q - i_{L3}. \quad (8)$$

L_1 discharged to the load by $2V_s - V_{c2}$. In the same time inductor, L_2 also released to load the same as inductor L_1 and the voltage across inductor L_3 charged to load by $V_{c2} - V_0$. In this state, inductors i_{L1} and i_{L2} decrease linearly and i_{L3} increases respectfully; this state is derived Eqs. (9)-(13).

$$i_{L1} = i_{L1-t_1} - \frac{2V_s - V_{c2}}{L_1} t, \quad (9)$$

$$i_{L2} = i_{L2-t_1} - \frac{2V_s - V_{c2}}{L_2} t, \quad (10)$$

$$i_{L3} = i_{L3-t_1} + \frac{V_{c2} - V_0}{L_3} t, \quad (11)$$

$$i_Q = 0, \quad (12)$$

$$i_{in} = i_{L2}. \quad (13)$$

4.2. State II (t_1-t_2). In this state, as depicted in Figure 6, when both the semiconductor switches S_1 and S_2 are turned off, diode D_1 is reverse biased. The current across the inductor

TABLE 1: Power/component.

Power (W)	Components
P_{L1}	L_1
P_{L2}	L_2
P_{L3}	L_3
P_{C1}	C_1
P_{C2}	C_2
P_{C3}	C_3
P_{C0}	C_0
P_{D1}	D_1
P_{D2}	D_2
P_{D3}	D_3
P_{S1}	S_1
P_{S2}	S_2
$P_{S'1}$	S'_1
$P_{S'2}$	S'_2

5. Proposed Converter Voltage Conversion Ratio

At the proposed converter inductors L_1 , L_2 , and L_3 , applying volt second balance method in each state, the connection between the proposed converters is given below in Eqs. (14)-(20). Steady-state behavior of inductor voltage and their currents are depicted in above Figure 7.

$$V_{L1} = V_s, \quad (14)$$

$$V_{L2} = V_s, \quad (15)$$

$$V_{L3} = 2V_{c2} - V_0, \quad (16)$$

$$V_{L1} = 2V_s - V_{c1}, \quad (17)$$

$$V_{L2} = 2V_s - V_{c2}, \quad (18)$$

$$V_{L3} = V_{c2} - V_0, \quad (19)$$

$$G = \frac{V_0}{V_s} = 2 \frac{1+D}{1-D}. \quad (20)$$

Voltage stress across the MOSFET switch in Eqs. (21)-(24)

$$V_{S1,2} = \frac{1}{3.2} V_0, \quad (21)$$

$$V_{D1(\text{stress})} = V_1 = -V_{c1} = -V_s, \quad (22)$$

$$V_{D2(\text{stress})} = V_2 = -V_{c2} = -\frac{2V_s}{1-D}, \quad (23)$$

$$V_{D3(\text{stress})} = V_3 = -V_{c3} = -\frac{2V_s}{1-D}. \quad (24)$$

5.1. Proposed Converter Power Loss Analysis. Total power loss in converter is equal to losses in each component of converter Table 1.

$$P_{\text{loss}} = P_{L1} + P_{L2} + P_{L3} + P_{C1} + P_{C2} + P_{C3} + P_{C0} + P_{D1} + P_{D2} + P_{D3} + P_{S1} + P_{S2} + P_{S'1} + P_{S'2}. \quad (25)$$

$$P_{L1} = I_{L1(\text{rms})}^2 \cdot R_{L1},$$

$$P_{L2} = I_{L2(\text{rms})}^2 \cdot R_{L2},$$

$$P_{L3} = I_{L3(\text{rms})}^2 \cdot R_{L3},$$

$$P_{C1} = I_{C1(\text{rms})}^2 \cdot R_{C1},$$

$$P_{C2} = I_{C2(\text{rms})}^2 \cdot R_{C2},$$

$$P_{C3} = I_{C3(\text{rms})}^2 \cdot R_{C3},$$

$$P_{C0} = I_{C0(\text{rms})}^2 \cdot R_{C0},$$

$$P_{D1} = I_{D1(\text{rms})}^2 \cdot R_{D1},$$

$$P_{D1} = I_{D1(\text{rms})}^2 \cdot R_{D1},$$

$$P_{D2} = I_{D2(\text{rms})}^2 \cdot R_{D2},$$

$$P_{D3} = I_{D3(\text{rms})}^2 \cdot R_{D3},$$

$$P_{S1} = I_{s1(\text{rms})}^2 \cdot R_{Ds(\text{on})1},$$

$$P_{S2} = I_{s2(\text{rms})}^2 \cdot R_{Ds(\text{on})2},$$

$$P_{S'1} = \frac{1}{2} \left[V_{S1(\text{max})} \cdot I_{S1(\text{max})} \cdot f_s \cdot (t_r + t_f) \right],$$

$$P_{S'2} = \frac{1}{2} \left[V_{S2(\text{max})} \cdot I_{S2(\text{max})} \cdot f_s \cdot (t_r + t_f) \right],$$

$V_{S1(\text{max})}$ = maximum voltage stress of S_1 , $I_{S1(\text{max})}$ = maximum current stress of S_1 , f_s = switching frequency, t_r = rise time of MOSFET switch, and t_f = fall time of MOSFET switch.

$$I_{L1(\text{rms})} = \sqrt{I_{L1(\text{avg})}^2 + \left(\frac{\Delta I_{L1}/2}{\sqrt{3}} \right)^2}. \quad (27)$$

Similarly, for I_{L2} (rms) and I_{L3} (rms),

$$I_{c1(\text{rms})} = \frac{I_{C1(\text{max})}}{\sqrt{3}} = \frac{\Delta I_{L1}/2}{\sqrt{3}},$$

$$I_{c2(\text{rms})} = I_{C3(\text{rms})} = \frac{\Delta I_{L2}/2}{\sqrt{3}},$$

$$I_{c0(\text{rms})} = \frac{\Delta I_{L3}/2}{\sqrt{3}},$$

$$I_{D1(\text{rms})} = \sqrt{D}(I_s - I_{L1}),$$

$$I_{D2(\text{rms})} = I_{D3(\text{rms})} = \sqrt{1-D} \cdot (I_{L1}),$$

$$I_{s1(\text{rms})} = \sqrt{D} \cdot I_{L1},$$

$$I_{s2(\text{rms})} = \sqrt{D} \cdot I_{L2}.$$

After applying voltage second balance law on all inductors, we get

$$V_2 = V_3 = \frac{2D_1}{D_1 - D} V_s,$$

$$M = \frac{V_0}{V_s} = \frac{(2D_1)(D + 2 - D_1) - (2D_1 - 2)(D_1 - D)}{D_1 - D},$$

$$D_1 = \frac{2L_1 - D}{DV_s T_s}. \quad (36)$$

5.3. Dynamic Modeling for the Presented Converter. For dynamic modeling, ripples of inductor current and voltage ripples of capacitor are assume very less. The equivalent circuit of presented converter is shown below in Figure 10 derived from Figure 5.

Subsequently, applying circuit theory in Figure 7, this derived in Eq. (37).

$$\begin{bmatrix} \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{i}_{L3} \\ \dot{V}_{c1} \\ \dot{V}_{c2} \\ \dot{V}_{c3} \\ \dot{V}_{c4} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-(1-u)}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{u}{L_2} & -\frac{u}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{u}{L_3} & -\frac{1}{L_3} & -\frac{1}{L_3} \\ \frac{(1-u)}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{u}{C_2} & -\frac{1}{C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{-u}{C_3} & -\frac{1}{C_3} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{u}{C_4} & -\frac{1}{C_4} & -\frac{1}{R_L C_4} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ V_{c1} \\ V_{c2} \\ V_{c3} \\ V_{c4} \end{bmatrix} + \begin{bmatrix} \frac{u}{L_1} \\ \frac{1+u}{L_2} \\ -\frac{1}{L_3} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} [e_t]. \quad (37)$$

Equation (37) can be written as Eq. (38) without considering losses.

$$\dot{x}(t) = A(u)x(t) + B(u)e(t), \quad (38)$$

where $x(t) = [i_{L1}, i_{L2}, i_{L3}, V_{c1}, V_{c2}, V_{c3}, V_{c4}]^T \in R^7$ is the normal value of state vector, $A(u)$ is a matrix in $R^{7 \times 7}$, and $B(u)$ is a vector in R^7 ; $V_s \in R$ = input voltage, whereas resistive load is R_L and u is a function of switch S with the binary value, which is $[0, 1]$. This means that when the switch value is $[0]$, the switch is off, and when the value is $[1]$, the switch is on. The above equation is based on nonlinear, and matrix $A(u), B(u)$ is based on control signal of $u(t) \in R$. The linearisation process method obtained the proposed converter behavior to small perturbations around an operation point. Therefore, the nominal steady-state operating system of the proposed converter can be written by setting (8), $AX + BE = 0$ and can be written as shown in Eqs. (49)-(55).

The voltage across the capacitor is

$$V_{c1} = V_s, \quad (39)$$

$$V_{c2} = \frac{2}{1-D} V_s, \quad (40)$$

$$V_{c3} = \frac{2}{1-D} V_s, \quad (41)$$

$$V_{c4} = 2 \frac{1+D}{1-D} V_s, \quad (42)$$

Current across the inductor is

$$i_{L1} = \frac{V_s}{(1-D)^4 R_L}, \quad (43)$$

$$i_{L2} = \frac{V_s}{(1-D)^4 R_L}, \quad (44)$$

$$i_{L3} = \frac{V_s}{(1-D)^2 R_L}, \quad (45)$$

where V_s = DC input voltage and D = duty cycle of the switch S , \tilde{u} = small - signal perturbations to the nominal duty cycle D , and \tilde{e} = to the nominal input voltage V_s to the nominal input voltage, so we can write the relationship between voltage and duty cycle as below (46), (47).

$$e(t) = E + \tilde{e}, \quad (46)$$

$$u(t) = U + \tilde{u}, \quad (47)$$

where $\tilde{e} \ll E$ and $\tilde{u} \ll D$, so we can also write as (48), (49).

$$X(t) = X + \tilde{x}, \quad (48)$$

$$V_0(t) = V_0 + \tilde{v}_0. \quad (49)$$

After substituting Eqs. (39)-(45) and (46), (47) into Eq. (40), we can derive linear mode after assuming that the

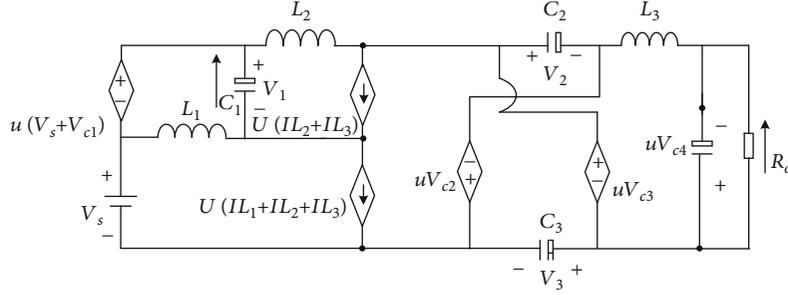


FIGURE 10: Average equivalent circuit.

perturbations are less enough and nonlinear terms can be avoided so that we can write Eq. (50).

$$\begin{bmatrix} \widetilde{i_{L1}} \\ \widetilde{i_{L2}} \\ \widetilde{i_{L3}} \\ \widetilde{V_{c1}} \\ \widetilde{V_{c2}} \\ \widetilde{V_{c3}} \\ \widetilde{V_{c4}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-(1-u)}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{u}{L_2} & -\frac{u}{L_2} & 0 \\ 0 & 0 & 0 & 0 & \frac{u}{L_3} & -\frac{1}{L_3} & -\frac{1}{L_3} \\ \frac{(1-u)}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{u}{C_2} & -\frac{1}{C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{-u}{C_3} & -\frac{1}{C_3} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{u}{C_4} & -\frac{1}{C_4} & -\frac{1}{R_L C_4} \end{bmatrix}$$

$$\begin{bmatrix} \widetilde{i_{L1}} \\ \widetilde{i_{L2}} \\ \widetilde{i_{L3}} \\ \widetilde{V_{c1}} \\ \widetilde{V_{c2}} \\ \widetilde{V_{c3}} \\ \widetilde{V_{c4}} \end{bmatrix} + \begin{bmatrix} \frac{V_s}{(1-D)L_2} & \frac{u}{L_1} \\ \frac{2}{(1-D)L_2} V_s & \frac{1+u}{L_2} \\ 2\frac{1+D}{(1-D)L_3} V_s & -\frac{1}{L_3} \\ \frac{V_s}{(1-D)^4 R_{Lc1}} & 0 \\ \frac{V_s}{(1-D)^4 R_{Lc2}} & 0 \\ \frac{V_s}{(1-D)^2 R_{Lc3}} & 0 \end{bmatrix} \begin{bmatrix} \widetilde{u} \\ \widetilde{e} \end{bmatrix}$$

(50)

and $V_{(t)} = [\widetilde{u}\widetilde{e}]$. When the perturbation input voltage is neglected $\widetilde{e} = 0$, so matrix B can be removed and written as (62).

$$\begin{bmatrix} \widetilde{i_{L1}} \\ \widetilde{i_{L2}} \\ \widetilde{i_{L3}} \\ \widetilde{V_{c1}} \\ \widetilde{V_{c2}} \\ \widetilde{V_{c3}} \\ \widetilde{V_{c4}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-(1-u)}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{u}{L_2} & -\frac{u}{L_2} & 0 \\ 0 & 0 & 0 & 0 & \frac{u}{L_3} & -\frac{1}{L_3} & -\frac{1}{L_3} \\ \frac{(1-u)}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{u}{C_2} & -\frac{1}{C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{-u}{C_3} & -\frac{1}{C_3} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{u}{C_4} & -\frac{1}{C_4} & -\frac{1}{R_L C_4} \end{bmatrix}$$

$$\begin{bmatrix} \widetilde{i_{L1}} \\ \widetilde{i_{L2}} \\ \widetilde{i_{L3}} \\ \widetilde{V_{c1}} \\ \widetilde{V_{c2}} \\ \widetilde{V_{c3}} \\ \widetilde{V_{c4}} \end{bmatrix} + \begin{bmatrix} \frac{V_s}{(1-D)L_2} \\ \frac{2}{(1-D)L_2} V_s \\ 2\frac{1+D}{(1-D)L_3} V_s \\ \frac{V_s}{(1-D)^4 R_{Lc1}} \\ \frac{V_s}{(1-D)^4 R_{Lc2}} \\ \frac{V_s}{(1-D)^2 R_{Lc3}} \end{bmatrix} \begin{bmatrix} \widetilde{u} \\ \widetilde{e} \end{bmatrix}$$

(52)

Equation (50) can be written as Eq. (51).

$$\dot{x}(t) = Ax(t) + Bv(t), \quad (51)$$

where $x_{(t)} \in R^7$ is the state vector, $A \in R^{7 \times 7}$ and B are constant matrix in $R^{7 \times 2}$, R^2 is vector of input voltage,

6. Results and Discussions

6.1. Simulation Results and Discussion. Figures 11(a) and 11(b) presented simulation results of proposed topology and conventional boost converter. These simulation results performed in Matlab Simulink at the same parameters, as

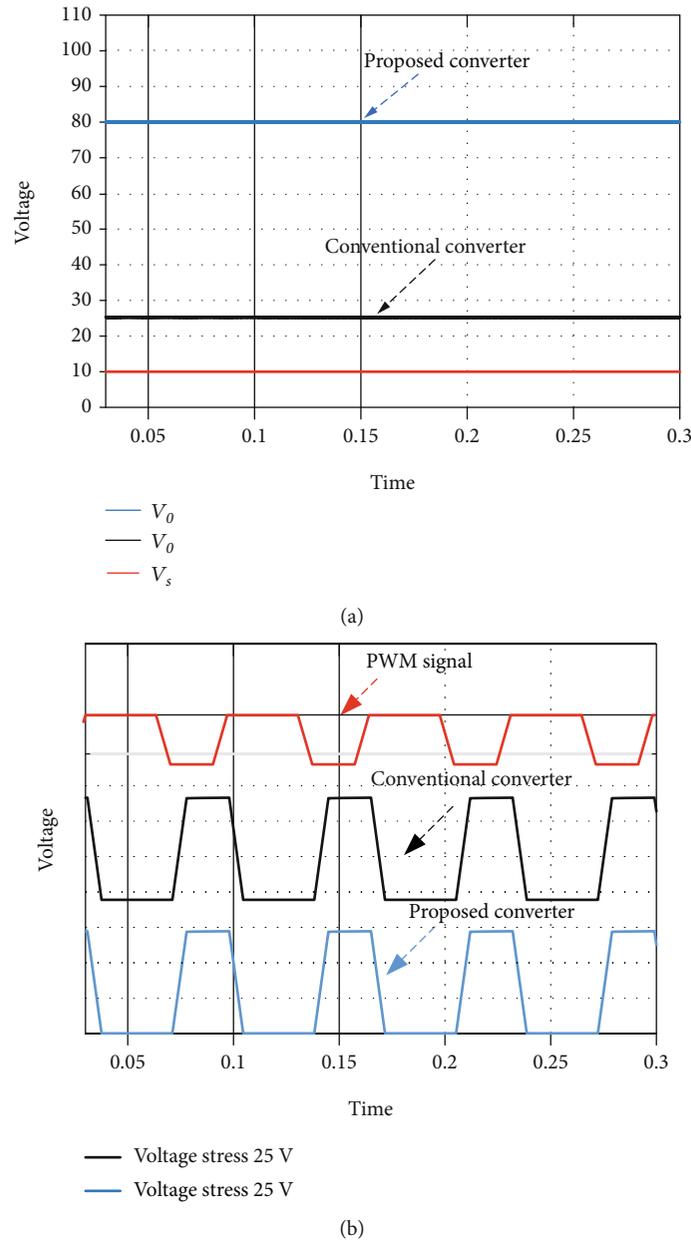


FIGURE 11: Proposed converter simulation results.

shown. Figure 11(a) shows the simulation results of both the conventional boost converter and proposed CPC converter, where input voltage given to both the converters is the same 10 V, and it can be seen that the output voltage of the proposed converter is higher as compared to conventional converter, which is 80 V as compared to 25 V output voltage of conventional boost converter, which is very low. In Figure 11(b), we can see that the voltage stress of the traditional boost converter is the same as output voltage, as mentioned in Eq. (2). Still, the voltage stress of the recommended converter CPC topology is very less. From simulation results, it is very clear that the presented converter contains many pros as compared to conventional converter, such as high voltage gains and lower semiconductor switching stress, as shown in Figure 11(b). In traditional boost converter, if we

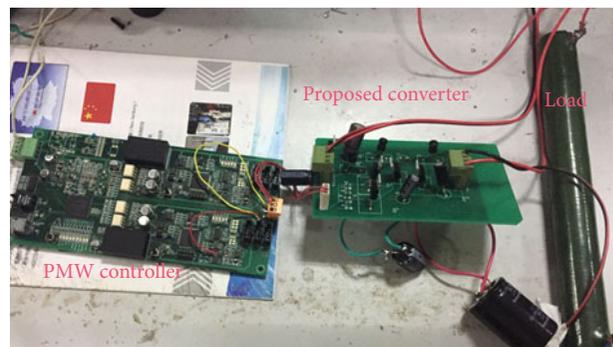


FIGURE 12: Experimental prototype of presented converter.

TABLE 2: Component type and cost.

Components	Symbol	Component type	Cost (\$)	Model number
Inductors ($L_{1,2,3}$)	L	Passive	0.15/piece	
Capacitor ($C_{1,2,3,4}$)	C	Passive	\$0.20-\$1/piece	
Resistor	R	Passive	\$14-\$20/piece	
MOSFET ($S_{1,2}$)	S	Active	\$0.22-\$0.24/piece	IRFZ46N
Diodes ($D_{1,2,3}$)	D	Active	\$0.21-\$0.24/piece	MUR860

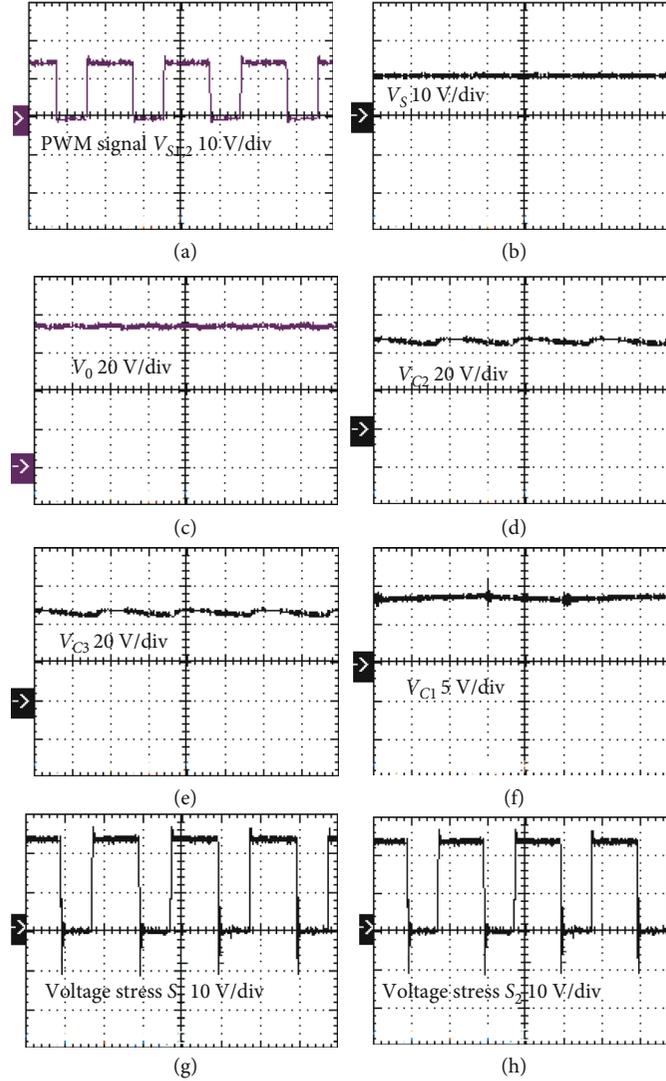


FIGURE 13: Proposed converter experimental results.

give 10 V as an input voltage to achieve the output voltage according to proposed topology from the conventional boost converter, it shall be operated at higher of duty ratio, which will result in increasing the component losses connected with the circuit and will degrade the overall system efficiency. The higher duty cycle could cause failure or malfunctioning of the switches because of the short conduction time.

6.2. Experimental Results and Discussion. To validate the operation principle and investigate the efficacy of the recom-

mended CPC converter topology, a lab-scale prototype was developed with the circuit parameters: $V_S = 10$ V; $V_0 = 80$ V; switching frequency = 100 kHz; $L_1, L_2,$ and $L_3 = 220$ μ H; load = 200 Ω ; $C_1, C_2, C_3,$ and $C_0 = 440$ μ F, 840 μ F, 840 μ F, and 420 μ F, respectively, as shown in Figure 12, and proposed converter component types and cost are presented in Table 2. The experimental results of the recommended CPC converter are depicted in Figure 13, where the duty cycle of the suggested CPC topology is set at $D = 0.6$, and it works in CCM mode. Figure 13(a) depicted switching signals

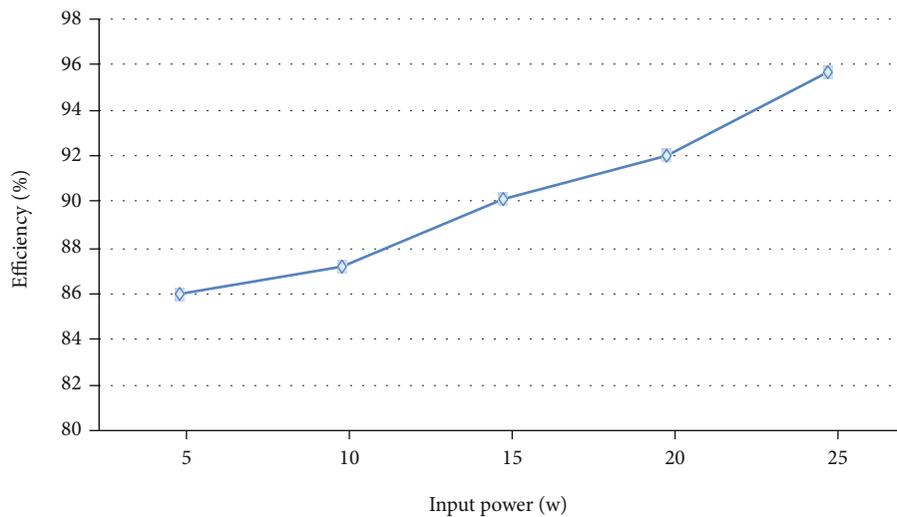


FIGURE 14: Efficiency graph.

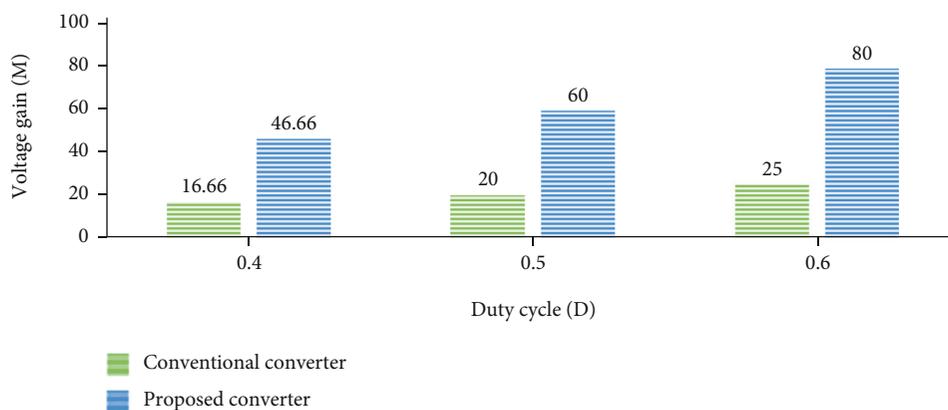


FIGURE 15: Voltage gain graph.

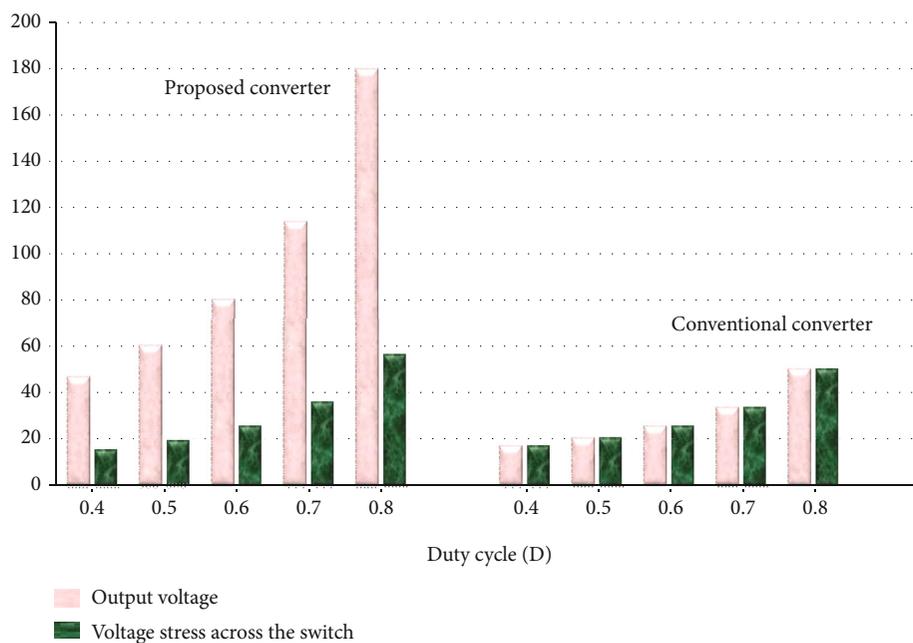


FIGURE 16: Switching stress graph.

of the anticipated converter, and Figure 13(b) depicted input voltage V_s . Figure 13(c) depicted where we can observe that the output voltage V_0 presented converter is around 78 V, which is very close to the voltage gain equation of the recommended converter. From output voltage, it is vibrant that the recommended converter CPC topology has achieved high voltage gain without higher duty ratio.

Figures 13(d) and 13(e) show the waveform of capacitor voltage V_{C2} and V_{C3} which is 49 V, respectively, which are also very close to the capacitors of Eqs. (40), (41). Figure 13(f) depicted voltage across the capacitor V_{C1} which is 10 V, which is equal to the input voltage. Furthermore, Figures 13(g) and 13(h) depicted voltage stress across the MOSFET switches S_1 and S_2 which are 25 V of each. So, it is testified that the recommended CPC converter topology can get high voltage gain at the load side with monomer switching stress.

The proposed converter efficiency vs. the traditional boost converter were observed at different load at input and output terminals in which input voltage and current and output voltage current were measured with a tool, and supported handling data by following the Eq. (53) were performed in Matlab Simulink.

$$\eta = \frac{V_0 * I_0}{V_{in} * I_{in}}. \quad (53)$$

The proposed converter efficiency graph is portrayed in Figure 14, and it can be observed that the maximum efficiency achieved by the proposed CPC topology is 95.68% at 25 W input power and 85.98% minimum efficiency at 5 W input. Thus, it is clear that the recommended CPC topology has shown an excellent efficiency with high voltage gain. Figure 15 shows the output voltages at altered duty cycles, where it can be simply observed that at any duty cycle, recommended converter achieved high voltage at the output in response to the conventional converter. Furthermore, in Figure 16, the switching stress and output voltage across the MOSFETs of recommended CPC converter and traditional boost converter are illustrated, where we can witness that at 0.4, 0.5, and 0.6 duty ratio levels, voltage gain of the proposed converter is very high and switching stress is low as compared to traditional boost converter, and the voltage gain is equal to voltage stress across the MOSFET switch.

7. Conclusions

Renewable energy systems are needed in order to meet the increasing demand of the global energy consumption, and power electronic converters are an important module in such systems. This paper presents new DC-DC boost converters based on the charge pump capacitor (CPC). The feature combination of CPC-DCBC with voltage multiplier cell attains high output voltage gain with lesser switching stress. After simulation and experimental results, it is evidenced that the CPC-DCBC proposed topology could achieve high output voltage without working at an extremely duty cycle with excellent efficiency. The presented converter topology is applicable where a grid supply is unavailable and the source

appliances generally run at high current with low input voltage, whereas their output load requirement is low current with high output voltage. for example, remote telecommunication system, off-grid solar system, and defense communication system. It also has the following advantages over traditional DC-DC boost converter:

- (i) It operates at a lower duty cycle, which reduces the losses linked with the components installed in circuit and improves its efficiency
- (ii) Less number of components, which reduce the risk of malfunctioning across the components and can, therefore, achieve higher voltage gain with very less voltage stress
- (iii) Fewer switch utilization because of low voltage stress across them, which tends to reduce the active switch cost
- (iv) Smaller inductor size because of less energy volume, which reduces the cost and size of the converter

Data Availability

The raw data used for this proposed work have been cited in the manuscript. Moreover, the derived data supporting the findings of this study have been graphically depicted and are available with the corresponding author on request.

Conflicts of Interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

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