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Research Article

Design of a High Step-Up DC-DC Converter with Voltage Doubler and Tripler Circuits for Photovoltaic Systems

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In this paper, a high step-up DC-DC interleaved boost converter is proposed for renewable sources with low voltages such as photovoltaic module and fuel cell. The proposed converter uses interleaving method with an additional voltage doubler and tripler circuit. In the proposed converter, the inductor at all phases is operated to gain high voltage through voltage doubler and tripler circuit capacitors with suitable duty cycle. The proposed topology operates in six switching states in one period. The steady-state analysis and operating principle are examined comprehensively which shows numerous improvements over the traditional boost converter. These improvements are high-voltage gain and low-voltage stress across switches. The proposed DC-DC interleaved boost converter has a gain/conversion ratio four times that of the conventional interleaved boost converter and four times less-voltage stress across the main switches. Simulation has been done in Matlab Simulink on a 70% duty cycle, and results are compared with conventional interleaved boost converter. For an input voltage of 15 volts, the proposed converter is able to generate an output voltage of 200 volts at 70% duty cycle with a voltage stress of 50 volts across main switches, whereas traditional interleaved boost converter generates 200 volts from same input voltage at 92.5% duty cycle with voltage stress of 200 volts across switches. From simulation results, it is clear that the proposed converter has better performance as compared to conventional interleaved boost converter for same design parameters.

1. Introduction

Renewable energy generation becomes more popular during the last decade. Renewable energy sources, for example, solar, wind, and fuel cell systems, are most effective sources to reduce the power generation crisis all over the world [1]. Energy resources, for example, coal, natural gas, and oil, have various bad influences on nature, such as pollution and greenhouse impacts; also, there is a massive contradiction among the global energy need and the fossil fuel supply. The key matters for human being development are lack of energy and environmental pollution. Renewable sources such as photovoltaic modules are a clean energy source, and their addition to the power system is constantly rising. It will contribute a huge amount of electricity among all the renewable energy sources [2, 3]. The PV grid-connected power system turns into a fast emergent section in the PV market [4]. Power electronics circuits must be followed for using energy sources (wind cells, solar, and fuel) as a front end of the electrical system [5]. Bidirectional DC-DC converters are also needed in the energy storage systems (ESSs), to store the excess energy during production and release it when needed in peak demand or off peak hours; hence, boost converter is required to step up low voltage of storage system [6]. The full utilization of power is generated through PV module, and to satisfy safety requirements, the latest research trend is to

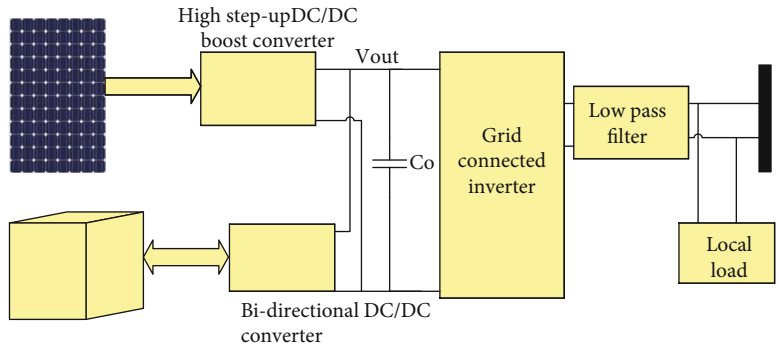

Figure 1: Drawing of the single-phase PV grid-connected power system.

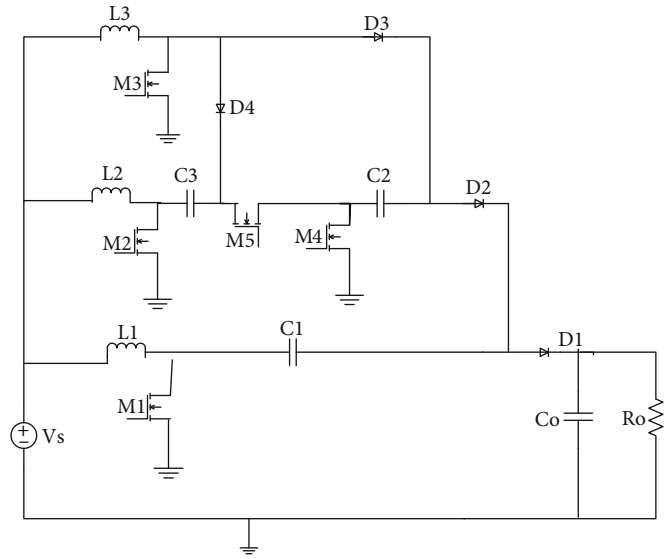

Figure 2: Circuit diagram of the proposed converter.

make parallel arrangement of PV module instead of series. A high DC bus voltage is required for the half-bridge, full-bridge, and multilevel grid inverters. The power in series configuration drops off significantly due to partial shading, particularly in the urban regions and mismatch of modules [7]. In this case, the PV parallel arrangement is more effective than the PV series-connected arrangement due to the functioning of PV modules [8, 9]. H-bridge multilevel inverters or other multilevel configurations are employed to enhance the PV modules output power in grid-connected PV power system [10, 11], but for this, some other power devices are needed, and the cost is increased in these solutions. Renewable sources mostly generate electrical power with small DC voltage. Hence, the electrical power has been produced with low DC voltage, and we know that 1.414 times of AC voltage is needed on the DC side to convert it into the desirable AC voltage. The complete model is shown in Figure 1.

Therefore, DC/DC high step-up converters are required. The conventional boost converters can attain a high gain on a high duty cycle, which causes a reverse recovery problem and high-voltage stress across the switching devices, which decreases the efficiency [12]. A triangle modulation (TRM) scheme decreased circulating current with ZCS behavior for the whole operating range; however, the feasibility of TRM is limited for the operation to gain more than unity [13]. To minimize these issues, it is desirable to plan a DC-DC step-up converter that can attain a high-voltage gain exclusive of high duty cycle, less reverse recovery problem, and improved efficiency with low-voltage stress across the main transistors. Theoretically, boost converter can attain infinite gain, but because of various parasitic in experimental layout, the infinite gain cannot achieve practically. Therefore, to overcome the limitation of such type on gain, different types of solutions have been introduced in the literature. In recent years, switched capacitor voltage boost converter has got more attention because of its exceptional full monolithic integration applications and higher power density as compared with conventional inductor-based voltage boost converters. The multistage switched-capacitor voltage boost converter characteristics can be investigated with no involvement of magnetic components [14, 15]. This particular property allows it to be used in analytical models and estimate the performance of voltage boost converter [16, 17]. Moreover, conventional models by using simple

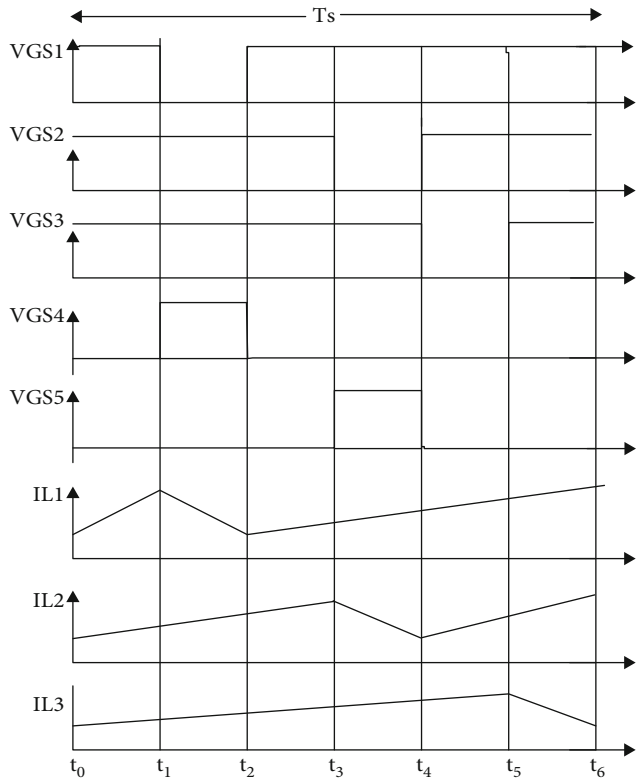

Figure 3: Major waveforms of the proposed converter.

switched-capacitor voltage boost converters have been reviewed in [18]; a small number of reports on a model using the modified switched-capacitor voltage boost converters can be discovered. Furthermore, even though the usual models practice a switching frequency FS and flying capacitance CF to design voltage boost converter, load capacitance CL and complementary switched-capacitor configuration are not taken into account. Hence, the accuracy of the model is not enough and cannot be used in real voltage boost converters. A switched-capacitor voltage boost converter has been used in the power range from monolithic integration to higher power application [19, 20]. Several voltage boost converters have been proposed. Boost converters with switched capacitor are broadly used since they can achieve high-voltage gain by linking voltage boost converters in a cascade [21]. It can generate a high gain, but the overall system efficiency will be reduced because the resultant efficiency will be the product of the efficiencies of the linked converters. Theoretically coupled inductor-based converter increased DC gain, by increasing the turns ratio of the coupled inductor, though the leakage inductance drawback should be thoroughly controlled [22]. Hence, a new interleaved boost converter with voltage doubler and tripler circuit is proposed here which gives improved results in terms of gain and voltage stress across the switching devices on small duty cycle. The circuit diagram of the mentioned topology is presented in Figure 2.

The mentioned topology is a three-phase interleaved circuit which consists of three inductors, voltage doubler and tripler circuits and a basic boost converter circuit. Switching devices M_1, M_2, M_3, M_4, and M_5 are turned on and off by a PWM source with a 120-degree phase shift for switch M_1, M_2, and M_3, while the switch M_4 will be on when the switch M_1 is off and vice versa. The same is the case for switches M_5 and M_2, such as both the switches will not be on or off at the same time. The inductors will charge in the on time of the switch M_1, M_2, and M_3 and will discharge to the capacitors when the switch M_1, M_2, and M_3 are in off state. With the proposed topology, the voltage gain will increase, and voltage stress across the switches, such as voltage drop, will reduce; hence, the losses will decrease.

2. Operating Principle of Proposed Converter

A three-phase interleaved boost converter with voltage doubler and tripler circuit is proposed in this paper. The below-mentioned assumptions were made for the operation of the mentioned converter.

(1) Capacitor C_1, C_2, C_3, and Co are of enough size that the voltage ripple is minor through them compared to their DC values

(2) Each component is considered to be ideal

(3) The operating mode is continuous conduction mode; thus, the current I_1 through inductor L_1, I_2 through inductor L_2, and I_3 through inductor L_3 flow continuously

(4) Inductors L_1, L_2, and L_3 have the same inductance L

All switches are operated by PWM signals. Signals for switchs M_1, M_2, and M_3 are having a phase shift of 120 degrees. The PWM signal for switch M_4 is the inverse of switch M_3, and the signal to switch M_5 is the inverse signal of the switch. V_S is the input voltage, and V_O is the output voltage. The proposed is converter operating with constant switching constant frequency F_S, where $T_S = 1/F_S$. For the proposed converter, there are six switching states such as modes in one complete switching period as shown in Figure 3 and a few major waveforms defining the operating behavior of the mentioned converter. The six switching states are $t_o = 0$ sec, $t_1 = (\mathrm{DTs} - 2\mathrm{Ts}/3)$ sec, $t_2 = (\mathrm{Ts}/3)$ sec, $t_3 = (\mathrm{DTs} - \mathrm{Ts}/3)$ sec,$t_4 = (2\mathrm{Ts}/3)$ sec, $t_5 = \mathrm{DTs}$ sec, and $t_6 = (Ts)$ sec

All the six switching states are described as follows:

(i) State: I, III, V:$(T_0 \le T \le T_1), (T_2 \le T \le T_3, T_4 \le T \le T_5)$

States I, III, and V are the same for the proposed converter. It begins when switches M_1, M_2, and M_3 are set high at starting of time with PWM signals to V_{GS1}, V_{GS2}, and V_{GS3}. Diodes D_1, D_2, D_3, and D_4 are off in these states. The circuit diagram for this state is shown in Figure 4. Inductors L_1, L_2, and L_3 are get charged by DC input voltage, and I_1, I_2, and I_3 through inductors L_1, L_2, and L_3 rise linearly with slopes $VS/L1$, $VS/L2$, and $VS/L3$, respectively. The capacitors C_1, C_2, and C_3 are neither charges nor discharges. In this state, the output capacitor C_O discharges to load, and

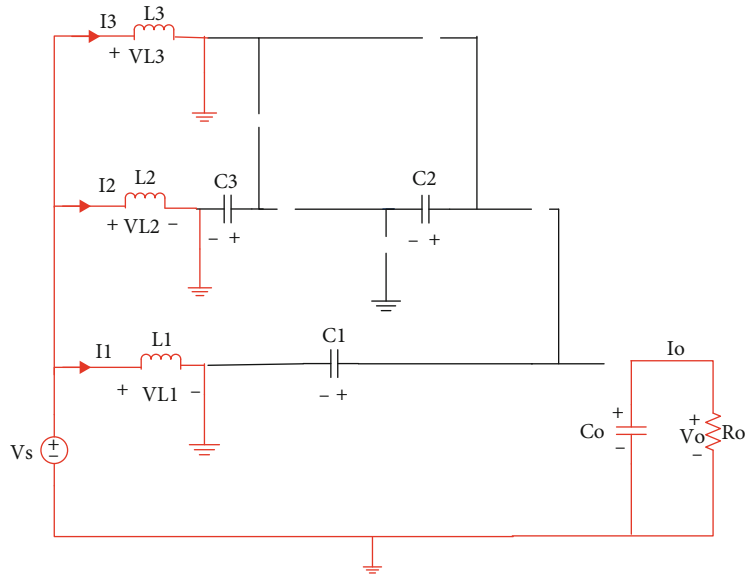

Figure 4: States I, III, and V.

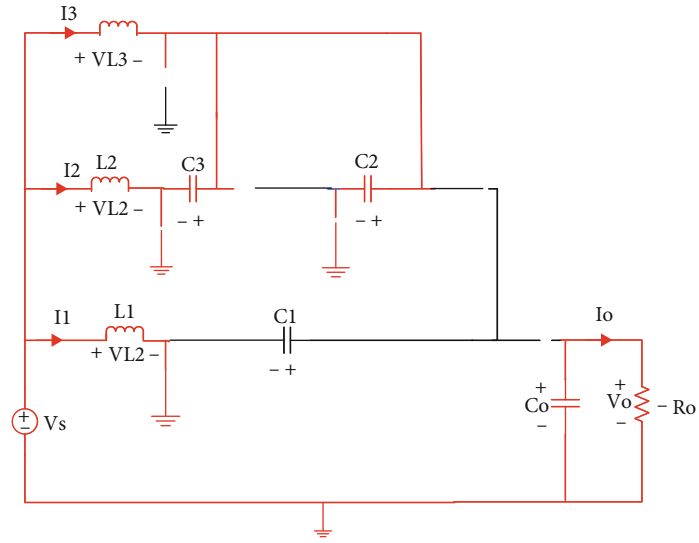

Figure 5: State II.

hence, output voltage Vo through Co decrease linearly with slope of $-VO/(RL * CO)$.

(ii) State: II $(T_1 \le T \le T_2)$

This circuit diagram for this state is shown in Figure 5. The inductor L_1 discharge in this state to capacitors C_2 and C_3, while L_2 and L_3 are still charging, and I_2 and I_3 through inductors L_2 and L_3 constantly rise with a slope of $VS/L2$ and $VS/L3$, respectively. So, in this state, the voltage across capacitors C_2 and C_3 increases because the capacitor is charging. Voltage across capacitor C_1 is still constant because current is not flowing through capacitor C_1. In this state, the output capacitors C_O discharge to load resistance, and hence, the voltage V_O at output across C_O falls linearly with a slope of $-VO/(RL * CO)$.

(iii) State: IV $(T_3 \le T \le T_4)$

The circuit diagram for this state is presented in Figure 6. Inductor L_1 is charging, and I_1 and I_3 through inductors L_1 and L_3 increase linearly with a slope of $VS/L1$ and $VS/L3$, correspondingly, inductor L_2 and capacitors C_2 and C_3 are discharging to capacitor C_1.So, in this state, the voltage across capacitors C_2 and C_3 decreases, and voltage across capacitor C_1 increases. In this state, the output capacitor C_O discharges to load; hence, the voltage at the output V_O through C_O decreases linearly with a slope of $-VO/(RL * Co)$.

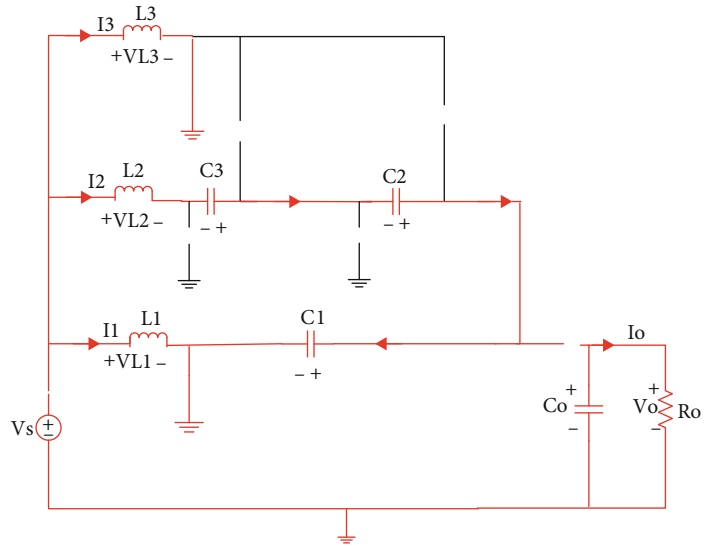

Figure 6: State IV.

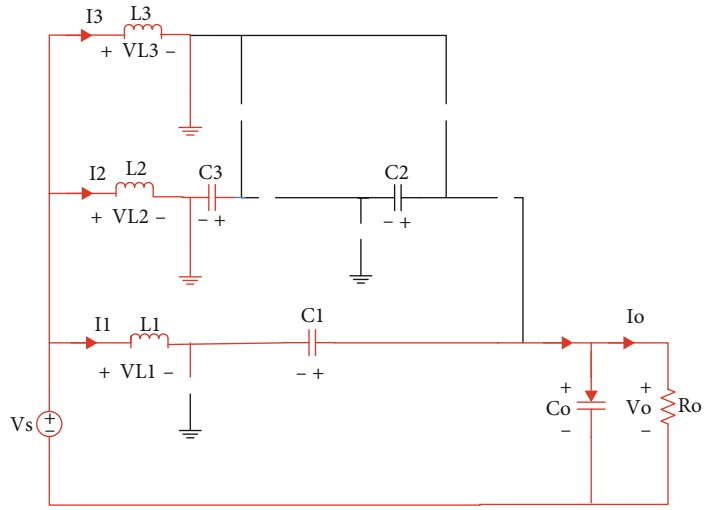

Figure 7: State VI.

Table 1: Converter parameters for simulation.

Name of parameter	Symbol	Value
Voltage at input	V_S	15 [V]
Voltage at output	V_O	200 [V]
Frequency	F_S	10 [kHz]
Load resistance	R_L	1537 [Ω]
Filter inductor in phase #1, 2, and 3	L_1, L_2, L_3	1 [mH]
Intermediate capacitor	C_1	1.75 [uF]
Intermediate capacitor	C_2	5.2 [uF]
Intermediate capacitor	C_3	5.2 [uF]
Output smoothing capacitor	C_O	5 [uF]
Voltage stress across M_1, M_2, M_3	$V_{M1,M2,M3}$ (stress)	50 {V]
Ripple in capacitor voltage V_{CO}	ΔV_{CO}	10 [V]

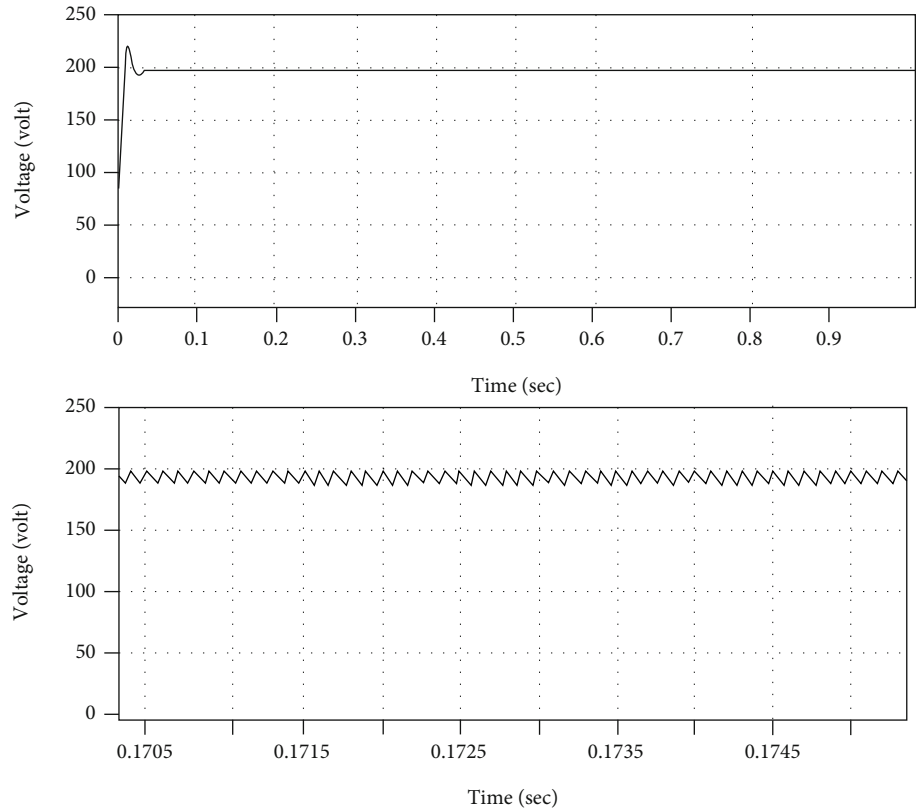

Figure 8: Output voltage waveform on 70% duty cycle.

(iv) State: VI $(T_5 \le T \le T_6)$

The circuit diagram for this interval is presented in Figure 7. Inductors L_2 and L_3 are charging while L_1 is discharging. I_2 and I_3 rise linearly with a slope of $VS/L2$ and $Vs/L3$ correspondingly, and inductor L_1 and capacitor C_1 are discharging to capacitor Co and load Ro. The voltage across capacitor C_1 is decreasing and the output capacitor Co gets charging, and hence, the voltage at output such as V_O across Co increases linearly.

3. Steady-State Analysis

To make an easy and simple assessment of the proposed circuit diagram, the time intervals for switching states put across in terms of switching period TS of duty cycle D as follows: $t_o = 0$ sec, $t_1 = (\mathrm{DTs} - 2\mathrm{Ts}/3)$ sec, $t_2 = (\mathrm{Ts}/3)$ sec, $t_3 = (\mathrm{DTs} - \mathrm{Ts}/3)$ sec, $t_4 = (2\mathrm{Ts}/3)$ sec, $t_5 = \mathrm{DTs}$ sec, and $t_6 = (\mathrm{Ts})$ sec.

3.1. DC Conversion Ratio. Voltage gain can be derived by using volt-second balance principles. Inductor L_3 is charging in states I, III, IV, V, and VI and discharging in state II.

The volt second balance of inductor L_2 gives:

$$\mathrm{VC2} = \frac{\mathrm{VS}}{1-D}, \qquad \mathrm{VC3} = \frac{\mathrm{VS}}{1-D}. \tag{1}$$

Similarly, inductor L_2 is charging during the interval I, II, III, V, and VI and discharging in IV.

The volt second balance of inductor L_2 gives:

$$\mathrm{VC1} = \frac{3\mathrm{VS}}{1-D}. \tag{2}$$

Inductor L_1 gets charged during states I, II, III, IV, and V and discharged during interval VI.

The volt second balance of inductor L_2 gives:

$$\frac{\mathrm{Vo}}{\mathrm{Vs}} = \frac{4}{1-D}. \tag{3}$$

The gain of the proposed converter is obtained as:

$$\mathrm{M} = \frac{4}{1-D}. \tag{4}$$

3.2. Voltage Stress across MOSFETS M_1, M_2, and M_3. When the switch is in an off state, the voltage stress or voltage drop is produced across it. The voltage stress across the MOSFET M_1 can be obtained as

$$\mathrm{VM1} = \mathrm{VCo} - \mathrm{VC1}. \tag{5}$$

The voltage stress through switch M_2 can be obtained as

$$\mathrm{VM2} = \mathrm{VC1} - \mathrm{VC3} - \mathrm{VC2}. \tag{6}$$

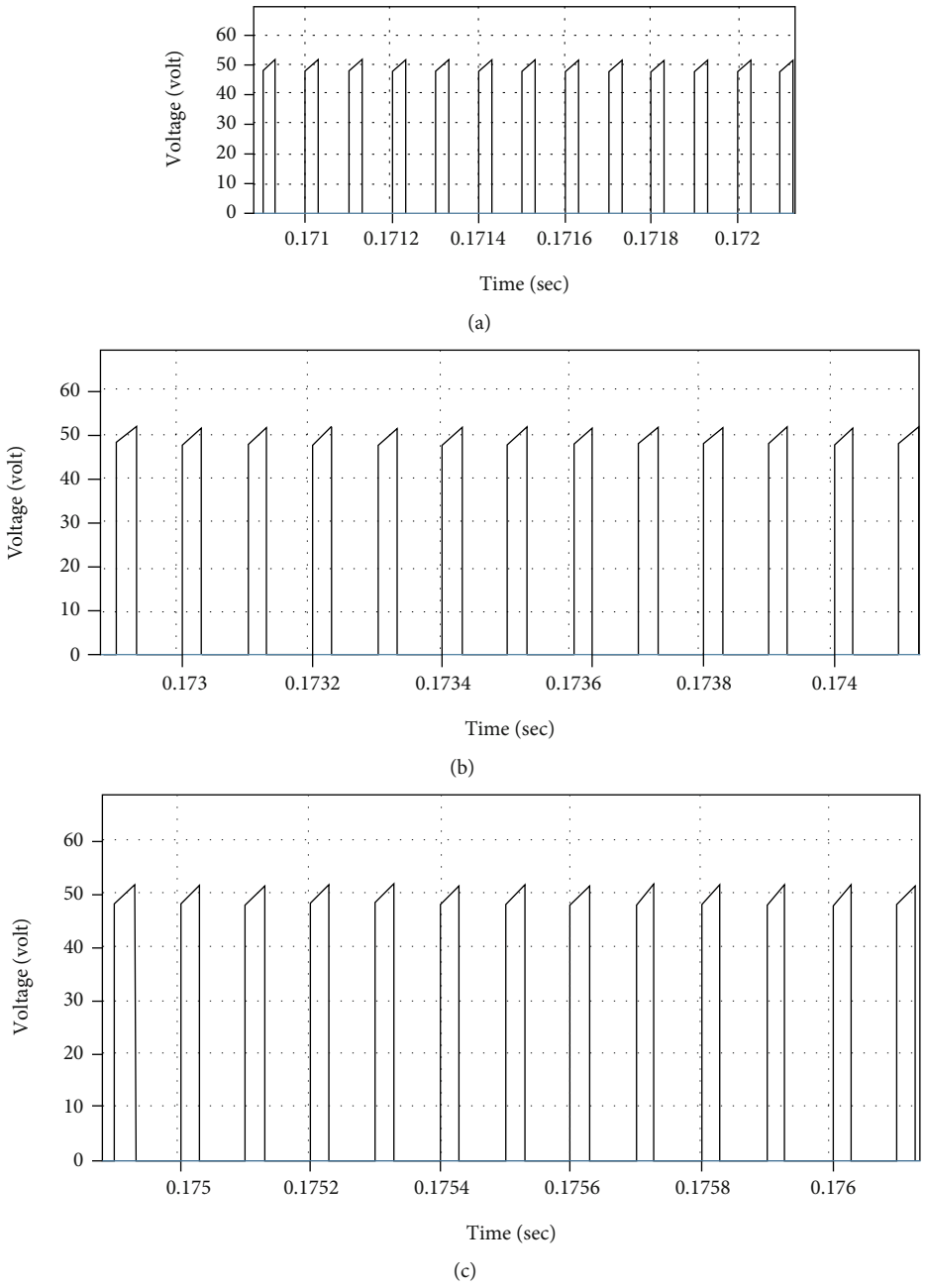

FIGURE 9: (a) Voltage stress across M_1. (b) Voltage stress across M_2. (c) Voltage stress across M_3.

The voltage stress across the switch M_3 can be obtained as

$$\mathrm{VM3} = \mathrm{VC2} = \mathrm{VC3}. \tag{7}$$

3.3. Ripple Current and Ripple Voltage. The $\Delta i1$ is the ripple current in current I_1, $\Delta i2$ in current I_2, and $\Delta i3$ in current I_3. The ripple current through inductors L_1, L_2, and L_3 can be expressed as follows:

$$\Delta I1, 2, 3 = \frac{\mathrm{VsDT}}{\mathrm{L}(1, 2, 3)}. \tag{8}$$

The ΔVco is the ripple voltage in V_{CO}, ΔVc1 in V_{C1}, ΔVc2 in V_{C2}, ΔVc3 in V_{C3}, and ΔVc4 in V_{C4}.

For finding ΔVco, the capacitor CO is discharging to the load. The ΔVco can be expressed as follows:

$$\Delta\mathrm{Vco} = \frac{\mathrm{Vo} * D}{\mathrm{Ro} * \mathrm{Co} * \mathrm{Fs}}. \tag{9}$$

For ΔVc1, capacitor C_1 is discharging to Co and load; ΔVc1 can be expressed as follows:

$$\Delta\mathrm{Vc1} = \frac{I1 * (1 - D)}{\mathrm{C3} * \mathrm{Fs}}. \tag{10}$$

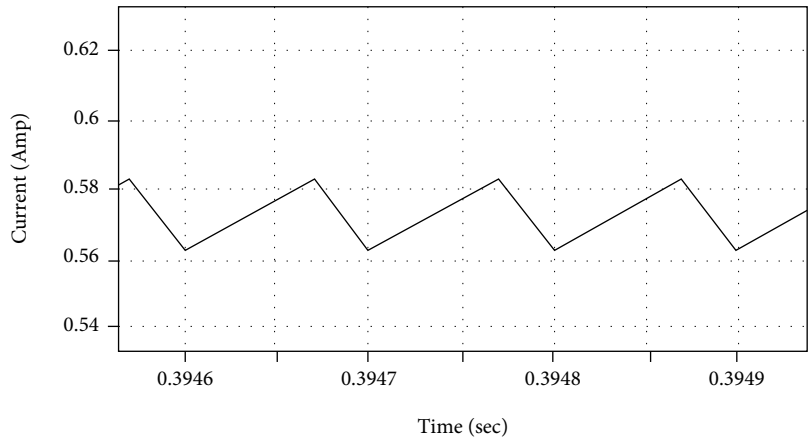

Figure 10: Phase current across L_1, L_2, and L_3.

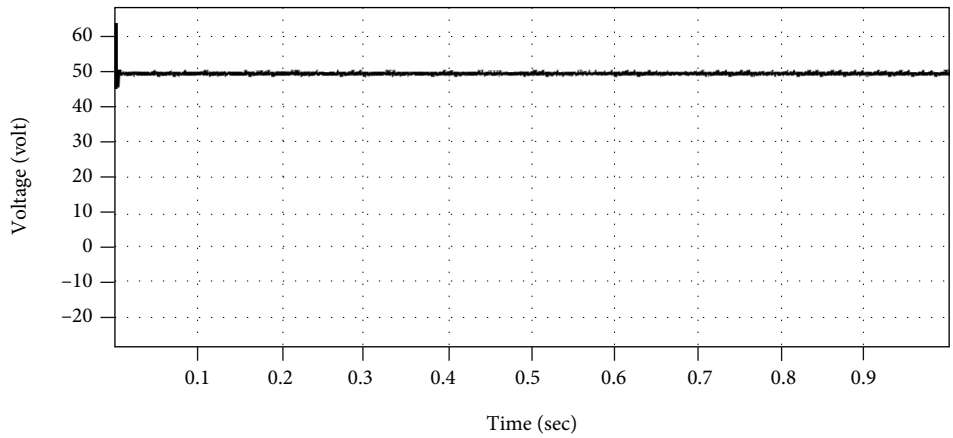

Figure 11: Output voltage waveform of conventional IBC on $D = 0.7$.

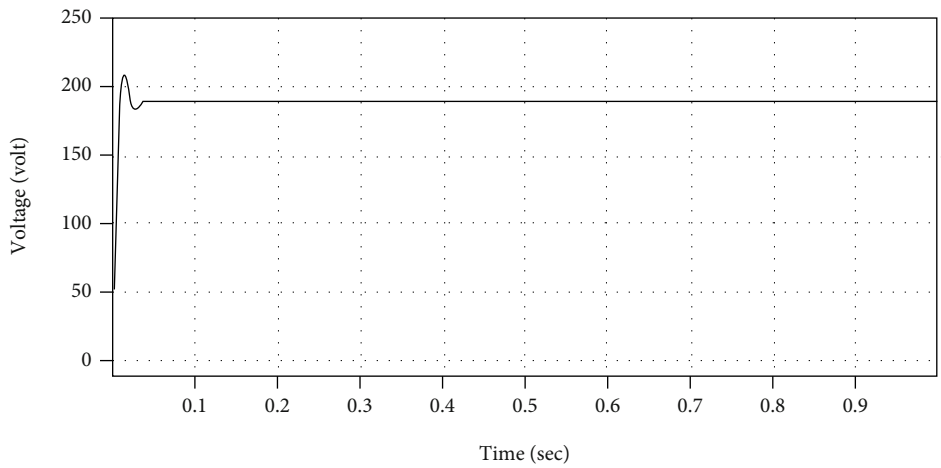

Figure 12: Output voltage waveform of conventional IBC on $D = 0.925$.

Here, $I1$ can be expressed as follows:

$$I1 = \frac{Io}{1 - D}. \tag{11}$$

For finding ΔVc2, capacitor C_2 is discharging to C_1; ΔVc2 can be expressed as follows:

$$\Delta Vc2 = \frac{I1 * 1 - D}{C2 * Fs}. \tag{12}$$

For finding ΔVc3, capacitor C_3 is discharging to C_1; Δ

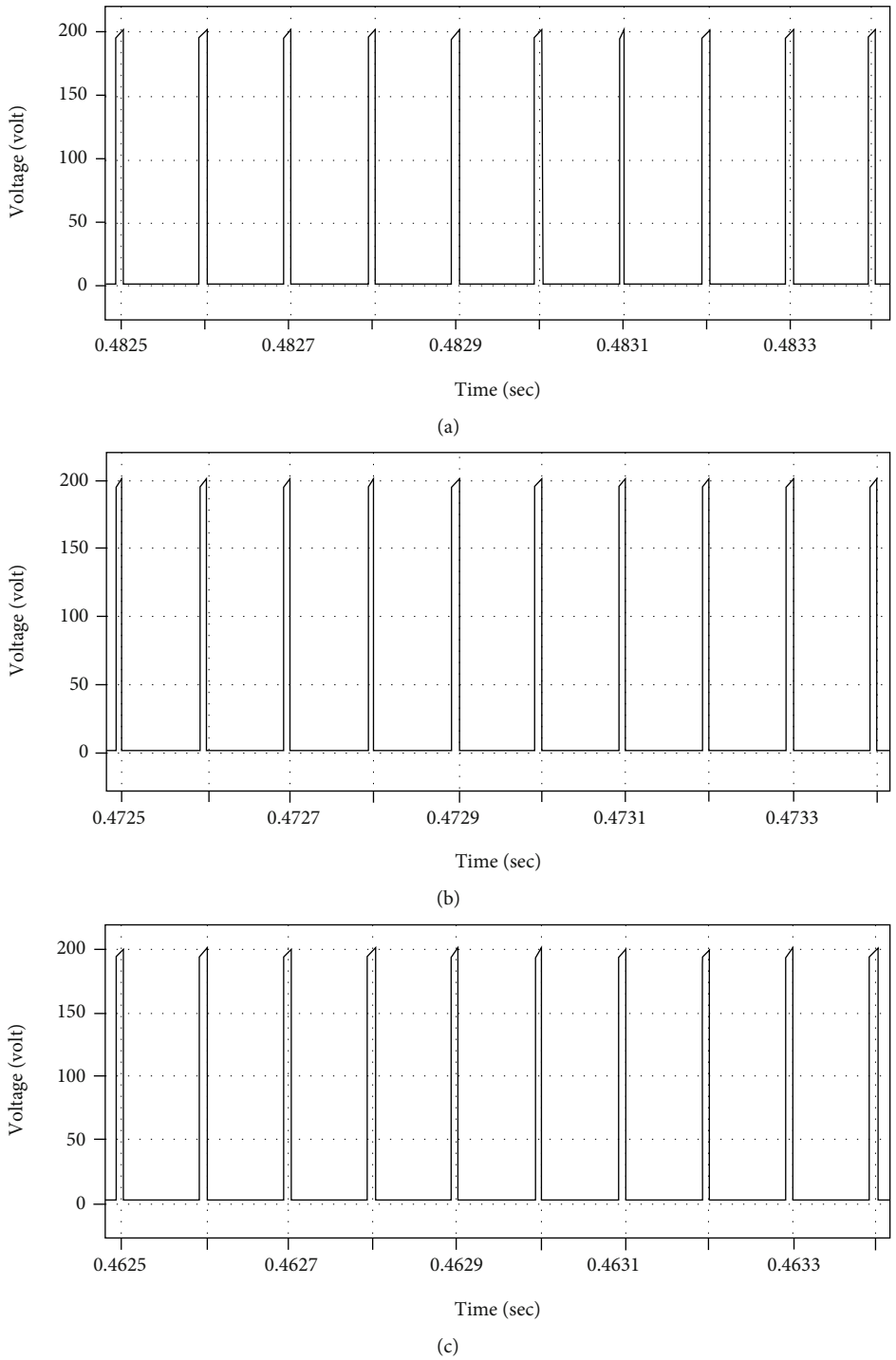

Figure 13: (a) Voltage stress across MOSFET M_1. (b) Voltage stress across MOSFET M_2. (c) Voltage stress across MOSFET M_3.

Vc2 can be expressed as follows:

$$\Delta \mathrm{Vc3} = \frac{I1 * 1 - D}{\mathrm{C3} * \mathrm{Fs}}. \tag{13}$$

3.4. Voltage Stress across the Switches. Voltage stress across the MOSFET M_1 can be expressed as follows:

$$\mathrm{VM1} = \mathrm{VCo} - \mathrm{VC1}. \tag{14}$$

Voltage stress across the MOSFET M_2 can be expressed as follows:

$$\mathrm{VM2} = \mathrm{VC1} - \mathrm{VC3} - \mathrm{VC2}. \tag{15}$$

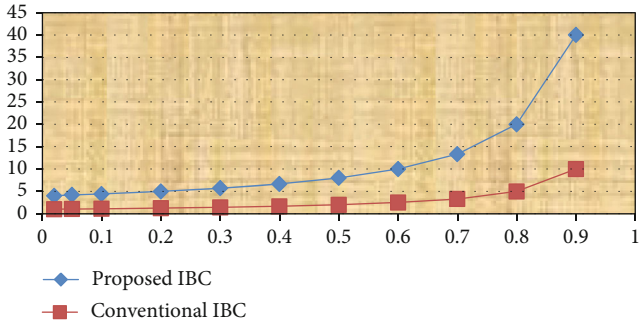

Figure 14: Voltage gain comparison between conventional IBC and proposed IBC.

Voltage stress across the MOSFET M_3 can be expressed as follows:

$$VM3 = VC2 = VC3. \quad (16)$$

4. Results

The simulation has been performed in Matlab Simulink to verify the performance of the proposed interleaved triphase boost converter and conventional DC-DC interleaved boost converter with parameters given in Table 1. The derived mathematical equations have been used up to obtain the theoretical results presented in Table 1.

4.1. Simulation Results. Output voltage waveforms of the proposed boost converter with a 70% duty cycle is 200 V shown in Figure 8

The voltages stress across the MOSFET M_1, M_2, and M_3 is 50 V as shown in Figures 9(a)–9(c); the phase current through inductors L_1, L_2, and L_3 is shown in Figure 10.

The simulation results clearly show that there is no difference between simulation results and theoretical results.

4.2. Comparison. Now, utilizing the parameters given in Table 1, the simulation results of the conventional DC-DC interleaved boost converter are also acquired. The output voltage waveform of the conventional boost converter is given in Figure 11, which is 50 volts with a 70% duty cycle. The conventional interleaved boost converter gives the output voltage 200 volts on a 92.5% duty cycle value such as $D = 0.925$ (as shown in Figure 12). Figures 13(a)–13(c) show that at $D = .925$; the voltage stress across MOSFETS for the usual interleaved DC-DC boost converter is 200 V.

It is clear from the simulation results that the presented converter topology has very good results as compared to the conventional interleaved DC-DC boost converter. As compared with a conventional converter, it is obvious that the proposed boost converter has a four times higher voltage conversion ratio, and the voltage stresses on main switches are approximately four times smaller than the conventional DC-DC interleaved boost converter. In the conventional IBC, the output voltage appears across the main switching devices, while the current is divided into all phases, due to which the inductor size is reduced in both conventional and proposed IBC.

Simulation results are provided for the conventional interleaved DC-DC boost converter and proposed interleaved DC-DC boost converter, which indicates that the proposed converter yields better results as compared with a conventional interleaved boost converter at the expense of only two additional switches (proposed converter uses 5 MOSFETs while conventional uses 3). The comparisons between the gain of the conventional IBC and proposed IBC are shown in Figure 14.

5. Conclusion

Compared with the conventional IBC, the proposed IBC has several good extra characteristics, which comprise a high gain/conversion ratio, and across the main MOSFETs, the low-voltage stress. Voltage doubler plus voltage tripler circuits are used to gain these benefits. The steady-state analysis and working principle of the offered converter of each state are examined clearly with the proposed circuit diagram and mathematical equations. Simulation results in Matlab Simulink show that normal interleaved DC-DC boost converter is affected by operating on extreme value of D (duty cycle) and will be having reverse recovery problem for switching devices for boosting 15-volt input voltage to 200 volts, while it is clear from both the simulation and theoretical outcomes that the presented converter can simply achieve 200 V with the appropriate value of D, and the voltage stress across the switches will also reduce to one-fourth of output voltage. The above-mentioned qualities of high DC-DC conversion ratio and reduced voltage stress across switching devices make the mentioned boost converter an appropriate candidate in case of low voltage renewable sources with low DC output voltages and more other functions where a high step-up conversion ratio is wanted.

Data Availability

Data will be provided on request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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