Research Article

New Control Approach of Multicell Stacked Cell Inverter for Solar Photovoltaic System

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Received 13 February 2022; Revised 6 March 2022; Accepted 23 March 2022; Published 11 April 2022

1. Introduction

The inverter is considered the most important component of an on-grid photovoltaic (PV) system. In recent years, the topology of power converters, system stability, and control of grid-connected PV power plants have all attracted a lot of attention [1, 2]. Existing technologies are insufficient for large-scale photovoltaic facilities. Extensive research has been conducted over the previous two decades to suggest novel inverter topologies [1, 3, 4]. This difficulty is solved by the structure of multilayer inverters, which have three or more layers. By splitting the DC voltage at the inverter input, this form of design allows for voltage stress on the switches to be limited. In an on-grid photovoltaic (PV) system, proper inverter control is required to achieve moderate power loss, low total harmonic distortion (THD), and security and grid reliability [5, 6]. The combination of a multi-level architecture with judicious control of the power switches can also eliminate certain families of harmonic lines and therefore improve the spectral content of the output signals (voltage and current) [1, 2]. The duty cycle modulation (DCM) method discussed in [7] has the particularity of producing fewer harmonics [8]. A DCM is a modulation in which an input signal x is transformed into a switching wave train where the duty cycle and period of the modulated signal vary simultaneously with the control signal [7–11]. A new, simpler, and better DCM was then proposed by Nneme and Mbihi [7]. Another particularity of the DCM is its modulation frequency, which is a function of the amplitude of the modulating signal. The work of [9] presents DCM as an effective tool in modulating transmission signals via high-quality results. However, the work in [10] presents an application of DCM in the control of a single-phase inverter. This control strategy, initiated in 2005 [11] for industrial
instrumentation purposes, has been the subject of further scientific work [12, 13] that has proven its reliability and efficiency. Since a theoretical study based on virtual simulations has already been completed successfully in recent works on a new IDCM topology [14], this scientific paper deals with a new control approach applied to a new five-level three-
phase multicell inverter (5 L–SMC H-bridge) topology based on a controller with a duty cycle. This strategy is called duty cycle space vector modulation (DCSVM). The principle of the DCSVM control is based on the advantages of the DCM control and the classical SVM control. This modulation provides very good performance and generates less current harmonics [5]. However, in practice, determining the sequences necessitates calculating the tangent of the angle

<table>
<thead>
<tr>
<th>Case</th>
<th>K1</th>
<th>K2</th>
<th>K3</th>
<th>K4</th>
<th>K5</th>
<th>K6</th>
<th>K7</th>
<th>K8</th>
<th>K9</th>
<th>K10</th>
<th>K11</th>
<th>K12</th>
<th>K13</th>
<th>K14</th>
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<td>1</td>
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<td>0</td>
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<td>1</td>
<td>0</td>
<td>-V</td>
</tr>
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<td>0</td>
<td>1</td>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>-V/2</td>
</tr>
<tr>
<td>9</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 3: Variants of the three-level inverter (3 L–SMC H-bridge): (a) with three stacked cells and (b) with one stacked cell.

Figure 4: 3 L – SMC H-bridge inverter with three stacked cells.
of the vector, which results in undesired singularities. This makes it easier to think about the duty cycle modulation strategy for generating SVPWM signals. In this paper, the modelling and simulation of a new control strategy, as an alternative to the classical SVPWM, implemented with a duty cycle controller using the MATLAB/Simulink software, to be used for the control of static converters is presented. To test the feasibility of DCSVM controllers, simulations have been carried out, the results obtained agree perfectly with those obtained with a conventional SVPWM controller.

After Introduction, a brief description of the studied inverter topology as well as its modelling is presented in Section 2. Section 3 is devoted to the presentation and analysis of the proposed DCSVM control technique. Section 4 includes simulation results and discussion. Finally, the conclusion is presented in Section 5.

### 2. Description of the Studied Topology

#### 2.1. Proposed Topology

Figure 1(a) shows an SMC converter. This converter structure is an evolution of the serial multicellular converter [15]. It was patented in 2000 in France [16, 17] and 2001 in the world [18]. In Figure 1(b), a modification of the basic NPC (Neutral Point Clamped) topology is presented. This variant of the NPC topology (three-level ANPC) makes it possible to push back certain limitations of the basic structure, such as the inequality of the reverse voltages supported by the diodes [19].

The basic cell of a multicellular converter can be made up of 4, 6, or 8 switches. The outer branches are made up of two 3-segment switches. The switches must be connected in series for voltage withstand. The voltage withstand of all the switches is equal to E/2. The middle branch is made up of two switches placed in opposition. For these switches, the maximum voltage withstand is equal to E/2; they do not need to be passed [15]. Figure 2 shows a new five-level three-phase multicell inverter (5 L–SMC H-bridge) topology based on stacked semiconductors and implemented using the PSIM software environment.

This inverter topology is based on the single-phase model of a three-level inverter (3 L – SMC H-bridge), two variants of which are given in Figure 3.

Figure 4 shows a stacked multicell converter and a half H-bridge. The multicell converter consists of two branches of stacked semiconductors (Cell+ and Cell-) connected to the T-Type bridge. However, by using an appropriate control, our converter provides a DC signal and a three-level AC signal (3 L) which can be filtered and fed into the public distribution network [20, 21]. The switches K3, K4, K7, and K8 make it possible to raise the voltage level and prevent the direct voltage source from being short-circuited (directly connected to ground) [22]. Switches K1 and K2 (Cell H), constituting the H-bridge, balance the voltage level at the output of the inverter.

The superimposed cells (Cell+ and Cell-) are the opposition of two semiconductors of the same control so as to form a bidirectional switch on blocking. Putting two switches in opposition does not increase switching losses, because only one of the two switches at the switching frequency, while the other switching only twice per modulation period. Unlike in the case of multicellular converters with floating capacitors (FC), the Cell+ and Cell- cells are not connected to each other by floating capacitors. The distribution of the voltage stress is linked to the state of the switches (on or off) [23]. As for the 2 × 2 SMC, it is possible to double these switches to obtain a structure with switches whose voltage resistance is identical. These will switch at a lower switching frequency (on the order of the modulation frequency). But this increases the number of switches even further: the total number of switches per phase is then 8 semiconductor components. The purpose of this study is, above all, to balance the DC bus. So, for more simplicity in the control, each switch has to hold a tension of V/2, which is considered unique [15].

#### 2.2. Modeling the Converter

To develop a mathematical model of the multicellular converter, consider that

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
<th>Values/units</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC voltage source</td>
<td>( V_{dc} )</td>
<td>100 V</td>
</tr>
<tr>
<td>Internal resistance</td>
<td>( R_{on} )</td>
<td>1.8 m( \Omega )</td>
</tr>
<tr>
<td>Snubber resistance</td>
<td>( R_{s} )</td>
<td>0.9 M( \Omega )</td>
</tr>
<tr>
<td>Snubber capacitance</td>
<td>( C_{s} )</td>
<td>5 ( \mu F )</td>
</tr>
<tr>
<td>Load resistance</td>
<td>( R_{1} = R_{2} = R_{3} )</td>
<td>5 ( \Omega )</td>
</tr>
<tr>
<td>Load inductance</td>
<td>( L_{1} = L_{2} = L_{3} )</td>
<td>3 mH</td>
</tr>
<tr>
<td>Modulation factor</td>
<td>( m )</td>
<td>0.8</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>( f )</td>
<td>50 Hz</td>
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<tr>
<td>Modulation frequency</td>
<td>( M_{f} )</td>
<td>21 kHz</td>
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<tr>
<td>Half-carrier time period</td>
<td>( T_{s} )</td>
<td>0.5 ms</td>
</tr>
</tbody>
</table>

### Table 2: Comparison between the five multilevel inverter structures.

<table>
<thead>
<tr>
<th></th>
<th>NPC</th>
<th>MPC</th>
<th>MNP</th>
<th>SMC</th>
<th>H-bridge</th>
<th>5 L-SMC H-bridge</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of DC voltage sources</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>((n-1)/2)</td>
<td>1</td>
</tr>
<tr>
<td>Number of capacitors</td>
<td>((n-1)(n-2))</td>
<td>(n-1)</td>
<td>(n-1)</td>
<td>(n-1)</td>
<td>(n-1)</td>
<td>0</td>
</tr>
<tr>
<td>Number of switches</td>
<td>(2^{*}(n-1))</td>
<td>(2^{*}(n-1))</td>
<td>(2^{*}(n-1))</td>
<td>(2^{*}(n-1))</td>
<td>(2^{*}(n-1))</td>
<td>(2^{*}(2n+3))</td>
</tr>
<tr>
<td>Number of looping diodes</td>
<td>(2^{*}(n-1))</td>
<td>(2^{*}(n-1))</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

### Table 3: The parameters and simulation conditions.
(i) Semiconductors are perfect

(ii) The switches of the same switching cell operate in a complementary manner

(iii) The supply voltage is continuous

In practice, the upper and lower branches of the structure can contain one or two semiconductors in series. The voltage applied to each switching cell in the off state is constant and is equal to [3, 23]:

\[ V_{\text{Cell}_j} = \frac{V}{p}, \quad (1) \]

with \( j \in \{1, \ldots, p\} \).

In the presence of a single switch, it must withstand a voltage stress twice as high as those of the middle branch. In order to standardize the distribution of the voltage stress, two identical semiconductors can be connected in series or in opposition; their commands being similar [3, 4, 23]. In this assumption, the stress in tension of all the switches of the structure is worth

\[ V_{\text{Int}_j} = \frac{V}{n \times p}, \quad (2) \]

with \( j \in \{1, \ldots, p\} \), where \( n \) and \( p \) represent, respectively, the number of stages and number of cells associated with the converter.
In Figure 4, the upper (Cell+) and lower (Cell-) branches of the structure contain two opposing semiconductors. The voltage applied to each switching cell in the off state is

\[
v_{\text{Cell}_j} = \frac{V}{2},
\]

with \( j \in \{1, 2\} \).

The opposition of switches of the outer branches is necessary for voltage withstand. The voltage withstand of all the different switches is \( V/2 \). Indeed, levels \(-V/2\) and \( V/2\) can be achieved in 2 different ways and level 0 in 3 different ways, as presented in Table 1.

One of the main drawbacks of this structure is the number of components that compose it. The structure of our inverter model can include 8 to 14 switches with different voltage resistances. Indeed, in each basic structure, the switches of the outer branches must hold a voltage \( V \) while those of the inner branch must hold a voltage of \( V/2 \). Doubling the switches increases switching losses, because the two switches switch simultaneously at the switching frequency. The middle branch is made up of two switches placed in opposition. For these switches, the maximum voltage withstand is equal to \( V/2 \); they do not need to be doubled. This converter is used to generate high output voltage levels. This new topology makes it possible to divide the input voltage into several fractions so as to lower the number of switching power semiconductors. Compared to competing topologies in this field of application, the SMC converter has excellent dynamic performance thanks to the multiplication of the chopped voltage frequency and the increase in the number of levels [23–25]. The stacked multicellular structure can be adapted to all configurations: chopper or inverter mounting.

Figure 5 shows some possible combinations of the three-phase five-level multicell inverter (5 L–SMC H-bridge).

The number of output levels is equal to 5 \([-V, -V/2, 0, +V/2, +V]\). In comparison with the 5-level NPC structure, the advantage of this structure is that it has redundancies for certain levels.

Table 2 shows a comparison between the different types of existing inverters with the new 5 L–SMC H-bridge three-phase multicell inverter.

Where \( n \) is the number of stages in the converter. From the above, it appears that the new 5 L–SMC H-bridge structure gives more advantages (absence of looping diodes and capacitors) over its competitors NPC, SMC, and H-bridge. The major drawback to note is the high number of switches used.

Multicellular topologies, on the other hand, use the series connection of switches, thus ensuring the distribution of the voltage stress of the converter over several switching cells. The interlacing or shifting of the controls allows these converters to reveal voltage levels and to multiply the apparent

![Figure 6: Neutral voltages (\(V_{an}, V_{bn},\) and \(V_{cn}\)) and Currents (\(i_a, i_b,\) and \(i_c\)).](image-url)
frequency at the output. These improvements induce a harmonically better quality output voltage spectrum and significantly reduce filtering requirements (volume, stored energy, and cost) [23].

3. New Proposed Command

The DCSVM control principle is based on the advantages of both the DCM control and the traditional SVM control. The implementation of the DCSVM strategy is carried out in the following steps:

Step 1. Determination of reference voltage \( v_d \) and \( v_q \).

The generation of vectors in the Concordia landmark \( (d, q) \) from the three-phase signals \( v_{AN}, v_{BN}, v_{CN} \) is given by the relation (4):

\[
\begin{align*}
  v_d &= \frac{2}{3} \left( v_{AN} - \frac{v_{BN}}{2} - \frac{v_{CN}}{2} \right) \\
  v_q &= \frac{\sqrt{3}}{3} \left( v_{AN} - v_{CN} \right)
\end{align*}
\]  

(4)

\[
\begin{bmatrix}
  v_d \\
  v_q
\end{bmatrix} = \frac{1}{3} \begin{bmatrix}
  2 & -1 & -1 \\
  0 & \sqrt{3} & -\sqrt{3}
\end{bmatrix} \begin{bmatrix}
  v_{AN} \\
  v_{BN} \\
  v_{CN}
\end{bmatrix}.
\]  

(5)

Step 2. Cartesian to polar transformation.

The system of equations given in Eq. (6) transforms corresponding elements of the two-dimensional Cartesian coordinate arrays \( d \) and \( q \) into polar coordinates \( (\rho, \theta) \).

\[
\begin{align*}
  \rho &= \sqrt{v_d^2 + v_q^2} \\
  \theta &= \tan^{-1} \left( \frac{v_q}{v_d} \right)
\end{align*}
\]  

(6)

Step 3. Generation of control signals and intermediate times.

The Simulink model is used to determine the control signals for switches \( T_{ag}, T_{bg}, \text{ and } T_{cg} \) and the intermediate times \( T_r, T_p, \text{ and } T_o \).

Furthermore, assuming that the reference voltage vector \( V_{ref} \) is synthesized from the two basic vectors, the operating
The time of two basic vectors can be calculated according to the volt-second equilibrium principle [26].

\[
\begin{align*}
T_1 &= \sqrt{3} \left( \frac{V_{\text{ref}}}{V_{\text{dc}}} \right) \sin \left( \theta - \frac{(k-1)\pi}{3} \right), \\
T_2 &= \sqrt{3} \left( \frac{V_{\text{ref}}}{V_{\text{dc}}} \right) \sin \left( \frac{k\pi}{3} - \theta \right), \\
T_0 &= T_S - T_1 - T_2,
\end{align*}
\]

(7)

where \(T_1\) and \(T_2\) are the times allocated to vectors \(\overrightarrow{V}_7\) and \(\overrightarrow{V}_8\), \(T_0\) is the time shared between the two null vectors \(\overrightarrow{V}_7\) and \(\overrightarrow{V}_8\), and \(T_S\) is the half-carrier time period.

After determining the times \(T_1\), \(T_2\), and \(T_0\), the time of the closing all keys to the rack at work is determined. In each sector, the switching time of each key is different and is expressed in (8):

\[
\begin{align*}
\text{For } \theta &\in \left[0, \frac{\pi}{3}\right] ; S = 1, \\
\text{For } \theta &\in \left[\frac{\pi}{3}, \frac{2\pi}{3}\right] ; S = 2, \\
\text{For } \theta &\in \left[\frac{2\pi}{3}, \pi\right] ; S = 3, \\
\text{For } \theta &\in \left[\pi, \frac{4\pi}{3}\right] ; S = 4, \\
\text{For } \theta &\in \left[\frac{4\pi}{3}, \frac{5\pi}{3}\right] ; S = 5, \\
\text{For } \theta &\in \left[\frac{5\pi}{3}, 2\pi\right] ; S = 6.
\end{align*}
\]

(8)

Step 4. Generation of the output voltage \(V_{\text{ref}}\).
The formula for determining output voltage (which should be achieved by modulation) $V_{\text{ref}}$ depending on the standard vector of boundary voltages and the closing time of the key:

$$V_{\text{ref}} = \alpha V_1 + \beta V_2,$$  

where $\alpha = T_1/T_s$ and $\beta = T_2/T_s$.

Substitute equation (8) into equation (6):

$$V_{\text{ref}} = \sqrt{3} \left( \frac{V_{\text{ref}}}{V_{dc}} \right) \left[ \sin \left( \theta - \frac{(k-1)\pi}{3} \right) + \sin \left( \frac{k\pi}{3} - \theta \right) \right],$$  

where the voltage modulation ratio can be expressed as $m = V_{\text{ref}}/V_{dc}$.

This modulation provides very good performance and generates fewer current harmonics [6]. However, during practical implementation, the determination of the sequences involves a calculation of the tangent of the angle of the vector which causes unwanted singularities. This led us to consider the duty cycle modulation technique to generate the SVPWM signals.

4. Results and Discussion

In the instance of a 5 L – SMC H-bridge three-phase multicell inverter, the simulation work was done with the MATLAB/Simulink software. The FFT block in Powergui is used to calculate THD percent values. The performance and ruggedness of the 5 L-SMC H-bridge three-phase multicell inverter are demonstrated and validated using simulation data. Table 3 lists the electrical simulation parameters.
Figure 10: Neutral voltages ($V_{an}$, $V_{bn}$, and $V_{cn}$) and currents ($i_a$, $i_b$, and $i_c$).

Figure 11: Spectrums of (a) neutral voltages ($V_{an}$, $V_{bn}$, and $V_{cn}$) and (b) currents ($i_a$, $i_b$, and $i_c$).
Using conventional SVM control, the simulation of the system allows us to obtain the characteristics of the voltage and the current, as well as their harmonic spectra in Figures 6–9.

After the application of the DCSVM, the characteristics of the voltage and the current, as well as their harmonic spectra, are obtained in Figures 10–13. Figures 10 and 11 present, respectively, signals of the phase-to-neutral voltages and that of the currents produced by the inverter.

Figure 11 shows the harmonic spectrum of the phase-to-neutral voltages and that of the currents produced by the 5L-SMC H-bridge inverter.

Figures 12 and 13, respectively, show the line voltages with its harmonic spectrum (Figures 12(a) and 12(b)) and the filtered line voltages with its harmonic spectrum (Figures 13(a) and 13(b)).

Table 4 reports the performance of simulations of the 5L-SMC three-phase H-bridge inverter using SVM and DCSVM commands.

It is observed that the voltages (between phase and neutral, line) at the output of the inverter present a THD and reduced fundamentals using the DCSVM command compared to the results that the SVM command can obtain. On the other hand, with the DCSVM command, the THD and the fundamental of the current are raised compared with the SVM command that gives low values. However, the THDs of the voltage and current are too high compared to the limits set by the standard IEC 61000.

The power loss distribution in each switch of the 5L-SMC H-bridge inverter is shown in Figure 14. When compared to the H-bridge 5L-SMC construction, the major advantage of stacked multicell converters is that they reduce losses. However, despite the fact that not all components switch at the switching frequency and during the modulation period, this structure is component-intensive. The power losses of the 5L-SMC H-bridge inverter, including switching loss and conduction loss, are investigated to assess the effectiveness of the suggested DCSVM control technique.
The equivalent on-state resistance and forward voltage drops define conduction losses, whereas the linear approximation of the voltage and current across the kth switch estimates switching losses [27]. The MATLAB/Simulink was used to calculate the power losses.

With DCSVM control, the 5L-SMC H-bridge inverter can be controlled to distribute the losses to the individual semiconductor components. However, the energy stored in the individual switches is a limitation to extending this structure to more levels. There are always several power components in series that generate the output current, which increases the conduction and switching losses. These losses are not evenly distributed among the different power components.

Table 5 compares the results of DCSVM with sinusoidal pulse width modulation (SPWM) [26], model predictive control (MPC) [5], or discontinuous pulse width modulation (DPWM) [28].
These results show that the energy losses generated by the production of harmonics are recovered and materialized by the increase in voltage and current in the case of DCSVM. From the above, the 5 L-SMC H-bridge multicell inverter gives better performance in terms of THD of the output voltage (41.29%) and current (9.49%) when using a DCSVM controller compared to SPWM, MPC, DPWM, and SVM controls. This converter appears as an interesting structure when the number of output voltage levels increases [15, 20, 23].

5. Conclusion

In this paper, a new three-phase converter structure with DCSVM control is presented. This topology allows the converter voltage stresses to be distributed among several switching cells. It also allows the input voltage to be divided into several fractions to reduce the number of power semiconductors to be switched. The application of DCSVM control to the 5 L-SMC inverter structure reduces the computational effort and faithfully reproduces the same output vectors as a conventional SVM. The simulation results obtained are better than those of the classical SVM control for similar simulation conditions. It should be noted that the voltages and currents give 41.19% for neutral voltages, 41.29% for line voltages, 11.63% for filtered line voltages, and 9.49% for currents, respectively, with fundamental values of 61.51 V, 106.7 V, 98.45 V, and 5.42 A. The THDs of the voltage and current are too high compared to the limits set by the standard IEC 61000. However, many studies can still be conducted for experimental verification of this work.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

On behalf of all authors, the corresponding author states that there are no conflicts of interest.

References

