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Research Article

Design of Polymer-Based Trigate Nanoscale FinFET for the Implementation of Two-Stage Operational Amplifier

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The major motivation behind transistor scaling is the requirement for high-speed transistors with lower fabrication costs. When the fin thickness or breadth is smaller than 10 nm in a trigate FET, charges travel in a nonconfined fashion, resulting in the creation of energy subbands and causing volume inversion. In comparison to the carrier near a surface inversion layer, volume inversion experiences less interface scattering. In large-scale integrations, we have focused on developing a 3D model for surface potential by establishing the three-dimensional Poison's equation and building a unique fin field-effect transistor (FinFET) structure. In this context, there is a growing interest in developing a low-cost, simple solution that combines plastic (polymer) as a substrate and organic materials to create electronics such as monitors and sensors. The research examines characteristics such as silicon width, oxide thickness, doping concentration, metal work-function about gate, and various surface potentials. For different circuit configurations, it also examines the DC and AC characteristics of the FinFET structure. A differential amplifier is built for RF application based on the device specifications. This work is aimed at improving the semiconductor design structure by adjusting device parameters, analyzing the results, establishing the best FinFET device preferences, and selecting an application for the optimized device. The 3D Poisson's equation may be used to create an analytical model of a trigate nanosize FinFET, which can then be tested using a TCAD simulator. By constructing such a FinFET, we can structure and analyze various electrostatic parameters. To facilitate the creation of FinFET-based circuits, including product development, a novel transistor needs a creative device basis. The infrastructure's support denotes a computationally advantageous numerical model that accurately depicts a FinFET. The work presents a compact model for semiconductor manufacturing that permits separate IC productions while achieving higher levels of excellence and using less power. The design outperforms the CMOS by 22.7% in gain, 31.48% in power consumption, and 12.72% in CMRR, while operating at a 5 GHz unity gain frequency.

1. Introduction

Over the last few decades, integrated circuit manufacturers have steadily shortened the physical length of planar silicon metal-oxide-semiconductor field-effect transistors (MOSFET) to improve their power efficiency, speed, and manufacturing cost per transistor. As a result, an undesired impact known as the second-order effect has developed parallel. The leakage current and, as a result, the dissipation of the leakage (static) power are growing due to short channel effects (SCE) [1].

Traditional bulk MOSFET scaling is nearing its conclusion, not just because of manufacturing problems but also because further scaling would not lower power dissipation but would likely raise it dramatically. But then again, Dennard law of scaling still holds good. This law states that, as

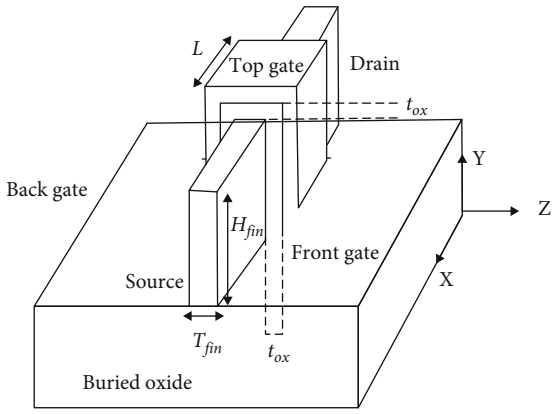


Figure 1: Structure of a basic 3D FinFET.

transistors get smaller, their power density stays constant, so that the power use stays in proportion with area, both voltage and current scale (downward) with length. On the other hand, leakage current poses a great challenge which leads to chip heat up and also leads to power dissipation. With currently available commercial microprocessors operating in the gigahertz range, shrinking the device's size also leads to an increase in operating frequencies [2]. The manufacture of complementary metal oxide semiconductors (CMOS) is now the industry standard. It is also the universal enabler of a staggering number of electronic credentials that have the potential to recast our daily lives [3]. Lower operating power, more performance, and lower standby power are the foundations for future technologies. High-performance logic is associated with significant, sophisticated integrated circuits that require high clock rates and low power consumption, such as a microprocessor system. Static leakage accounts for roughly half of the dissipated power with each chip when using traditional planar, bulk MOSFET scaling. Conventional bulk MOSFET scaling is nearing its conclusion, not only because of manufacturing problems but also because further scaling would significantly increase power dissipation [4–6]. When transistors are scaled down, a new generation of technology or node emerges. Deeper integration, lower energy consumption and higher performance are the parameters to be addressed when the devices are decided to scaled-down [7]. With currently available commercial microprocessors working in the gigahertz range, shrinking the device's size likewise boosts operating frequencies. As a result, every new generation of semiconductor technology streamlines circuit performance and power consumption, allowing the realization of increasingly complex systems [8].

Transistors are linked and correlated towards the top metal layers to attain output power outwardly. Apart from integrating, the connected transistors are used in differential common-source compensated amplifier steps. The neutralization capacitor improves the transistor's stability and maximum possible gain by utilizing the gate-to-drain capacitor's feedback effect. Unit cells were used in the design and a system MOM-cap for neutralization during the input, operator, and output stages. Self-heating due to the centre fins causes a microscopic unit-cell transistor to change quickly, and fingers are gently implanted, resulting in more dependable heat dissipation. Furthermore, the small transistors with quick fan-out to top metals allow adhering to the requisite electromigration criteria easy [9].

Because of the current decrease in MOSFET scaling, new technologies are absolutely necessary. There are two options for getting to the various approaches. The first is to create novel materials that have improved carrier transport characteristics. Second, the new transistor architectures (nonclassical multigate MOSFETs) with superior electrostatics and performance metrics allow for even more device scaling. In multigate, the current drive is determined by the total currents of the gate electrode interfaces if the carriers have equal mobility on all interfaces. Since charge sharing has ramifications inside the surrounding gates, premature inversion rises around the corners of SOI devices. Corner effects are fully parasitic in traditional single gate; however, in multigate, the corners are intrinsic transistors. To ease the creation of FinFET-based circuits, a novel transistor needs a creative device basis. The infrastructure's compliance denotes a computationally advantageous numerical model that accurately depicts a FinFET. A compressed model, on the other hand, is referred to as a spice standard. The paper presents a compact paradigm for semiconductor production that permits separate IC manufactures while achieving higher efficiency and using less power. The investigation's goal is to improve the semiconductor design structure by adjusting device parameters, studying the results, establishing the best FinFET device preferences, and selecting an application for the optimized device. Moreover, the methods for fabricating standard size circuits with SWCNTs (single-walled carbon nanotubes) and organic polymers are not compatible with manufacturing techniques like silicon-based semiconductors. Due to the absence of clearly identifiable on/off behavior, grapheme with polymer's almost zero band-gap semimetallic feature restricts its promise for electronic innovations, making it more ideal for radio-frequency (RF) applications with FinFETs [10, 11].

The objectives of this paper are to (i) examine and evaluate the usability of standard electron transport models used in commercial TCAD simulators for modelling the behavior of nanoscale channel lengths, (ii) develop an analytical model of a trigate nanoscale FinFET using 3-D Poisson's equation, (iii) evaluate the result using a TCAD simulator, and (iv) construct analog/RF circuits with FinFETs that have the best device characteristics and compare their performance to CMOS Analog Circuit Design.

2. Related Works

A 30 nm SOI FinFET Berkeley short-channel IGFET and conventional multigate architecture for OP-Amp design are proposed in [12]. To achieve compactness and lower power consumption in sensor and biomedical applications, researchers used a study technique against subthreshold control using FinFET developed OTA. It denoted, examined, and reasoned that OTA gain is independent of current in the weak inversion region; however, it is dependent in the vital

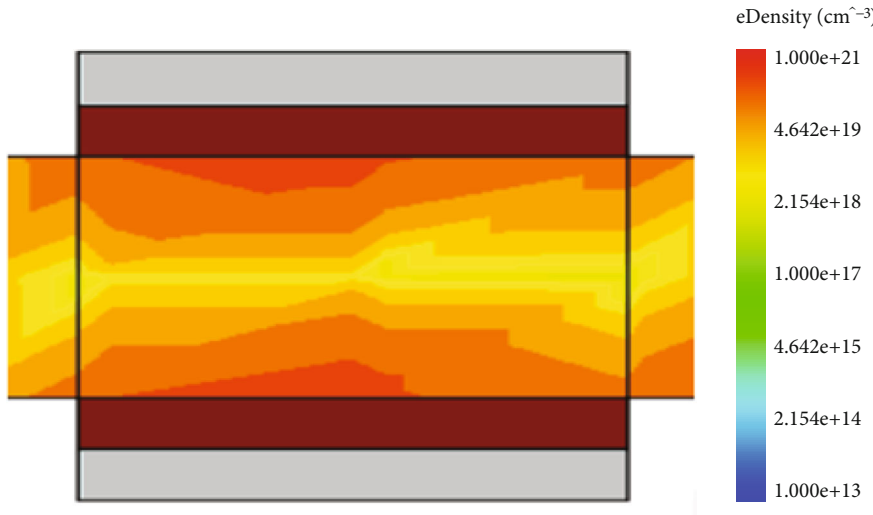


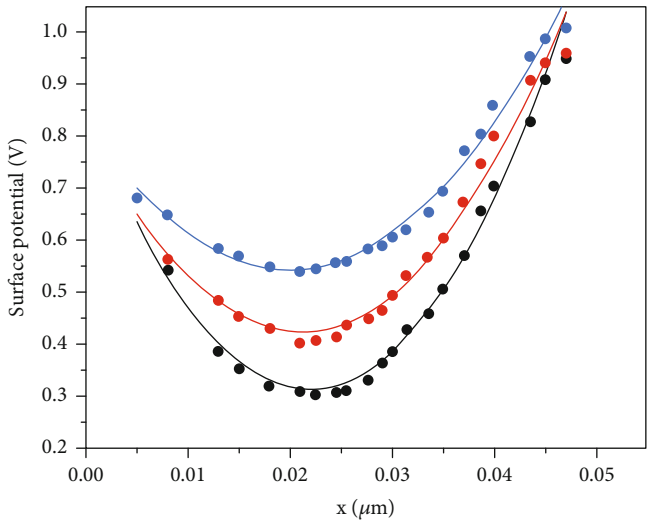
Figure 2: Electrostatic potential within the channel.

inversion region. Thanks to the compensation capacitor, the unity gain margin and slew rate have improved. A sophisticated electrostatic channel potential mathematical model to analyze lightly doped multigate FinFETs and debated how the larger k dielectric material affects the SCE is introduced in [13]. A subthreshold surface potential analytical modeling and the threshold voltage and subthreshold swing using a triple material trigate FinFET are proposed in [14].

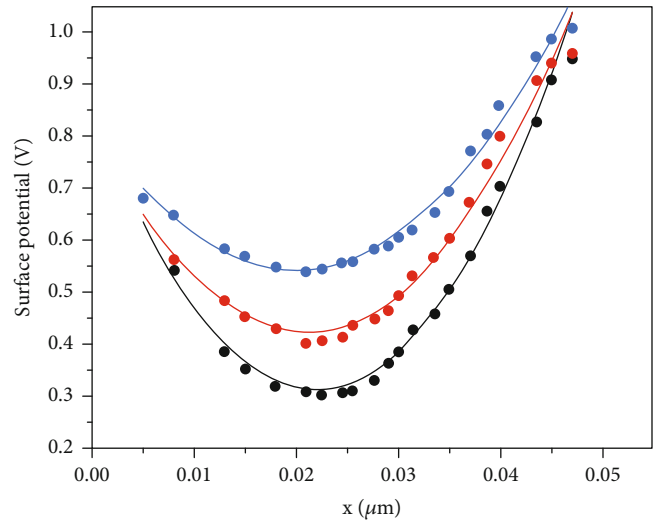
In contrast to TCAD simulated outcomes, analytical model validation is obtained and proved to be more precise. The inherent advantages of applying the source side (dual-kS) and drain side (dual-kD) alone to boost these analog/RF figures of merit (FOM) toward low power performance at a channel length of 20 nm are discussed in [15]. The results show that a FinFET device with a dual-k spacer (inside spacer high k) boosts specific gate fringe field coupling across a specified underlap area on the source side. A bulk FinFET structure with high k spacer Si_3N_4 and low k spacer SiO_2 with a gate length of less than 10 nm is proposed in [16]. The device's DC and AC performances are examined and compared, revealing that spacer material increases the parasitic capacitance and delays through device scaling. The impact of HFin and WFin modifications on various performance indicators is discussed in [17]. Static and dynamic figures of merit (FOM) and specific DC and AC FOMs are all included. Because cut-off frequency (f_T), gate capacitance (C_g), inherent delay, and output resistance (R_O) are offered regularly by the adjustment concerning device geometry guideline, the fixed or low-frequency concerts plus active or high-frequency enforcement are presented constantly. The findings can aid designers in creating 3-D designs that are practically tailored to their needs.

A quantum model of the trigate n-FinFET device using the Bohm quantum potential framework is proposed in [18]. This included quantum confinement effects during specific simulations. Substantial scaling capabilities of FinFET transistors were examined, and the channel length was calculated conservatively. Short channel effects may be achieved by simply altering fin width and gate work function. This research demonstrates that the n-FinFET in the presence of ZrO_2 is a viable device for the CMOS industry's future. The study underlines the importance of doping level in determining the electrical properties of a FinFET channel. Designed an inverted T (IT) FinFET structure and discovered that a fin width (WFin) of less than 10 nm is required for robust gate controllability; otherwise, punch through occurs. Although the resistance to short-channel impact is significantly lower than that of SOI FinFET at significantly scaled L_g, an ideally outlined IT FinFET may deliver a higher current and confirm reduced intrinsic delay discussed in [19]. The Junction less inverted T-shaped gate FET construction and found that I_{ON} rose as channel capacity and fin width grew, and thin thickness suffered greater degradation in threshold voltage. With the same ITSB width, the significant height of fins is required to withstand SCEs and reduce threshold voltage deterioration as channel length decreases proposed in [20].

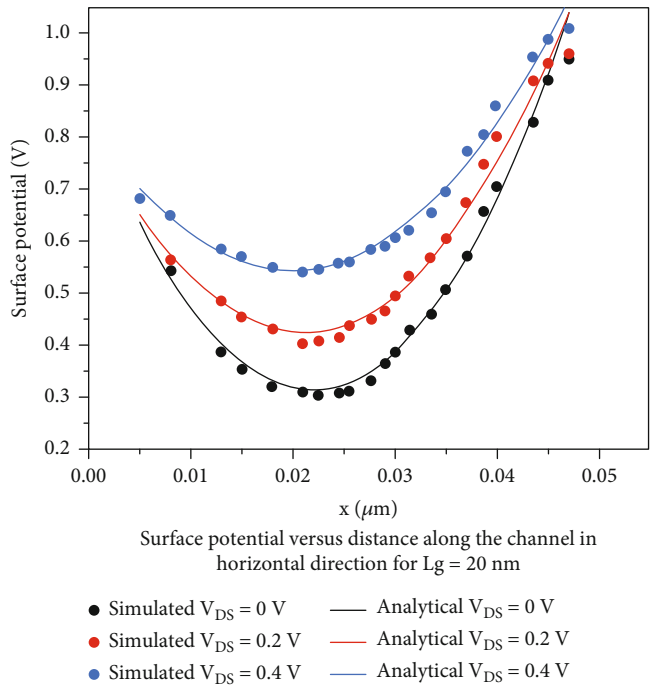
The transistor's external resistance (R_{ext}) is aggressively affected by the extension doping indicated during a specific inclination of the epitaxial expanded S/D. The continued doping orientation varies across external resistance for various threshold voltage (V_{th}) models, including ultralow V_{th}, low V_{th}, ordinary V_{th}, and variable transistor supply voltages (V_{dd}). The channel's electrostatic gate switch is represented as a subthreshold swing (SS_{sat}) with a high drain voltage (V_d). Some SS_{sat} for peak I_{eff} declines with enormous V_{th} essence, including a strategy for FinFET evolution on the scaling domain and a more moderate operation V_{dd} well discussed in [21]. FinFET devices at 14 nm technology node dimensions with and without LDD insertion are proposed in [22]. The V_{tsat} discrepancy between n-MOSFET transistors in neither LDD should drop by 20% if HCI's incorporated design authenticity connected with components among LDD is taken into account. The results show that, in addition to no LDD, FinFET architecture with a more constrained mask delivers greater cost-effectiveness, exciting accomplishment, and area scalability than designs with LDD as major performance and lower power systems.



Surface potential versus distance along the channel in horizontal direction for Lg = 10 nm



Surface potential versus distance along the channel in horizontal direction for Lg = 16 nm



Surface potential versus distance along the channel in horizontal direction for Lg = 20 nm

Figure 3: Surface potential vs. distance along the horizontal channel.

Totally depleting dual-material double-gate (DMDG) MOSFET as a surface potential 2D model is proposed in [23]. This model takes into account the effect of temperature as well as the impression of interface charge density. This model has also taken into account the effects of a large dielectric constant element like HfO_2, predicting that the surface potential on this channel will play a step role that will exceed multiple SCE. As a consequence, the model specifies that the oxide thickness using HfO_2 should be larger than SiO_2 in order to perceive this associated estimation regarding surface potential. Drain current and surface potential models for a physical-based double halo MOSFET in the subthreshold regime are introduced in [24]. Margins with unequal doping were used to regulate the depletion layer extent against pseudo-two-dimensional Poisson's equation. By monitoring each surface potential and draining current models, this classic silicon-dioxide (SiO_2) balances among a dielectric, hafnium oxide (HfO_2).

Because of the complexity associated with transistor scaling down and the emergence of new carrier transport mechanics, standard models can no longer be utilized to simulate such nanoscale devices, as stated above. As a result, particular care should be taken in selecting the appropriate simulation model. In this paper, we have focused on

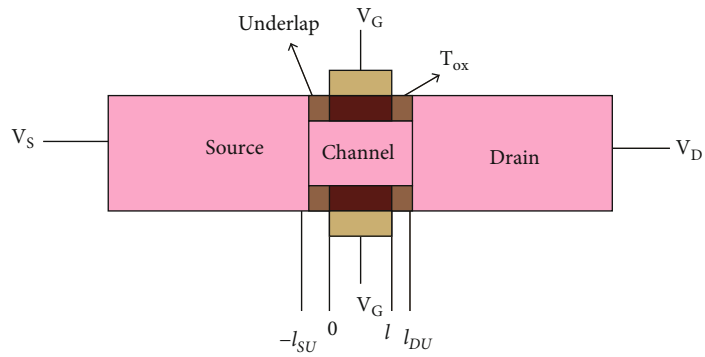


Figure 4: Two-dimensional underlap FinFET structure.

developing a 3D model for surface potential by establishing the three-dimensional Poison's equation and building a unique fin field-effect transistor (FinFET) structure. Further we proposed two-stage operational amplifier for RF application based on the device specifications.

3. Trigate Nanoscale FinFET

The fundamental impetus for transistor scaling is the need for high-speed transistors with lower fabrication costs. This decrease in transistor size or length shrinks circuits, increasing the number of transistors on integrated circuits. Due to the current lack of MOSFET scalability, novel technologies or methodologies are required. There are two options for getting to the various methods: creating a novel material with improved carrier transport properties. Second, the new transistor architectures (nonclassical multigate MOSFETs) with superior electrostatics and performance metrics allow even more device scaling. In multigate, the current drive is determined by the total currents of the gate electrode interfaces if the carriers have equal mobility on all interfaces.

In a trigate FET with a fin thickness or width less than 10 nm, charges can pass in a nonconfined way, resulting in the creation of energy subbands, which causes volume inversion. Compared to the carrier near a surface inversion layer, volume inversion experiences less interface scattering. As a result, the multigate structure has improved mobility and transconductance. Calculating and virtually implementing the channel charge density through a particular representation can result in a simple and compact mathematical model for trigate FinFET, as illustrated in Figure 1. Without interfering with the mobile charge densities at the source and drain, the model expression's drain current can be expressed. It is simple to derive a well-matching mathematical and corresponding 3D mathematical simulation. Through compressed modeling, a mobile deterioration that is expected across velocity overshoots and the scattering mechanism that is part of SCE can be constructed as an outspread version.

The analytical model of trigate FinFET is derived from the solution of Poisson's equation, which implies a little doping concentration in the channel. Due to the strong nonlinearity of the equation across the short channel, the perturbation approach is employed to compute the channel potential based on the three-dimensional Laplace solution. An electrostatic potential expression is retrieved from FinFETs in a doped channel area, recognizing relevant boundary limitations. The three-dimensional Poisson equation has been solved analytically; using the technique of splitting variables about the boundary stands to realize the 3D channel's potential. It is not possible to make fractions of fins due to quantized device width. Therefore, designers can only define the dimensions of the devices in multiples of complete fins. The entire fin area is considered analogous to calculate and formulate the effective silicon fin height (H_{eff}) and effective silicon fin thickness (T_{eff}).

$$\begin{aligned} T_{\text{eff}} &= T_{\text{fin}} + \left(\frac{2S_{\text{si}}}{S_{\text{ox}}}\right) T_{\text{ox}}, \\ H_{\text{eff}} &= H_{\text{fin}} + \left(\frac{S_{\text{si}}}{S_{\text{ox}}}\right) T_{\text{ox}}, \end{aligned} \tag{1}$$

where S_{si} is silicon dielectric permittivity and S_{ox} is the dielectric permittivity of SiO_2. The summation of the channel potential due to top (ψ_{tg}), front (ψ_{fg}), and back gates (ψ_{bg}); source (ψ_{s}); and drain (ψ_{d}) expresses the 3D surface channel potential function (ψ_{3D}):

$$\psi_{3\text{D}} = \psi_{\text{tg}} + \psi_{\text{fg}} + \psi_{\text{bg}} + \psi_{\text{s}} + \psi_{\text{d}}. \tag{2}$$

To validate the analytical model, the 3-dimensional simulator device "Sentaurus TCAD" was utilized to examine the potential surface distribution inside thin-film silicon. We used $V_{\text{sub}} = 0\,\text{V}$, $N_A = 11020\,\text{cm}^3$, $t_{\text{ox}} = 1.5\,\text{nm}$, $V_{\text{ds}} = 0.5\,\text{V}$, and $\varphi M = 4.7\,\text{eV}$ to calculate the surface potential along the channel. Here, $V_{\text{sub}} = 0\,\text{V}$ is used, and the charge density $Q_0 = 0$ is used. The electrostatic potential along the channel is illustrated in Figure 2.

The computed and simulated surface potential values for channel lengths of 10, 16, and 20 nm are graphed in the x -direction with a horizontal distance along the channel. At a fixed drain voltage of 0.4 V_{ds}, the electrostatic charge density increases as the channel X direction is changed. Given that the threshold voltage is determined by the minimal level surface potential near the source junction, it is easier to forecast the proper threshold voltage range for the trigate

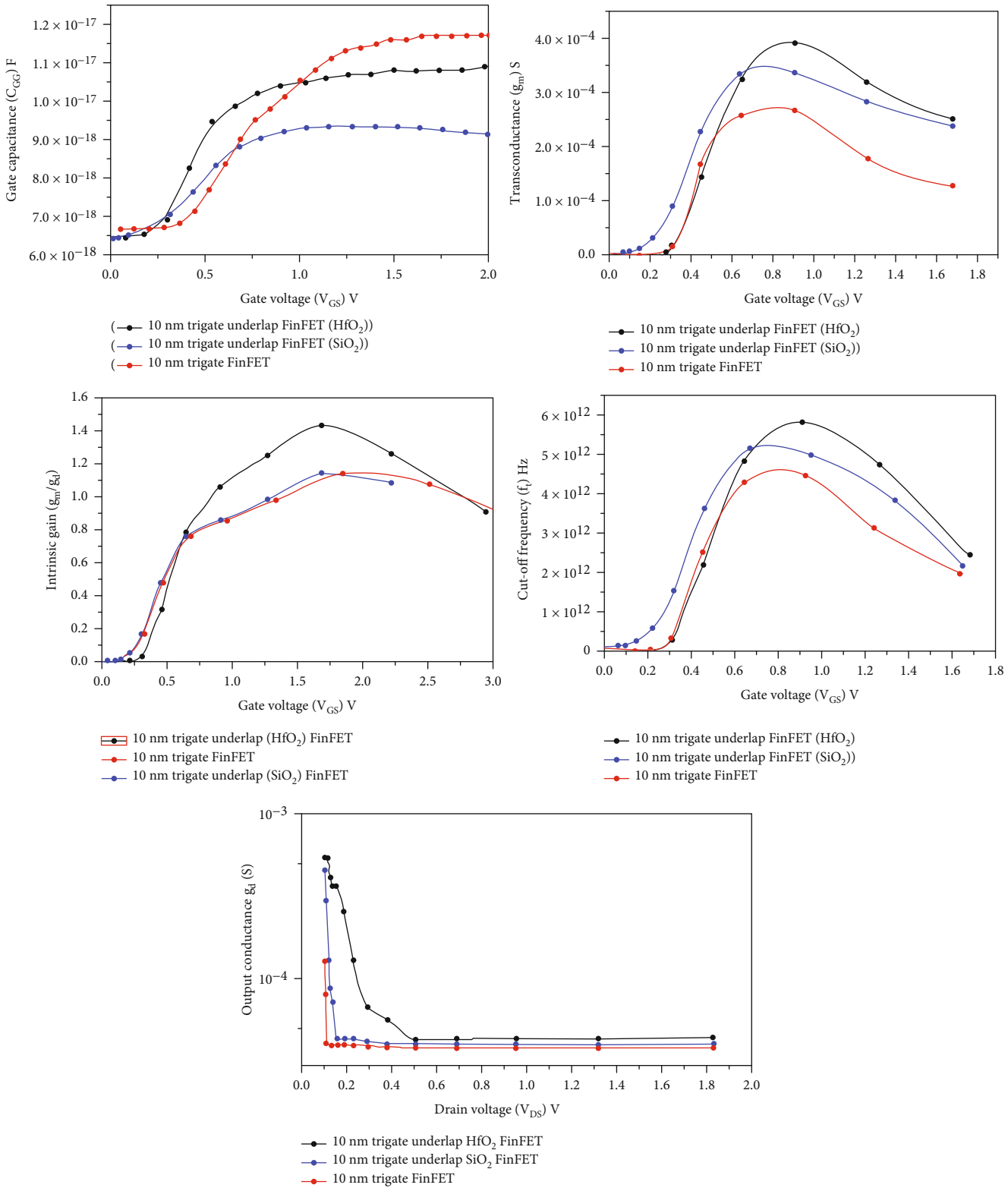


Figure 5: Performance analysis of the FinFET.

FinFET device. The device's performance is slowed by a high threshold voltage, whereas a lower threshold voltage tends to increase the OFF-state leakage current as illustrated in Figure 3. FinFET of 10 nm will have enough electrostatic control because of sufficient gate length which provides good electrostatic control. But beyond 5 nm, it will not have enough electrostatic control.

Quantum mechanical (QM) confinement occurs across the channel of charge carriers in FinFET devices with a very thin fin thickness (10 nm). Both structural and electrical

Table 1: Comparison of analog performance parameters for *n*-type 10 nm FinFET device.

Parameter	Ref. [29]	10 nm FinFET	Proposed trigate underlap (HfO_2) FinFET	Proposed trigate underlap (SiO_2) FinFET
Transconductance (μS)	352	262	390	315
Output conductance e(S)	7.54×10^{-4}	2.84×10^{-3}	8.37×10^{-4}	7.84×10^{-4}
Intrinsic gain (A_{VO})	1.09	1.07	1.4	1.02
Parasitic gate capacitance (F)	1.04×10^{-15}	1.18×10^{-17}	1.05×10^{-17}	0.85×10^{-17}
Cut-off frequency (THz)	0.05390	3.54	5.92	5.90

Table 2: Analog performance parameters towards *n*-type 16 nm SOI FinFET structure.

Parameter	Bias condition	*n*-FinFET
ON current (I_{ON})	$V_{ds} = 0.4$ V	334 (μA/μm)
OFF current (I_{OFF})	$V_{ds} = 0.4$ V	3.19*E*-6 (μA/μm)
Transconductance	$V_{ds} = 0.4$ V	408.2 μS
Threshold voltage	$V_{ds} = 0.4$ V	0.29 V
Subthreshold slope	$V_{ds} = 0.4$ V	77.6 mV/decade
Output resistance	$V_{ds} = 0.4$ V	1.92×10^5 Ω
Intrinsic gain	$V_{ds} = 0.4$ V	1.6
Parasitic gate capacitance	$V_{ds} = 0.4$ V	1.1×10^{-17} F

confinement show the source of these confined carriers [25]. The threshold voltage varies in response to the influence of QM (V_{th}, QM), which may be measured as a function of the carrier's effective mass to free-electron mass as well as the thickness of the silicon film in the confinement direction [26]. When the drain-source voltage V_d is increased beyond the saturation voltage $V_{dsat} = V_g - V_t$, a pinch-off occurs in the channel travelling from the drain to the source. This effect, referred to as channel length modulation (CLM), causes the channel to be slightly shorter than its physical length L [27].

$$L^{\iota} = L - \Delta L, \tag{3}$$

where L' is the gate electrical length due to drain-source voltage V_d and ΔL relates to the difference between L and the pinch-off. λ_{eff} is the effective natural length of trigate FinFET.

$$\Delta L = \lambda_{eff}\, V_{dpinch}. \tag{4}$$

Calculating the channel charge density, which is essentially a specific representation originating from the whole surface and core potential models yields a concise mathematical model for trigate FinFETs. The mobile charge densities at the source and drain are used to create the drain current expression. The mathematically modeled components and the three-dimensional mathematical simulations are well-matched. The compressed model is an outspread design that considers SCE, such as mobility loss due to scattering mechanisms, velocity overshoot, and quantum effects.

FinFETs are widely regarded as the most effective way to achieve higher OFF-state leakage current (I_{OFF}) and drain-induced barrier lowering (DIBL). FinFET technology is widely used in both analogue and digital circuit applications. FOM analogue, transconductance, early voltage, intrinsic DC gain, output conductance, and cut-off frequency are all affected by SCE. It also depends on the gate's influence on electrostatic integrity (EI) in the channel region. Practically, FinFETs are not completely robust to short channel effects but FinFETs have ability to mitigate the short channel effects because FinFETs contain gate all around the fin architecture which gives complete control to gate over the channel which reduces the short channel effects. But the channel control becomes difficult in FinFET. Even though underlap FinFET has a series parasitic rise, downscaling the structure aids in analogue realization. Underlap creation in FinFET structures may limit source-drain junction misalignment and improve SCE immunity.

The electrostatic integration (EI) of the underlap FinFET is superior, and its performance is less immune to interdevice variability and parametric fluctuations [28]. The barrier near the underlap lengths of FinFET is accentuated by spacers in the underlap FinFET as illustrated in Figure 4. The primary reason of the barrier changes is an extension of the gate fringing field, which moves the lateral electric field toward the drain. By increasing intrinsic DC gain, this electric field shift improves transconductance (g_m) while degrading output conductance (g_d).

Because of the lateral electric field swing between the gate edge and the drain, the underlap zone improves gate control by reducing SCE. Analog FOM is considerably enhanced, along with cut-off frequency (f_t), Transconductance (g_m), early voltage ($V_{EA} = I_{ds}/g_d$), and intrinsic DC gain (A_{VO}) [29]. By comparing and plotting the different features of a FinFET, we can analyze the analogous performance for different spacers as illustrated in Figure 5.

HfO_2 and SiO_2 as spacers are used to evaluate the performance of trigate FinFET and underlap trigate. When compared to trigate FinFET without underlap, underlap FinFET has a better overall performance. The underlap trigate FinFET with HfO_2 as a spacer, in particular, overcomes the SCEs with a 14.20% increase in g_m and a 28.44% increase in intrinsic gain, as well as a 5.9 THz cut-off frequency. In the inversion zone, the results show a noticeable linear increase. Because of the improved g_m and cut-off frequency properties, this device compares favorably to regular FinFETs shown in Table 1. It is also well suited for analog/RF

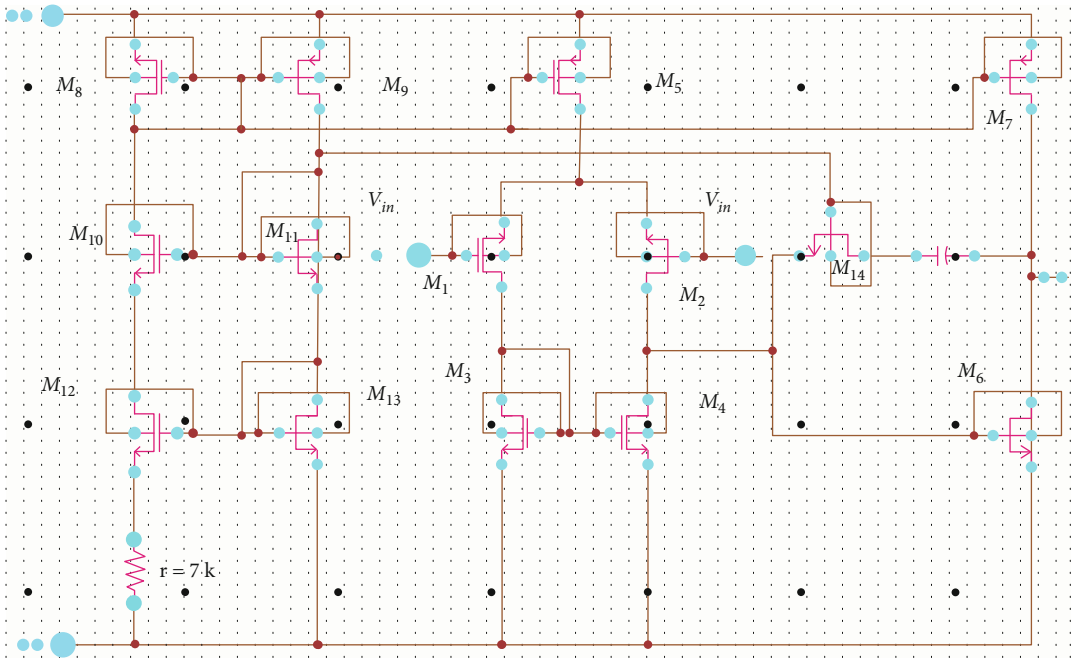


Figure 6: Two-stage differential amplifier block diagram.

applications. Both FinFETs and trigate are frequently seen as belonging to a larger category of devices known as multigate devices. The term trigate is that the channel has gates on three sides of it out of four, whereas FinFET is one of the tri-gate implementations. The orientation in the paper is to elevate the tri-gate-based device.

4. Two-Stage Operational Amplifier Design

Electromagnetic interference (EMI) caused by electronic devices increases noise in the analogue circuit. Because of its low electromagnetic interference capabilities, the OP-Amp is widely used in analogue and mixed-signal systems. Though EMI is added to the input signal and fed into the OP-Amp as an input, its output is either boosted as a common-mode component or rejected as a differential mode component. FinFET can be used instead of tiny CMOS to create an OP-Amp with high gain and low power especially, suitable for design of two-stage operational amplifier because FinFET-based two-stage operational amplifiers give enhanced performance at high voltage and a remarkable great performance at lower supply voltage compared to conventional MOSFET-based two-stage operational amplifiers.

The device's analogue performance is improved through the use of geometrical structure design to acquire optimum parameters [30]. Table 2 shows that subthreshold slope (SS), unity gain frequency, output conductance (g_d), intrinsic gain (A_{VO}), transconductance (g_m), and output resistance (R_O) are among the analogue optimal parameters' equations.

A differential amplifier is followed by a common source polymer-based amplifier in the two-stage OP-Amp, which improves gain and strengthens the output voltage swing. Differential amplifier generates a differential voltage between the inverting and noninverting terminals, which is amplified by the differential amplifier. The differential signal, which is fed as input to the current mirror circuit to create single-ended output voltage, provides active loads to the RF circuit. To improve the amplification, the common source amplifier is used as a buffer. With the help of a biasing circuit, all of the transistors operate in the saturation area. To run the OP-Amp with great stability and over a wider frequency range, a compensating circuit is used [31] as displayed in Figure 6.

Small signal analysis of a differential amplifier includes NMOS (M1 and M2) as the first stage's inverting and noninverting terminals and NMOS (M3 and M4) as the active load. A_{v1} is the voltage gain of the first stage of a differential amplifier. The common source amplifier for gain (A_{v2}) is used in the second stage, with an active load of NMOS (M6) and NMOS (M7) transistors.

$$\begin{aligned} A_{v1} &= G_{m1}R_1 = g_{m2}(r_{o2}\|r_{o4}), \\ A_{v2} &= -g_{m6}(r_{o6}\|r_{o7}). \end{aligned} \tag{5}$$

And the product of the first and second stages is the overall voltage gain:

$$A_0 = A_{v1}A_{v2} = -g_{m2}g_{m6}\,(r_{o2}\|r_{o4})(r_{o6}\|r_{o7}). \tag{6}$$

In the first stage, the total capacitance is (C_1), and in the second stage, the total capacitance is (C_2):

$$\begin{aligned} C_1 &= C_{GD2} + C_{DB2} + C_{GD4} + C_{DB4} + C_{GS6}, \\ C_2 &= C_{DB6} + C_{DB7} + C_{GD7} + C_L. \end{aligned} \tag{7}$$

To build a shunt feedback loop using the Miller capacitance, the drain of the NMOS (M6) transistor is linked to

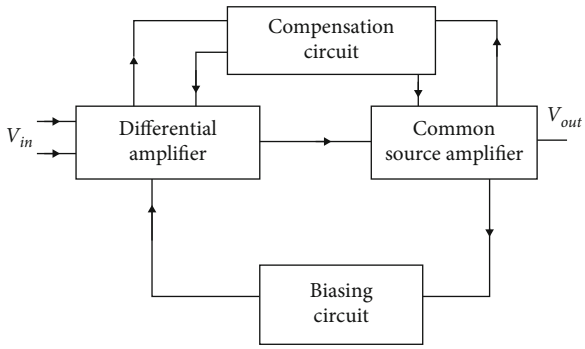


Figure 7: Two-stage differential amplifier design using FinFET.

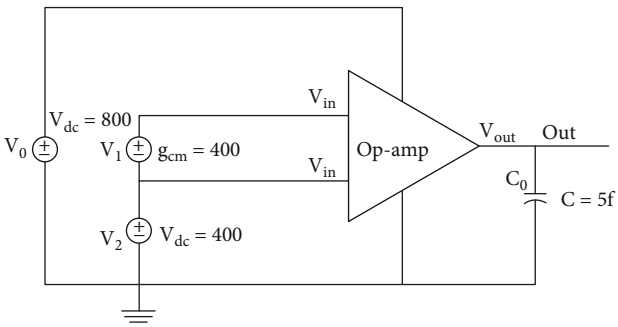


Figure 8: Two-stage OP-Amp with gain enhancement AC analysis.

the gate of the NMOS (M6) transistor (CC). For high-frequency operations, the feedback loop boosts stability. The dominating pole is calculated by combining the first and second stages of total capacitances. The frequency performance at first (f_d) and second poles (f_2) is as follows:

$$f_d = \frac{1}{2\pi R_1[C_1 + C_C(1 + g_{m2}R_2)]},$$
$$f_2 = \frac{G_{m2}C_c}{2\pi(C_1C_2 + C_1C_C(1 + C_2C_C))}. \quad (8)$$

The gain bandwidth product (GBW) at the first stage is expressed as

$$G_{\mathrm{BW}} = A_0 * f_d = \frac{G_{m1}}{C1} = \frac{1}{2\pi C_C}\mu_n C_{\mathrm{ox}}\left(\frac{W}{L}\right). \quad (9)$$

Miller capacitance (CC) increase is thought to aid in achieving improved stability and lowering the gain bandwidth product. Nonetheless, as compared to standard CMOS, the transconductance (g_m) of nano FinFET is high, resulting in better gain bandwidth and unity gain frequency. The two-stage differential FinFET OP-Amp has three phases, namely, the differential phase, common source gain phase, and biasing phase. FinFETs have turned the differential input signal into a single-ended output signal in the first phase (M1-M5). Noninverting and inverting FinFET gate terminals are M1 and M2, respectively. The differential phase gain determines how much the single-ended output is amplified. This phase gain is based on specific transconductance around the M1 FinFET, and it outputs total resistance to the M2 FinFET's drain terminal. The M3 and M4 FinFETs work as active load, single-ended conversion, and CMMR management by acting as a current mirror. The M5 FinFET is used to keep the differential pair's bias constant.

The common source gain phase amplifies the signal from the M2 FinFET using a common source M6 FinFET. This phase's active load will be transistor M7. The gain of the phase is determined by the specific transconductance around M6 FinFET and the total output load resistance toward M6 and M7. The gain improvement is achieved by giving output bias current to M6 and M7 FinFETs. With an active load inverter, this phase acts as a current sink. During the biasing phase, the M8-M13 FinFET transistors are used in current mirror architecture to provide a biasing network and also serve as a current source for the remarkable M5 and M7 FinFET transistors. The current sink for this phase will be the FinFET M5 plus M7 as illustrated in Figure 7.

In the RF region of operation, stray capacitances in the circuit generate an undesired phase shift, which makes the network unstable and difficult to remove. A frequency compensated capacitor (C0) is a series connected to the negative feedback network to maintain steady operation as illustrated in Figure 8. In a closed-loop design, an extra pole is formed during the amplification stage. As a result, if the dominating pole is greater than the new pole location, the phase falls. The C0 capacitor is a capacitor that rejects the effects of poles. To maintain good stability, an RC Miller adjusted circuit is used. The frequency response associated with gain enhancement technique is shown in the diagram below. It was discovered that the gain is 23 dB and that the frequency of unity gain is 5.07 GHz.

5. Results and Discussions

From Figure 9, it can be noticed that the phase has risen to 180 degrees, as can be seen. The RC compensated circuit can boost the unity gain bandwidth by increasing the bias current. When operating at 5 GHz, the circuit consumes a total of 537.1 μW.

The differential polymer-based amplifier is built using 16 nm FinFET technology, and its performance is compared to that of traditional MOSFETs. Using 16 nm FinFET technology, the overall gain increased to 22.7%. The FinFET's strong gm boosts the gain by a significant amount. The operational amplifier's unity gain frequency is 5 GHz, thanks to FinFET technology. FinFET minimizes power dissipation by 31.48% when compared to the reference circuit and provides an ideal bandwidth range. Using a 16 nm FinFET with a constant current bias and current mirror circuit, the CMRR was enhanced to 12.72%. When compared to ordinary MOSFETs, the FinFET OP-Amp produces better results. FinFET technology outperforms CMOS technology in terms of gain and unity gain frequency. The frequency of unity gain is 5.07 GHz, which is suitable for RF models. The same can be concluded by observing Table 3. This proposed novel model also provides scope for cost effective chip

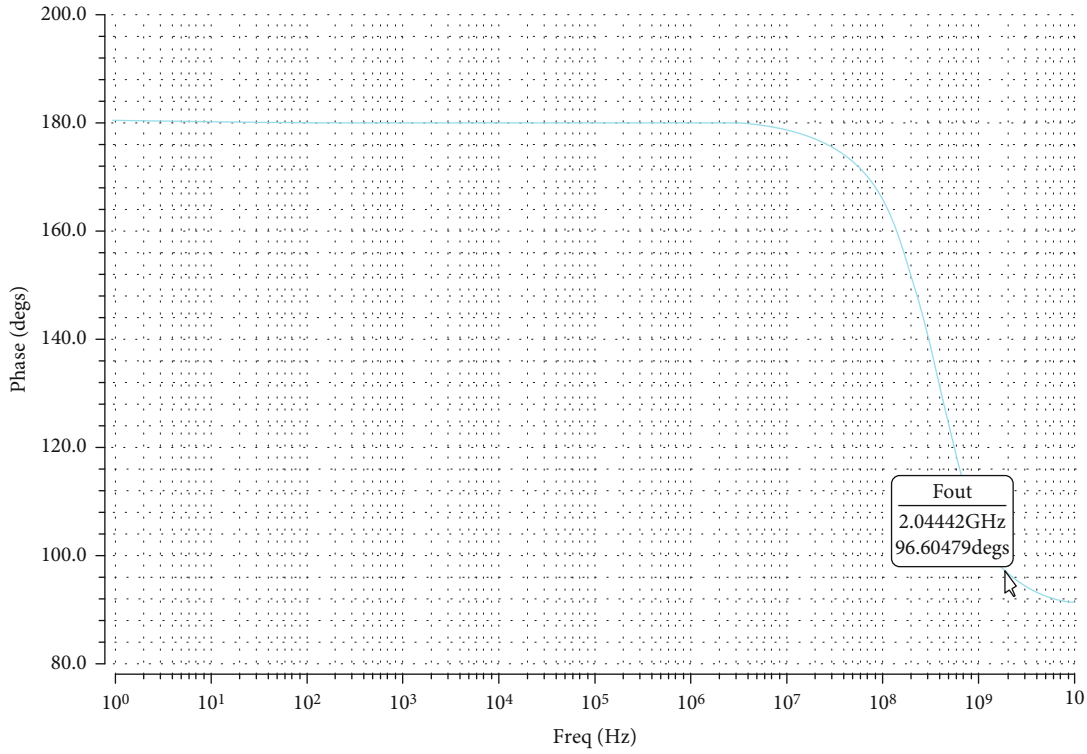


Figure 9: Phase plot of FinFET two-stage OP-Amp.

Table 3: Comparison table of polymer-based two-stage differential OP-Amp with CMOS and FinFET technology.

Parameter	Ref. [32]	Ref. [12]	Proposed method
Technology node	16 nm FinFET	30 nm CMOS	16 nm FinFET
Mode of operation	Saturation	Saturation	Saturation
VDD (V)	0.9	1.8	1
Gain (dB)	19.3	61.7	23.7
Unity gain frequency (GHz)	2.47	0.475	5.07
Power consumption (μW)	784	1258	537.1
CMRR (dB)	68	64.2	76.67

design, especially for low power, high speed, and area efficient applications.

6. Conclusions and Future Scope

CMOS scaling has emerged as the most important predictor of silicon technology advancement in terms of improving performance and incorporating more functions into a chip. The goal of this research was to develop a three-dimensional polymer-based trigate FinFET and a circuit utilizing the implemented compact model. FinFET is a three-dimensional structure that conducts channels around a vertical fin in three facets to improve driving current and functions as totally depleted for superior performance. With rising HFin, both I_{ON} and I_{OFF} increase. Because of its low electromagnetic interference capabilities, the OP-Amp is widely used in analogue and mixed-signal systems. With its 16 nm predictive technology model (PTM) FinFET, it is building a high gain and low-power FinFET polymer-based two-stage OP-Amp. Create a TCAD SPICE file with the FinFET device in it. The SPICE file has a lookup table-based model of the TCAD device. The design outperforms the CMOS by 22.7% in gain, 31.48% in power consumption, and 12.72% in CMRR, while operating at a 5 GHz unity gain frequency. Process variation in multigate devices is another issue that needs to be addressed in order to achieve device performance. The performance of the planned underlap FinFET is less immune to interdevice variability and parametric fluctuations, and it has better electrostatic integration (EI). In the future, new architectures such as negative capacitance, FETs that operate in the terahertz frequency range, and entirely depleted SOI for quantum computing are planned. As a result, greater gains in gate control over lower V_{DD} can be obtained.

Data Availability

There is no data availability statement for this manuscript.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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