

Editorial

Current Trends on Reconfigurable Computing

**Jürgen Becker,¹ Michael Hübner,¹ Roger Woods,² Philip Leong,³
Robert Esser,⁴ and Lionel Torres⁵**

¹ Universität Karlsruhe (TH), 76131 Karlsruhe, Germany

² Queens University Belfast, Belfast BT7 1NN, Northern Ireland

³ Chinese University Hong Kong, Hong Kong

⁴ Xilinx Inc., San Jose, CA 95124, USA

⁵ Le Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier (LIRMM),
Université Montpellier II/CNRS, 161 Rue Ada, 34392 Montpellier, France

Correspondence should be addressed to Jürgen Becker, becker@itiv.uni-karlsruhe.de

Received 15 December 2008; Accepted 15 December 2008

Copyright © 2008 Jürgen Becker et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

This special issue covers actual and future trends on reconfigurable computing given by academic and industrial specialists from all over the world. In the issue, Boukhechem and Bourennane address transaction-level modeling, a promising technique for increasingly complex embedded system. They present a technique for modeling, validating, and verifying an open embedded platform which allows faster and more efficient architecture exploration. Puschini et al. argue that future systems will have distributed decision making capability, one of which will be to control the voltage scaling in the device. They apply game theory to the run-time optimization of the frequency of multiprocessor SoC platforms, resulting in a temperature reduction. The work by Amagasaki et al. outlines an approach for varying the granularity of an FPGA logic cell when implementing arithmetic and random logic. The resulting cell gives improved logic depth and needs less reconfiguration data when compared to a Xilinx Virtex-4 device. Siozios et al. have presented tools for exploration of alternative interconnection schemes for 3D FPGAs which provide partitioning, placement and routing, and power estimation. The work on medical image registration by Dandekar et al. outlines a novel multiobjective optimization strategy for exploring the tradeoff between FPGA resources and implementation accuracy. Craven and Athanas present work on a high-level development environment for reconfigurable designs, that leverages an existing high-level synthesis tool to enable the design, simulation, and implementation of dynamically reconfigurable hardware based on a C specification. Guilleminet et al. looked at the integration

of field-induced magnetic switching and thermally assisted switching magnetic RAMs in FPGA design, highlighting reductions in both power consumption and configuration time at power up when compared to classical SRAM-based FPGAs. The work by Steiner and Athanas describes the computing infrastructure that needs to be included in order to allow a system to change its operation without requiring outside intervention. Together, we hope that this special issue will serve as an introduction to users who have newly joined the community as well as provide specialists with recent results in this field of research.

Jürgen Becker
Michael Hübner
Roger Woods
Philip Leong
Robert Esser
Lionel Torres

