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Corrigendum

Corrigendum to "An Impulse-C Hardware Accelerator for Packet Classification Based on Fine/Coarse Grain Optimization"

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In the article titled "An Impulse-C Hardware Accelerator for Packet Classification Based on Fine/Coarse Grain Optimization" [1], the authors acknowledge the minor reuse of text from their following two conference papers:

(1) M. Walton, G. Grewal, and G. Darlington. 2010. "Parallel FPGA-based implementation of scatter search". In Proceedings of the 12th annual conference on Genetic and evolutionary computation (GECCO '10). ACM, New York, NY, USA, 1075–1082. doi: https://dx.doi.org/10.1145/1830483.1830683.

(2) O. Ahmed, K. Chattha and S. Areibi, "A hardware/software co-design architecture for packet classification," 2010 International Conference on Microelectronics, Cairo, 2010, pp. 96–99. doi: 10.1109/ICM.2010.5696215.

References

[1] O. Ahmed, S. Areibi, R. Collier, and G. Grewal, "An impulse-C hardware accelerator for packet classification based on fine/coarse grain optimization," *International Journal of Reconfigurable Computing*, vol. 2013, Article ID 130765, 23 pages, 2013.