A Fuzzy-Based Coordinated Power Management Strategy for Voltage Regulation and State-of-Charge Balancing in Multiple Subgrid-Based DC Microgrid

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Multiple DC subgrids in close proximity can be connected to form a DC microgrid. The interconnected DC subgrids enhance reliability and efficient utilization of resources. In this paper, a novel coordinated power management strategy is proposed for interconnected subgrids of a DC microgrid. Each DC subgrid has PV and battery units. The proposed strategy is implemented on interlinking bidirectional converters (IBCs). The strategy considers the state-of-charge (SoC) and charging/discharging current of the batteries for SoC balancing-based power sharing through IBCs. A fuzzy logic controller is implemented to decide the amount of power flow through the IBCs from SoC and the charging/discharging current of battery units. Moreover, with the coordinated strategy, a high SoC battery takes more loads compared to a lower SoC battery. The proposed strategy supports fast charging and fast discharging of batteries depending on the SoC level. In addition, the coordinated strategy can seamlessly transfer the control of IBC from the power regulating mode to the voltage regulating mode without any additional control scheme during an outage of the battery unit. The feasibility of the proposed strategy is validated through simulation in MATLAB/Simulink and OPAL-RT real-time digital simulator.

1. Introduction

With renewable energy sources (RESs) and storage systems such as photovoltaic (PV), wind generators, fuel cells, and batteries, DC microgrids (DCMGs) are gaining importance in day-to-day life. DCMGs have advantages over AC microgrids like higher efficiency due to fewer conversion stages, no transfer of reactive power, and no synchronization issue [1–4]. The excessive addition of unpredictable RESs and uncertainty in load variations create challenges in managing the stability of DCMG [5]. To improve the reliability and stability of DCMG, multiple subgrids can be interconnected in close vicinity to form a DCMG cluster. The interconnected subgrids can support each other in a coordinated way. The main advantages of interconnected DC subgrids are (1) the need for fewer energy storage units, (2) full utilization of RES and energy storage units, (3) optimal economic dispatch through coordination control, and (4) enhanced stability and reliability of DCMG [6–8].

In general, multiple subgrids of a DCMG can be connected through tie-line and breakers [9, 10]. The tie-line-based interconnection may reduce the flexibility of DCMG. The plug-and-play features of DC subgrids are also influenced, which reduces the scalability of DCMG. To enhance the flexibility and reliability of interlinking DC subgrids, multiple DC subgrids can be connected through interlinking bidirectional converters (IBCs). In [11, 12], a centralized structure-based coordination control strategy for IBC has been discussed, which relies on communication lines. Although the centralized controller has better controllability and observability control, it has communication failure issues, less reliability, scalability, and flexibility issues [13]. To improve the system’s reliability, decentralized droop control techniques are widely adopted [14–16]. The droop control
strategies provide reliable and flexible operation of DCMG. However, the major drawback of the droop control strategy is poor voltage regulation, which may affect voltage-sensitivity loads. Moreover, the droop strategy may lead to circulating current problems in DC subgrids. To avoid these issues, secondary controllers are added above the primary droop controller in DC subgrids [17]. For the secondary controller, the low bandwidth communication (LBC) channel shares the desired information to mitigate the voltage droop error and establishes a coordinated power flow among the subgrids [18].

In [19], a coordinated power sharing strategy using the secondary controller is presented. In the presented method, load demand information is shared over LBC to the secondary controllers of local generation and IBC. The implemented strategy regulates the DC bus voltage at its reference value. However, SoC balancing strategy has not been established. A coordinated power management strategy for a DCMG cluster is implemented in [20]. With the proposed strategy, battery capacity-based power regulation and bus voltage regulation have been achieved. However, SoC-based power regulation among the subgrids has not been considered in the presented strategy. Further, the peak voltage deviations are more than 5% of their nominal values.

A hybrid control structure for interconnected DCMGs is proposed in [21]. The proposed structure mainly focuses on the regulation of DC bus voltages. However, the presented method does not consider the SoC of the battery and the peak capacity of individual subgrids. In [22], a power sharing strategy using a common bus is proposed for interconnected DCMGs. In the presented strategy, common bus voltage information is used for power sharing. However, the proposed strategy does not consider the SoC balancing of storage units. Further, the common bus voltage oscillates with the change in load demand. In [23], a power sharing strategy using a priority-driven IBC control technique is proposed. In this strategy, the IBC power regulation depends on the bus voltage deviation of DCMG. Further, SoC balancing-based power management has not been addressed in the proposed method.

A power sharing strategy for multiple subgrids through the interlinking bidirectional converters is proposed in [24]. The proposed strategy tunes the IBCs from normalized voltage error information obtained from different subgrids.

A coordinated secondary control strategy is added to improve the DC bus voltage regulation as well as the power sharing performance of IBCs. In [25, 26], a power management strategy using DC bus-signaling method is proposed. In this strategy, the DC bus voltage is regulated by battery controllers. However, overcharging and over-discharging of the battery have not been considered. An SoC-based power management scheme is presented in [27].

In this strategy, the DC bus voltage is regulated by the secondary controller of the battery. However, the proposed strategy is not suitable for the interconnection of subgrids. A tie-line-based power management scheme for interconnected DCMGs is proposed in [28–30]. In this structure, the power flow among the DCMGs depends on the voltage droop characteristics of the DC buses. Hence, with this structure, nominal DC bus voltage regulation is difficult to achieve, and the flexibility of DCMGs may reduce.

From the aforementioned literature, a coordinated power sharing strategy for interconnected DC subgrids is a challenging task. Further, the power sharing strategy should consider the SoC balancing of the battery units and nominal voltage regulation of DC buses. To overcome these issues, a coordinated power management strategy (CPMS) considering SoC and DC bus voltage is proposed in this paper. The proposed coordination strategy is implemented on three DC subgrids connected through IBCs. Each subgrid has a PV, a battery unit, and DC loads connected to its DC bus. For SoC balancing and coordinated power sharing among the subgrids, a fuzzy-based coordinated secondary control technique for IBC is proposed.

The main contribution of the proposed strategy can be summarized as follows:

1. A fuzzy-based CPMS is proposed for IBC control. The fuzzy-based CPMS is robust and ensures reliable operation and critical control of DC bus voltage magnitude during load switching.
2. The proposed CPMS enables a low SoC battery to fast charge than a high SoC battery, which restrains the deep discharge of a low SoC battery. Further, the CPMS enables a high SoC battery to charge at a slower rate and take more load demand. Hence, overcharging of the battery can be avoided.
3. The CPMS can regulate the DC bus voltage of each DC subgrid at its nominal value. Hence, the voltage-sensitive loads remain unaffected by changes in load demand, unlike the droop control strategy.
4. The proposed strategy supports the plug-and-play operation of storage. Moreover, with the proposed CPMS, a seamless mode transition with improved transient stability can be established.

The rest of the paper is organized as follows: configuration of DCMG, voltage regulation strategy for subgrids, and IBC controller are illustrated in Section 2. The coordinated power sharing strategy is illustrated in Section 3. In this section, SoC-based coordination control strategy with fast charging and discharging of battery is manifested. The mathematical model of converters, stability analysis, and sensitivity analysis are illustrated in Section 4. Simulation results are shown in Section 5 to verify the power sharing strategy. Section 6 concludes the paper.

2. Structure and Control of DCMG

2.1. Structure of DCMG. Figure 1 shows the structure of interconnected subgrids of a DCMG. Three DC subgrids are connected to form an islanded DCMG. These subgrids are connected through two interconnected IBCs. The proposed configuration can be extended to more subgrids when necessary. In each subgrid, battery and PV generations are included. The battery terminal regulates the DC bus voltage, and PV operates as a constant power source.
2.2. Coordinated Power Management Strategy. The coordinated power management strategy includes regulation of DC bus voltage and SoC-based power sharing among the subgrids. The DC bus voltage regulation is managed by a battery controller, and SoC-based power sharing is managed by an IBC controller. These controllers operate in multilayer structures with different time scales. For the battery controller, the droop-based primary controller layer and DC bus voltage regulation-based secondary control layer are implemented. For the IBC controller, the primary controller is the conventional power regulating controller, and the secondary controller is the SoC balancing-based power sharing control strategy. Further, the PV generation in each subgrid operates in maximum power point tracking (MPPT) mode or power control mode. Hence, for the PV generation regulation, the existing control strategy in [31] is implemented. A detailed analysis of PV controller is not discussed in this paper. In this section, a detailed analysis of battery control and IBC control strategies is elaborated.

2.2.1. Battery Controller. The battery controller consists of a primary control loop and a secondary control loop, as shown in Figure 2. The primary droop control technique for voltage regulation of DCMG can be expressed as [32]

\[
V_{\text{ref}} = V_{\text{nom}} - a \cdot P_b,
\]

\[
a = \frac{V_{\text{max}} - V_{\text{nom}}}{P_{b_{\text{max}}}},
\]

where \( V_{\text{ref}} \) is the reference DC bus voltage, \( V_{\text{nom}} \) is the nominal DC bus voltage, \( a \) is a voltage droop gain, \( V_{\text{max}} \) is the maximum DC voltage at the output of the converter, \( P_b \) is the power of the battery, and \( P_{b_{\text{max}}} \) is the peak power of the battery.

The primary droop controller is the fastest control loop in the power management strategy. It ensures the voltage stability of the DCMG. However, the droop-based control of the battery controller causes DC bus voltage deviation while regulating the generation and demand. Hence, a secondary control structure is included in each battery controller to restore the DC bus voltage to its nominal value. The DC bus voltage is measured and sent to the secondary layer through a low bandwidth communication (LBC). A PI controller is used to generate a voltage correction factor for the primary layer as follows:

\[
\delta V_m = \left( k_{ps} + \frac{k_{is}}{s} \right) (V_{\text{nom}} - V_{\text{dc}}),
\]

where \( k_{ps} \) is the proportional gain, and \( k_{is} \) is the integral gain of the secondary PI controller. The shifting term \( \delta V_m \) shifts the line droop characteristics to maintain the bus voltage at its nominal value.

2.2.2. IBC Controller. In each IBC, two layers of control structures are used, similar to the battery control strategy. The primary control layer of the IBC is the power control loop. The main aim of the primary loop is to track the reference power generated by the secondary control layer. The secondary control layer is included in the IBC control structure to improve the power flow among the subgrids based on the DC bus voltage of each subgrid. In the conventional IBC control, the normalized DC bus voltage deviation-based IBC control strategy is adopted, benefiting
coordinated power-sharing among the subgrids. The normalized DC bus voltage deviation \( NV_i \) can be expressed as [24]

\[
NV_i = \frac{V_{\text{nomi}} - V_{\text{dci}}}{n_i},
\]

where \( V_{\text{dci}} \) and \( V_{\text{nomi}} \) are the lower and upper limits of DC voltage of \( i \)th subgrid, respectively. At balance condition, i.e., \( NV_1 = NV_2 \), the power flow through the IBC does not require to be changed. At unbalance condition, a secondary controller is added to impel \( NV_1 = NV_2 \). However, the secondary battery controller also eliminates the normalized voltage deviation. Therefore, the normalized voltage deviation-based IBC secondary controller is inept in maintaining the supply and demand of subgrids from the normalized voltages. It results in poor performance of the IBC power sharing strategy. To achieve coordination in power sharing, the LBC can be utilized as an information carrier. By using LBC, a coordinated secondary control strategy for the IBC is proposed. A detailed analysis of the proposed coordinated secondary IBC control strategy is elaborated in Section 3.

### 3. Proposed Coordinated Secondary IBC Control

Figure 3 shows the power regulation control structure of an IBC. By using LBCs, a coordinated secondary controller is developed for the IBC with the awareness of the DC bus voltage, SoC, and \( I_b \) information of connected subgrids. The coordinated IBC secondary controller has two objectives, named as (i) SoC-based power sharing and (ii) seamless transfer of IBC controller from power sharing mode to voltage regulation mode and vice versa during plug-and-play of the battery unit in a subgrid. A detailed analysis of the seamless transfer of the mode of the IBC controller is discussed in Section 4. In this section, SoC-based power sharing strategy with fast charging and fast discharging operation mode is manifested.

#### 3.1. SoC-Based Power Sharing

For proportional power sharing of battery units, each IBC needs the SoC levels and charging/discharging current information of battery units of its connected subgrids. Using the LBC, the SoC and charging/discharging current information of batteries is sent to the IBC secondary controller. By gathering the information on DC bus voltage, SoC, and charging/discharging current of the battery, the IBC secondary controller generates a modified normalized voltage for each subgrid. The modified normalized voltage \( NV_i \) can be expressed as

\[
NV_i = \frac{V_{\text{nomi}} - V_{\text{dci}} - \Delta V_v}{n_i},
\]

The adjusted virtual voltage deviation \( \Delta V_v \) is proposed considering depth-of-discharge (DoD) and depth-of-charge (DoC) in discharging and charging mode, respectively. \( \Delta V_v \) is defined as

\[
\Delta V_v = \begin{cases} 
    k \times (\exp(\text{DoC}) - 1) \times \frac{I_b}{\Delta I_b}, & \text{if } I_b < 0, \\
    k \times (\exp(\text{DoD}) - 1) \times \frac{I_b}{\Delta I_b}, & \text{if } I_b > 0,
\end{cases}
\]

where \( \text{DoC} \) is the lower cut-off SoC of battery, \( k \) is a constant, \( I_{b_{\text{max}}} \) is the peak discharging limit, and \( I_{b_{\text{min}}} \) is the peak charging limit. \( I_b \) represents the battery charging mode, and \( I_b > 0 \) represents the battery discharging mode. From (4), the power errors through the IBCs \( \Delta P_{e_{12}}, \Delta P_{e_{13}} \) can be defined as

\[
\begin{align*}
\Delta P_{e_{12}} &= NV_1 - NV_2 \\
\Delta P_{e_{13}} &= NV_1 - NV_3
\end{align*}
\]

It can be observed that if the power errors can be minimized, the power flow through the IBC will be linked with the SoC and charging/discharging current of batteries. Hence, a SoC balancing-based power sharing among subgrids can be established by eliminating power errors. In this paper, a fuzzy logic controller is used for IBC secondary controllers to eradicate the power errors. The fuzzy logic controller is robust compared to the conventional PI controller, and it can cover a wider operating range of DC bus voltages. Moreover, the fuzzy-based control strategy can minimize voltage transient during load switching compared to the conventional control strategy. The control diagram of the fuzzy-based secondary IBC controller is manifested in Figure 4(a).
The modified normalized voltages are the inputs to the fuzzy logic controller, which calculate the change in IBC power to transfer among the subgrids. In the fuzzy logic controller, input and output variables have 7 membership functions, as shown in Figures 4(b) and 4(c). The membership functions are defined in Table 1. Table 2 shows the fuzzy rules for the IBC secondary controller. The generated reference power of IBC is given to the primary controller of the IBC.

3.2. Fast Charging and Discharging Mode. The concept of fast charging and fast discharging of battery is added to prevent a low SoC battery from deep discharge and prevent a high SoC battery from overcharge. If a battery operates below a specific SoC limit, it should charge quickly and discharge slowly. Similarly, if a battery operates beyond a certain SoC limit, then it should operate at fast discharging to balance the SoC limit and charge slowly to avoid overcharging condition. To incorporate the fast charging and fast discharging conditions, the secondary IBC control strategy is further modified depending on the three SoC levels. These three SoC levels are defined as normal SoC mode (NSM), high SoC mode (HSM), and low SoC mode (LSM). Hence, the SoC-based virtual voltage deviation is modified based on the three operating modes of the SoC. The modified virtual voltage deviation is shown below.

In charging condition,

\[
\Delta V_v = \begin{cases} 
  k \times (\exp(Do_C) - 1) \times \frac{I_b}{\Delta I_b}; & \text{if } SoC_l < SoC < SoC_u (NSM), \\
  \left( k \times (\exp(Do_C) - 1) - \frac{SoC - SoC_u}{100} \right) \times \frac{I_b}{\Delta I_b}; & \text{if } SoC < SoC_l (HSM), \\
  \left( k \times (\exp(Do_C) - 1) + \frac{SoC - SoC_l}{100} \right) \times \frac{I_b}{\Delta I_b}; & \text{if } SoC > SoC_u (LSM). 
\end{cases}
\]

In discharging condition,
4. Control of Converters and Stability Analysis

In this section, modeling of battery, PV, and IBC converters is defined. The small signal models of these three converter controls are analyzed for the design of the converter controllers.

4.1. Small Signal Model of PV and Battery Controller. The block diagram of the PV and battery controller is shown in Figure 6. For the PV controller, a PI regulator is implemented for power regulation of the PV terminal. The reference power for the PV controller is generated from an MPPT strategy. This paper does not conduct a detailed analysis of the MPPT technique. The implementation of the MPPT technique can be followed in [33,34]. The battery controller regulates the DC bus voltage, and the PV controller operates as a power source for the DC subgrid. The battery converter has a primary loop and a secondary loop. The secondary loop aims for nominal DC bus voltage regulation. Hence, it generates a desired reference DC bus voltage for the primary loop. The control response of the secondary controller is analyzed considering the time delay ($T_d$). For each subgrid, the dynamics of the battery terminal output for voltage regulation are shown as follows [20]:

$$
\Delta P_{b1} = \frac{u_b i_i}{T_f} = \frac{u_{b1}}{T_f} \left[ (\Delta u_{ref1} - \Delta u_{dc1}) \left( k_{pu1} + k_{i1} \right) \right] G_{ii}(s),
$$

$$
\Delta u_{ref1} = \Delta u_{nom1} - a \Delta P_{b1} + (\Delta u_{nom1} - \Delta u_{dc1}) \left( k_{pu1} + k_{i1}/s \right) \left( 1 + sT_d \right),
$$

where $u_b$ is the battery voltage, $i_i$ is the inductor current, and $k_{pu1}$ and $k_{i1}$ are the proportional and integral gains of the voltage loop PI controller, respectively. Subscript ‘1’ indicates subgrid-1. $P_i$ is the base value of power, and $a$ is the voltage droop coefficient. $G_i(s)$ is the closed-loop transfer function of the inner current loop of the battery controller. $G_{ii}(s)$ can be expressed as [20]

$$
G_{ii}(s) = \frac{U_{dc1} \left( k_{pi1}s + k_{i1}\right)}{L_b s^2 + k_{pi1} U_{dc1} s + k_{i1} U_{dc1}},
$$

where $L_b$ is the inductor of BDDC, $U_{dc1}$ is the rated DC bus voltage of subgrid-1, and $k_{pi1}$ and $k_{i1}$ are the proportional and integral gains of the current loop PI controller, respectively. For the DCMG, the dynamic DC bus voltage in the small signal model can be expressed as

$$
\begin{align*}
\frac{C_1 U_{dc1}^2}{P_t} & \Delta \dot{u}_{dc1} = \Delta P_{pv1} + \Delta P_{b1} - \Delta P_{dc12} - \Delta P_{dc13}, \\
\frac{C_1 U_{dc}^2}{P_t} & \Delta \dot{u}_{dc2} = \Delta P_{pv2} + \Delta P_{b2} + \Delta P_{dc12}, \\
\frac{C_1 U_{dc}^2}{P_t} & \Delta \dot{u}_{dc3} = \Delta P_{pv3} + \Delta P_{b3} + \Delta P_{dc13},
\end{align*}
$$

where $C_i$ (i = 1, 2, 3) represents the DC bus capacitance, and $U_{dc1}$ represents the nominal DC voltages of the subgrid.
From (9) to (11), the dynamic response of DC bus voltage in each subgrid can be expressed as

\[
\Delta u_{dc1} = \frac{\Delta P_{pv1} - \Delta P_{ibcl2} - \Delta P_{ibcl3}}{sK_i - G_{bus}(s)} = G_{p1}(s)(\Delta P_{pv1} - \Delta P_{ibcl2} - \Delta P_{ibcl3}),
\]

\[
\Delta u_{dc2} = \frac{\Delta P_{pv2} + \Delta P_{ibcl2} - \Delta P_{ibcl3}}{sK_i - G_{bus}(s)} = G_{p2}(s)(\Delta P_{pv2} + \Delta P_{ibcl2} - \Delta P_{ibcl3}),
\]

\[
\Delta u_{dc3} = \frac{\Delta P_{pv3} + \Delta P_{ibcl3}}{sK_i - G_{bus}(s)} = G_{p3}(s)(\Delta P_{pv3} + \Delta P_{ibcl3}),
\]

where \( K_i = \left( C_i \cdot U_{dc1} \right)^2 / P_i \). The transfer function \( G_{pi}(s) \) can be used for DC bus voltage droop control analysis in the DC subgrids. From (9), \( G_{bus}(s) \) is expressed as

\[
\Delta P_{ni} = G_{bus}(s)\Delta u_{dc1} = -\left( \frac{K_{pu1} + (K_{iu1}/s)G_{i1}(s)}{P_i/H_{b}} + \Delta u_{dc1}\right)\Delta u_{dc1}.
\]

4.2. Small Signal Model of IBC Controller. The IBC controller regulates the power flow through the IBC from the reference power generated by the IBC secondary controller. Hence, the dynamic analysis of the IBC controller can be carried out from \( \Delta P_{ibc} \) to \( \Delta P_{ibc-ref} \). From the primary loop, the dynamic characteristics of the inner power tracking loop (\( \Delta P_{ibc1j}(s) \)) can be expressed as

\[
\Delta P_{ibc1j}(s) = \frac{U_{dc1j}(k_{ph1j}/s + K_{ibc1j})}{L_{1j}^2s^3 + k_{ph1j}U_{dc1j} + k_{ibc1j}U_{dc1j}}\Delta P_{ref1j}(s),
\]

where \( j = 2, 3 \), \( L_{1j} \) is the inductor of IBC, and \( T \) is the time delay for IBC reference power generation. From (14), any change in power reference will be observed in the dynamics of the IBC output power. For control parameter design, a stability analysis study is carried out in the next section.

4.3. Stability Analysis. The small signal models from (12) to (14) are used for stability analysis. The generic model obtained from the equation can be expressed as
4.3.1. Stability Analysis during NOM. In normal operation mode, the pole-zero locations of the related transfer function from $\Delta P_{\text{ibc13}}$ to $\Delta u_{dc1}$ are shown in Figure 7. By varying the inner loop proportional gain ($k_{pibc13}$) from 0.0001 to 0.0021, with a step of 0.0002, it can be observed that, with the increase in gain value, the system moves towards the left of the s plane, as shown in Figure 7(a). It shows that the increase in the gain value increases the system stability and dynamics. In this case, the time delay is taken as 1 ms. Further, Figure 7(b) shows the pole-zero location of the related transfer function with the variation of time delay from 0.0001 to 0.0031, with a step of 0.0003. It can be observed that the increase in time delay leads the system towards an unstable region. With the implemented time delay (1 ms), the system remains stable.

4.3.2. Stability Analysis during Outage of Battery Unit. If one of the DC subgrids undergoes an outage of the battery unit, then the voltage regulation of that subgrid is transferred to the corresponding IBC connected to it. The challenge is whether the IBC will support a seamless transition from normal operating mode to voltage regulation mode. To analyze the dynamics in this condition, (12) can be rewritten as

\[
\begin{bmatrix}
\Delta u_{dc1} \\
\Delta u_{dc2} \\
\Delta u_{dc3}
\end{bmatrix} = 
\begin{bmatrix}
G_{p1}(s) & 0 & 0 \\
0 & G_{p1}(s) & 0 \\
0 & 0 & G_{p1}(s)
\end{bmatrix}
\begin{bmatrix}
\Delta P_{pv1} \\
\Delta P_{pv2} \\
\Delta P_{pv3}
\end{bmatrix} + 
\begin{bmatrix}
-G_{p1}(s)G_{ibc12}(s) & -G_{p1}(s)G_{ibc13}(s) & 0 \\
G_{p2}(s)G_{ibc12}(s) & 0 & -G_{p3}(s)G_{ibc13}(s)
\end{bmatrix}
\begin{bmatrix}
\Delta P_{ibc12} \\
\Delta P_{ibc13}
\end{bmatrix},
\]

where $G_{p1}(s) = 1/sK_1$ instead of $1/(sK_1 - G_{ibc1}(s))$. It indicates that the battery in subgrid-1 has undergone an outage. To check the dynamics and stability of the system, the pole-zero analysis of related transfer functions from $\Delta P_{\text{ibc13}}$ to $\Delta u_{dc1}$ is shown in Figure 7(c). It can be observed that, with the increase in proportional gain ($k_{pibc13}$) from 0.0005 to 0.0025, with a step of 0.0002, the system stability increases. Excessive increases in gain lead to a sluggish system. Further, the step response of DCMG to change in power is shown in Figure 7(d). It can be observed that, with an increase in proportional gain ($k_{pibc13}$) from 0.0005 to 0.002, with a step of 0.0005, the time constant and settling time of the step response have reduced. Hence, the response is faster and smoother. From the above analysis, suitable gain values are selected for the PI controllers of DCMG. The design parameters of DCMG are shown in the appendix.

4.4. Sensitivity Analysis. In this section, the sensitivity analysis of the DCMG is performed with the variation of time delay, variation of the inductance of BDDC converter, and increase of droop gain. Figure 7(b) shows the eigenvalues with the variation of time delay. It can be observed that, with an increase in communication time delay, the eigenvalues of the system moved towards the right half of the complex plane. Hence, the system is sensitive to the communication time delay. With a higher value of communication time delay, the DCMG may lose its stability.

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5. Results and Discussion

In the simulation study, three interlinked subgrids are simulated in islanding mode. The single-line diagram of the implemented DCMG is shown in Figure 9. The simulations are carried out with three case studies with a comparative...
analysis of the results for verification of the viability of the proposed strategy. Further, the feasibility of the proposed coordinated strategy is verified in the OPAL-RT OP-4510 real-time digital simulator (RTDS). In normal operating mode, all the subgrids operate with battery units, and PV sources operate at MPPT throughout the case study. For simplicity in coordination control analysis, the PV generations are set to operate at 25°C and 1000 W/m² throughout the simulation. The parameters of subgrid components are manifested in Table 3. The maximum power transfer capacities of IBCs are set at 11 kW. To observe the change in SoC, the battery capacity has taken 10 Ah. For a higher capacity battery, precise observation of the change in SoC will take a longer time. In the implemented DCMG, the LBC has been taken as a dedicated wired communication for the analysis. In all the cases, the IBC power from subgrid-2 to subgrid-1 has been shown as positive, and vice versa. Similarly, the IBC power from subgrid-3 to subgrid-1 has been shown as positive, and vice versa.

5.1. Case 1: SoC Balancing Based Power Sharing. Figure 10 shows the simulation results of DCMG in fast charging and fast discharging mode and in NOM. The load demand in DCMG is shown in Table 4. Subgrid-1 operates in NSM, subgrid-2 operates in LSM, and subgrid-3 operates in HSM. Hence, subgrid-1 operates in NOM, subgrid-2 operates in fast charging mode, and subgrid-3 operates in fast discharging mode.
The DCMG starts its operation with charging mode in subgrid-2 and discharging mode in subgrid-1 and subgrid-3. It can be observed that all the DC bus voltages operate at their nominal value, as shown in Figure 10(a). However, during 12 to 14 s, $V_{dc2}$ operates at 401 V, which is well within the allowable deviation limit [35], and it does not affect the voltage-sensitive loads. The small voltage deviation in subgrid-2 indicates peak charging of BS-2.

It can be noted that the charging power of BS-2 is higher than the battery powers in subgrid-1 and subgrid-3, as shown in Figure 10(a). It indicates that, due to the fast charging operation in subgrid-2, BS-2 takes higher power compared to subgrid-1 and subgrid-3. Similarly, due to HSM in subgrid-3, BS-3 always operates in discharging mode. Compared to NOM, a low SoC battery takes more charging current and lesser load demand with the fast charging mode. Similarly, with the fast discharging mode, a high SoC battery charges at a slower rate and takes more load demand compared to the NOM. It can be seen that, with fast charging mode, the SoC of BS-2 improves 0.5% more compared to NOM. Similarly, with fast discharging mode, the SoC of BS-3 decreases 0.4% more compared to NOM. Hence, with the fast charging factor, the low SoC battery is allowed to operate in fast charging mode. Similarly, a high SoC battery is allowed to operate in slow charging mode. Hence, deep discharge of a low SoC battery is prevented, and overcharge of a high SoC battery is avoided.

Figure 10(b) shows the power flow through the IBCs. To support the change in load demand, the charging power of BS-2 reduces, so the power through IBC12 also increases. It can be observed that, with fast charging and fast discharging mode, the power through IBC13 is unaffected till 10 s as BS-3 operates at constant discharging power. During this period, the IBC31 operates at its full transfer power. Thus, it validates the SoC balancing-based power sharing of IBCs. All the PV generations operate at their peak generation as power demand is greater than the generation, as shown in Figure 10(b).

### Table 3: Components parameters of DCMG.

<table>
<thead>
<tr>
<th>Components</th>
<th>Parameters</th>
<th>Subgrid-1</th>
<th>Subgrid-2</th>
<th>Subgrid-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>PV capacity</td>
<td>@1000 W/m²</td>
<td>5 kW</td>
<td>10.4 kW</td>
<td>10.4 kW</td>
</tr>
<tr>
<td>Load capacity</td>
<td></td>
<td>10 kW</td>
<td>20 kW</td>
<td>20 kW</td>
</tr>
<tr>
<td>Battery</td>
<td>Storage capacity</td>
<td>10 Ah</td>
<td>10 Ah</td>
<td>10 Ah</td>
</tr>
<tr>
<td></td>
<td>Nominal voltage</td>
<td>120 V</td>
<td>240 V</td>
<td>240 V</td>
</tr>
<tr>
<td></td>
<td>Peak charging and discharging power</td>
<td>10 kW</td>
<td>12 kW</td>
<td>12 kW</td>
</tr>
<tr>
<td>Subgrid voltage and parameters</td>
<td>$V_{uc}$</td>
<td>210 V</td>
<td>420 V</td>
<td>420 V</td>
</tr>
<tr>
<td></td>
<td>$V_{nom}$</td>
<td>200 V</td>
<td>400 V</td>
<td>400 V</td>
</tr>
<tr>
<td></td>
<td>$V_{lc}$</td>
<td>190 V</td>
<td>380 V</td>
<td>380 V</td>
</tr>
<tr>
<td></td>
<td>SoC$_{u}$</td>
<td>90%</td>
<td>90%</td>
<td>90%</td>
</tr>
<tr>
<td></td>
<td>SoC$_{c}$</td>
<td>30%</td>
<td>30%</td>
<td>30%</td>
</tr>
<tr>
<td></td>
<td>SoC$_{l}$</td>
<td>20%</td>
<td>20%</td>
<td>20%</td>
</tr>
<tr>
<td></td>
<td>$k$</td>
<td>10</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>$\alpha$</td>
<td>0.002 V/W</td>
<td>0.004 V/W</td>
<td>0.004 V/W</td>
</tr>
</tbody>
</table>

The battery in subgrid-3 is tested to verify the plug-and-play capability of the proposed CPMS. The load demands are similar to those of case-1 throughout the simulation.

The DCMG starts its operation with charging mode in subgrid-2 and discharging mode in subgrid-1 and subgrid-3. All the DC bus voltages are maintained at nominal voltages, as shown in Figure 11(a). At $t = 3$ s, the BS-3 is stopped operating to emulate the plug-and-play operation of storage. It can be observed that the IBC secondary controller worked normally and regulated the DC bus voltage of subgrid-3. Further, the transient outage of BS-3 does not drastically affect $V_{dc1}$ and $V_{dc2}$. It indicates that the proposed IBC control has seamlessly transferred from SoC balancing-based power sharing mode to voltage control mode after an outage of the battery terminal without affecting other IBCs. Moreover, after the outage of BS-3, BS-1 and BS-2 are managed to fulfill the load demand and share their power according to their SoC levels, as shown in Figure 11(b). The discharging rate of BS-2 is less than BS-1, which prevents BS-2 from deep discharge and helps enhance its life span. At $t = 11$ s, the BS-3 starts its operation to emulate the plug-and-play process of the battery. It can be observed that, due to the turning on of BS-3, there is a voltage spike in $V_{dc3}$. However, the transient voltage in subgrid-3 is well below its allowable deviation. Further, the turned-on operation of BS-3 does not drastically affect $V_{dc1}$ and $V_{dc2}$. It indicates the plug-and-play features of the CPMS. All the PV generations operate at their peak generation as power demand is greater than the generation, as shown in Figure 11(b).

### 5.3. Case 3: Comparison of the Fuzzy-Based Controller with the Conventional Controller.

Figure 12 shows the performance of DCMG with the fuzzy-based controller and with a conventional controller. All the subgrids are operating in NOM. The performance of the microgrid is investigated with seven load steps. The load demand in DCMG is shown in Table 4.

Figure 12(a) shows that the DC bus voltages are regulated at their nominal value with the fuzzy-based controller and with the conventional controller irrespective of load variation. The fuzzy-based controller has replaced the conventional controller in the secondary IBC controller;
however, the battery controllers operate with the conventional PI controller. The fuzzy-based controller and conventional controller can operate in SoC balancing-based power sharing strategy, as shown in Figures 12(a) and 12(b).

However, it can be observed that, with the fuzzy-based controller, the voltage peak in $V_{dc2}$ and $V_{dc3}$ is lesser than the conventional controller at the time of load switching. It shows the inertia support of the fuzzy-based controller compared to the conventional controller. Hence, it can be observed that the fuzzy logic controller is robust compared to the conventional PI controller.

5.4. Real-Time Digital Simulation Results. The performance of the fuzzy-based power management strategy is validated through OPAL-RT OP-4510 real-time digital simulator, as shown in Figure 13. Two interconnected DC subgrids are implemented on the simulation platform. The capabilities of the fuzzy-based controller are observed in two case studies, that is, NOM in case-1 and fast charging and fast discharging mode in case-2. The load variations in case-1 and case-2 are shown in Table 5. For all the cases, the IBC power flow from subgrid-2 to subgrid-1 has been shown as positive, and vice versa.

![Figure 10: Performance of DCMG with fast charging and fast discharging condition. (a) $V_{dc}$ variations and battery power in three subgrids. (b) Change in SoC, power through IBCs, and PV generations in three subgrids.](image-url)

**Table 4: Load variations on each subgrid.**

<table>
<thead>
<tr>
<th>Time interval (Sec)</th>
<th>1–2</th>
<th>2–4</th>
<th>4–6</th>
<th>6–8</th>
<th>8–10</th>
<th>10–12</th>
<th>12–14</th>
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<tbody>
<tr>
<td>SG1 Load (kW)</td>
<td>9.5</td>
<td>15</td>
<td>20</td>
<td>23</td>
<td>23</td>
<td>15</td>
<td>8</td>
</tr>
<tr>
<td>SG2 Load (kW)</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>SG3 Load (kW)</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>10</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Total Load (kW)</td>
<td>17.5</td>
<td>23</td>
<td>28</td>
<td>31</td>
<td>36</td>
<td>23</td>
<td>16</td>
</tr>
</tbody>
</table>
5.4.1. Case-1: RTDS Results in NOM. Figure 14 shows the performance of DCMG with the proposed fuzzy-based CPMS in NOM. The performance of the DCMG is studied with six load steps. BS-1 is set to operate at 40% of SoC, and BS-2 is set to operate at 70% of SoC. Figure 14(a) shows that both DC bus voltages are regulated at their nominal values throughout the result. During load switching, the DC bus voltages are well within their allowable deviation limits. Hence, the proposed strategy is robust to load variation. It can be observed that the charging power of BS-1 is higher than the charging power of BS-2. Further, from Figure 14(b), it can be observed that the increase in SoC in BS-1 is 0.5% compared to 0.15% in BS-2. It indicates the SoC balancing-based power management performance of the proposed CPMS. During the experiment, all the PV generations operate at maximum power. The power generation of PV-2 is shown in Figure 14(b) for verification.

5.4.2. Case-2: RTDS Results in Fast Charging and Fast Discharging Mode. Figure 15 shows the performance of DCMG with the proposed fuzzy-based CPMS in fast charging and fast discharging mode of operation. BS-1 is set to operate at 25% of SoC, and BS-2 is set to operate at 95% of SoC. The viability of the proposed CPMS is studied with six load steps. Figure 15(a) shows that the DC bus voltages are regulated at their nominal values during the operation. Hence, the change in load does not affect the voltage-sensitive loads. Further, it can be observed that the charging power of BS-1 is higher than the charging power of BS-2.
Figure 12: Performance of DCMG with fuzzy-based controller and conventional controller. (a) $V_{dc}$ variations and battery power in three subgrids. (b) Change in SoC, power through IBCs, and PV generations in three subgrids.

Figure 13: OPAL-RT OP-4510 real-time experiment setup.
Table 5: Load variations on each subgrid.

<table>
<thead>
<tr>
<th>Case</th>
<th>Time interval (Sec)</th>
<th>0–1</th>
<th>1–3</th>
<th>3–5</th>
<th>5–7</th>
<th>7–9</th>
<th>9–10</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SG1 Load (kW)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Case-1</td>
<td>6.5</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>6.5</td>
<td></td>
</tr>
<tr>
<td>Case-2</td>
<td>4</td>
<td>4</td>
<td>6</td>
<td>11</td>
<td>4</td>
<td>4</td>
<td></td>
</tr>
</tbody>
</table>

Table 6: Comparison of proposed CPMS with related strategies.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal voltage regulation</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>IBC controller</td>
<td>PI</td>
<td>Fuzzy</td>
<td>PI</td>
<td>PI</td>
<td>PI</td>
<td>Fuzzy</td>
<td></td>
</tr>
<tr>
<td>SoC balancing-based control</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Fast charging/fast discharging control</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Overcharge and overdischarge regulation</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Control flexibility of battery</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Moreover, BS-1 always operates in charging mode during the experiment, and BS-2 operates in discharging mode. From Figure 15(b), it can be observed that, with fast charging and fast discharging operation, the SoC of BS-1 increases to 25.7%, and the SoC of BS-2 decreases to 94%. Hence, with fast charging and fast discharging factor, the low SoC battery is allowed to operate in fast charging mode. Hence, deep discharge of the low SoC battery is avoided. Similarly, the high SoC battery is allowed to operate in slow charging mode. Hence, overcharging of the high SoC battery is avoided. During the experiment, both the PV generations and telecommunication systems. For more robust control of SoC balancing-based power management and DC bus voltage regulation with an improved transient response, an intelligent algorithm or optimization technique can be implemented with a fuzzy controller in future research.

To validate the effectiveness of the proposed CPMS, a comparative study of the proposed CPMS with related reference strategies is summarized in Table 6. The majority of reference works are utilized PI-based IBC control strategy, while few implemented fuzzy logic controllers. Further, SoC balancing with nominal voltage regulation and overcharging and discharging regulation is not investigated simultaneously in the addressed research works.

6. Conclusion

In this paper, three DC subgrids are interconnected through two interlinking bidirectional converters (IBCs). In each subgrid, the PV source and battery storage are connected to the DC bus. For regulation of DC bus voltage at its nominal value, a secondary controller has been added above the primary controller of each battery controller. Further, a fuzzy-based coordinated power management strategy has been implemented for each secondary IBC controller for SoC balancing-based power sharing among the subgrids. In addition, with the fast charging and fast discharging mode of the proposed strategy, a low SoC battery charges at a faster rate and a high SoC battery discharges at a faster rate to balance the SoC levels. It has been observed that, in fast charging mode, the SoC of a low SoC battery improves more than 0.5% in 14 s compared to the normal operating mode. Similarly, the SoC of a high SoC battery decreases more than 0.4% in 14 s compared to the normal operating mode with the fast discharging mode. Hence, with the proposed strategy, deep discharge of a low SoC battery has been prevented, and overcharge of a high SoC battery has been avoided. Moreover, the proposed strategy can operate with the plug-and-play condition of the battery unit. The proposed strategy does not depend on a central controller, enhancing the reliability of the DC microgrid. The viability of the proposed strategy has been validated through simulation in MATLAB/Simulink and OPAL-RT real-time digital simulator. The proposed strategy can be implemented in remote area DC microgrids interconnections and telecommunication systems. For more robust control of SoC balancing-based power management and DC bus voltage regulation with an improved transient response, an intelligent algorithm or optimization technique can be implemented with a fuzzy controller in future research.

Appendix

A. Subgrid Design Parameters

The subgrid design parameters are as follows:
\[ L_{b1} = 0.6 \text{ mH}, \]
\[ L_{b2} = L_{b3} = 1 \text{ mH}, \]
\[ L_{pv1} = L_{pv2} = L_{pv3} = 8 \text{ mH}, \]
\[ C_1 = C_2 = C_3 = 20 \text{ mF}, \]
\[ u_{b1} = 120 \text{ V}, \]
\[ u_{b2} = u_{b3} = 240 \text{ V}, \]
\[ k_{p1} = k_{p2} = k_{p3} = 4, \]
\[ k_{i1} = k_{i2} = k_{i3} = 30, \]
\[ k_{pu1} = 6, \]
\[ k_{iu1} = 50, \]
\[ k_{pu2} = k_{pu3} = 10, \]
\[ k_{iu2} = k_{iu3} = 50, \]
\[ k_{pi1} = 0.001, \]
\[ k_{ii1} = 1, \]
\[ k_{pi2} = k_{pi3} = 0.001, \]
\[ k_{ii2} = k_{ii3} = 0.5, \]
\[ \text{(A1)} \]

B. IBC Design Parameters

The IBC design parameters are as follows:
\[ L_{12} = L_{13} = 0.5 \text{ mH}, \]
\[ C_{12} = C_{13} = 20 \text{ mF}, \]
\[ k_{pibc12} = k_{pibc13} = 0.001, \]
\[ k_{ibc12} = k_{ibc13} = 0.5 \]
\[ \text{(B1)} \]

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References

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