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Research Article

A New Multifunctional Protection System for Reducing Fault Current, Ferroresonance Overvoltage, and Voltage Fluctuations in Power Networks

Peyman Tanha Bashoo and Mostafa Jazaeri

Department of Electrical and Computer Engineering, Semnan University, Semnan, Iran

Correspondence should be addressed to Mostafa Jazaeri; mjazaeri@semnan.ac.ir

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This paper introduces a multifunctional protective system to mitigate more likely threats in power networks. The proposed device can cope with short circuit current, voltage sag, or swell and dangerous overvoltages due to ferroresonance by elaborate switching in its unified structure. The switching is in fact the main key for playing among the functions and altering the structure. Since the switches receive the control system's commands based on what happens in the network, an intelligent controller has to be designed to interpret four operating modes and activate the correct function. Following the activation command, the structure is customized through switching action and the network is equipped with the corresponding protection function. The proposed scheme by employing minimum components and therefore achieving significant saving in costs can meet all expectations satisfactorily. Moreover, the control system's performance is examined by a set of numerical simulations in a Matlab/Simulink environment. The obtained results show that the proposed device is feasible and successfully performs all three functions independently.

1. Introduction

Today, the widespread use of nonlinear loads has increased the risk of instability and reduced the reliability and quality of power systems [1–3]. One problem with nonlinear loads is the unpredictability of their behavior, which causes the system to experience voltage or current faults. These faults including short circuit current, ferroresonance overvoltage, and voltage sag/swell are the major cause of damage to the consumer and energy producer, which can deteriorate the insulation of the distribution network equipment and the consumer, and also reduce the quality of power supply by voltage drop, voltage rise, or voltage imbalances [4, 5]. Fortunately, these threats are unlikely to occur simultaneously, and it is possible to capture each one independently. Hence, designing a high speed and efficient multifunctional protection scheme with minimum cost and complexity can be a serious challenge, and if such a system is introduced, it has many benefits. On the other hand, the power electronic-based devices have significantly enhanced the capability of protection systems and power system control [6]. High accuracy measurement and control, and high-speed performance are approved features of such devices [7]. Today, with the proposed new methods in digital control and protection areas, the capability of the power system is increased [8]. Now some questions may be raised, for instance, is a high speed multi task protection system with minimum components and cost feasible? or is it possible to decrease the complexity of the design while its efficiency and reliability are kept constant? Many researches have been carried out to give a suitable answer to such questions in the literature.

Dynamic voltage recovery (DVR) is a device that has the ability to manage voltage unbalances, compensate voltage swell/sag, reduce total harmonic distortion (THD) in the load voltage [9–11], correct the power factor, and control the reactive power in the power system [12–16]. On the other

hand, the power system is continuously subject to short circuit currents up to several times of nominal level that pass through the lines and equipment, and impose severe voltage drops to the network [17]. Using power electronic switches, a fault current limiter (FCL) can manage the fault current by injecting a series impedance into the line [18]. However, the FCL is inactive in the normal operation as well as in unbalanced network conditions and does not affect power quality [19]. There are various technologies for using FCL in the power network. Using resistor and inductor in series in the network causes a quick reaction against the fault current [20]. The injection of a controlled resonance impedance, in series or in parallel, can be employed to reduce instantaneous fault currents [21–23]. Although fault current limiting and dynamic voltage recovery are two different functions and are managed independently, several components with some technology can be used to combine them intelligently.

Another nonlinear phenomenon in the network is ferroresonance overvoltage, which can occur between the breaker's capacitor and the voltage transformer [24]. Using a nonlinear load, the magnetic core of the voltage transformer may be saturated and show a completely nonlinear and unpredictable behavior [25]. Ferroresonance overvoltage can overheat the transformer core and burst the surge arresters [26]. Ferroresonance limiter is one of the important functions in the power systems protection that can be a power electronic-based device and limits and even eliminates such overvoltage [27–29]. The number of circuit elements and costs can be reduced by using an integrated structure of protection and power quality functions. In Ref. [30], a dual purpose protective device is introduced to limit the fault current and compensate for the voltage deviations simultaneously by employing 24 power switches to provide two functions. In addition, three switches are used to activate or deactivate the normal mode. Therefore, the proposed device utilizes totally 27 switches that in comparison with competitors with less switches, has higher power losses and costs. A combined structure of a fault current and a ferroresonance limiter with acceptable performance is analyzed in Ref. [31]. But, using thyristors to put the DC capacitor in the correct direction is inappropriate because the power switches do not turn off and on when the ferroresonance phenomenon is resolved. Radmanesh et al. [32] also introduce a dual function protection structure named fault current limiter and ferroresonance overvoltage limiter. The structure consists of an inductor series with a capacitor that introduces a series resonance circuit. In addition, a resistor series with power switches is connected across the capacitor. In the normal state, the switches are open and the series impedance is in resonant mode and hence short-circuited. Following a short circuit, the switches are closed and the series impedance becomes large and limits the short circuit current. Moreover, in order to reduce the ferroresonance overvoltage, the DC capacitor is entered into the network in two half cycles, in the opposite direction of the voltage waveforms, and thus controls the overvoltage. In Ref. [33], a fault current limiter and a ferroresonance overvoltage limiter are placed in the circuit using the DC voltage transient behavior of the network. In this paper, current and voltage faults are limited using a proposed control method. In Ref. [34], the fault current is limited by using a dynamic voltage restorer. In this compensator, when a current fault occurs, a variable series impedance proportional to the current level is injected into the network and when a voltage sag/swell occurs, a controlled series DC capacitor is employed. An interline dynamic voltage restorer for sag mitigation is presented in Ref. [12]. It is made of several dynamic voltage restorers with a common DC link, where each DVR is connected in series with the distribution feeder. A bridge-type FCL-DVR structure is introduced in Ref. [35]. The bridge activates a DC capacitive circuit for voltage sag in the DVR-mode or a DC inductive circuit for a short circuit current in the FCL mode through using switching strategies. However, two serious concerns with such dual function protective systems are converter oversizing and high DC link voltage. In Ref. [36] a LC filter coupled with series coupled capacitor at the AC side is employed to optimize the capacity of the key components. These concerns may be evaluated from loss and cost viewpoints. Hence, lower loss and cost can be two important issues that Ref. [37] tries to give a solution for them by introducing a topology with reduced number of switches, gate drive, and control circuit components. Ref. [38] introduces a commercial multiprotection instrument to protect overhead transmission lines and underground cables. Although it provides several protection functions, they are related to short circuit and over/under voltage protections in the lines and unable to limit or compensate events.

This paper introduces a structure of a unified multifunctional protective system that can cope with power quality pollution, manage heavy short-circuit currents, and limit ferroresonance overvoltage. To achieve these goals, Section 2 presents the limiting and compensating of the physical structure and then introduces four operating modes, including normal operation, dynamic voltage compensation, fault current reduction, and ferroresonance limiting. In the third section, the mathematical relationships, and in Section 4, the conceptual control schemes are described. In Section 5, the performance of the proposed structure is examined by simulation results in Matlab/Simulink environment. Section 6 deals with the prototype model. Finally, Section 7 concludes the paper.

2. Proposed Structure

A typical distribution network equipped with the proposed model is shown in Figure 1. In the figure, the upstream network is modeled by the Thevenin equivalent circuit seen from the load bus with a voltage source (E_s) in series with an impedance (Z_s). In addition, the load is assumed as a constant impedance which can be represented by $Z_L = R_L + \mathrm{j}X_L$.

In the proposed structure and in order to facilitate a bidirectional power flow in the design range, two isolated transformers with turn ratio 1 : 1 in per unit (pu) are used. The lack of electrical connection between the primary and secondary sides, causes ground separation on both sides of the transformer and also independent measurement of

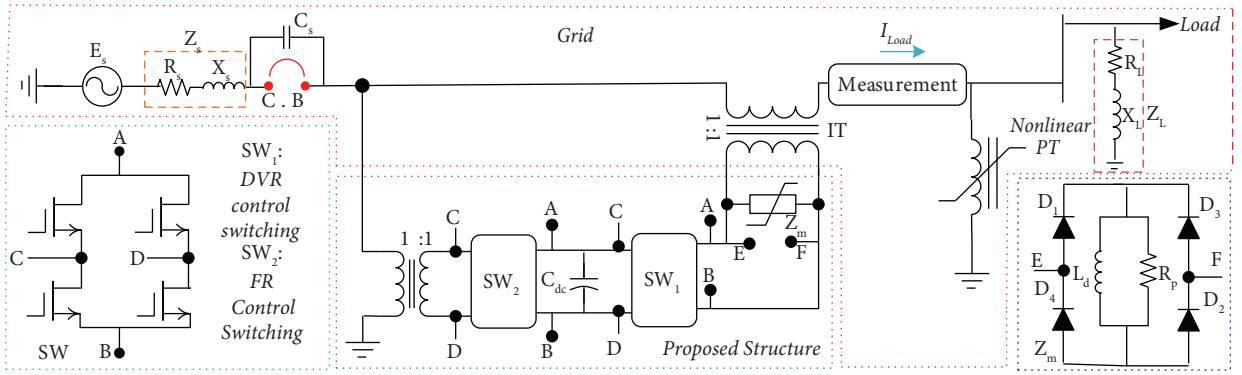


Figure 1: Schematic of the study network equipped with the proposed multifunctional protection device.

quantities are facilitated. In this model, eight switches ($T_1 - T_8$) embedded into SW_1 and SW_2 can be of the IGBT type, so that the circuit can simultaneously enjoy the advantages of high switching frequency at high power. Thus, in the unified structure, 24 power switches are totally employed in three phases that provide all triple functions satisfactorily, while Ref. [30] uses 27 switches for two functions.

2.1. Operation Modes. Due to the multifunctionality of the proposed protective structure, all working situations can be considered in four different operating modes as follows:

(i) Prevalent working conditions in which the network is often operated in such a state (normal mode)

(ii) Conditions due to which the voltage in the network increases or decreases for some reasons (DVR mode)

(iii) Short circuit current limitation by entering series impedance (FCL mode)

(iv) Limiting the overvoltage caused by ferroresonance phenomenon (FRL mode)

In the following, the above operating modes are described.

2.1.1. Normal Mode. In this case, the proposed multifunctional device does not affect the normal operation of the network. The circuit diagram of this state is shown in Figure 2. In this mode, the proposed structure is modeled using an inductor (L_d), resistor (R_p), and diode bridge ($D_1 - D_4$). Also, in this case, all switches ($T_1 - T_4$) are inactive (turn off). Switches ($T_5 - T_8$) are activated via the proposed capacitor charge control system (C_{dc}). The DC link capacitor (C_{dc}) does not affect the network performance while it is in charging status.

According to Figures 2(a) and 2(b) when the network does not encounter voltage and/or current faults on the consumer side, the proposed model controls the network fault in the positive and negative half cycles. As shown in Figures 2(c) and 2(d), because there are no changes in the current and voltage, the inductor (L_d) is a short circuit so that the resistance (R_p) does not affect the network performance. In this case, the power system operates normally without voltage and current faults (changes in current and voltage are almost zero). In this regard, the control system measures the DC link voltage and charges the capacitor using the positive and negative cycles of the network to react to a voltage sag/swell. In fact, according to Figure 2(a), if the network is in a negative half cycle, the control system places the capacitor (C_{dc}) parallel to the network by activating the transistors (T_7-T_8), and if the network is in a positive cycle, according to Figure 2(b), the control system charges the capacitor by activating the transistors (T_5–T_6). In addition, if the control system detects that the DC link is fully charged, it will disconnect all power switches ($T_5 - T_8$). Figures 2(c) and 2(d) show the magnitude of the voltage and current of the series inductor proposed in Figures 2(a) and 2(b). In addition, the series inductor is short-circuited when the network is in the normal operation. On the other side, when the network experiences a voltage or current fault, the voltage and current of the inductor is also changed to react correspondingly.

The meaning of current fault is a typical short circuit current drawn from the network while a severe short circuit has occurred. This paper does not consider other types of current faults like an open circuit.

2.1.2. Dynamic Voltage Compensation Mode. The main task of the compensator in this mode is to maintain the voltage amplitude against all kinds of network events that can lead to voltage sag or swell at the load bus. The meaning of voltage fault is both voltage sag and/or voltage swell. Other types of voltage disturbances are not considered. When a voltage sag or swell is observed, the compensator is put into the network quickly and in proportion to the size of the voltage deviation, and by using the appropriate combination to operate in this mode, tries to limit and compensate for the voltage faults. In this model, a diode bridge ($D_1 - D_4$) is used to control the inductor polarities (L_d), and a transistor bridge is used to place the polarities of the capacitor or voltage source correctly. Figure 3 shows the proposed structure of the voltage fault compensator in this mode.

In order to limit the voltage sag/swell, a voltage source is needed to be able to store or generate electrical energy that the capacitor (C_{dc}) is used for this purpose. The capacitor (C_{dc}) is placed in series in both the drop and rise voltage

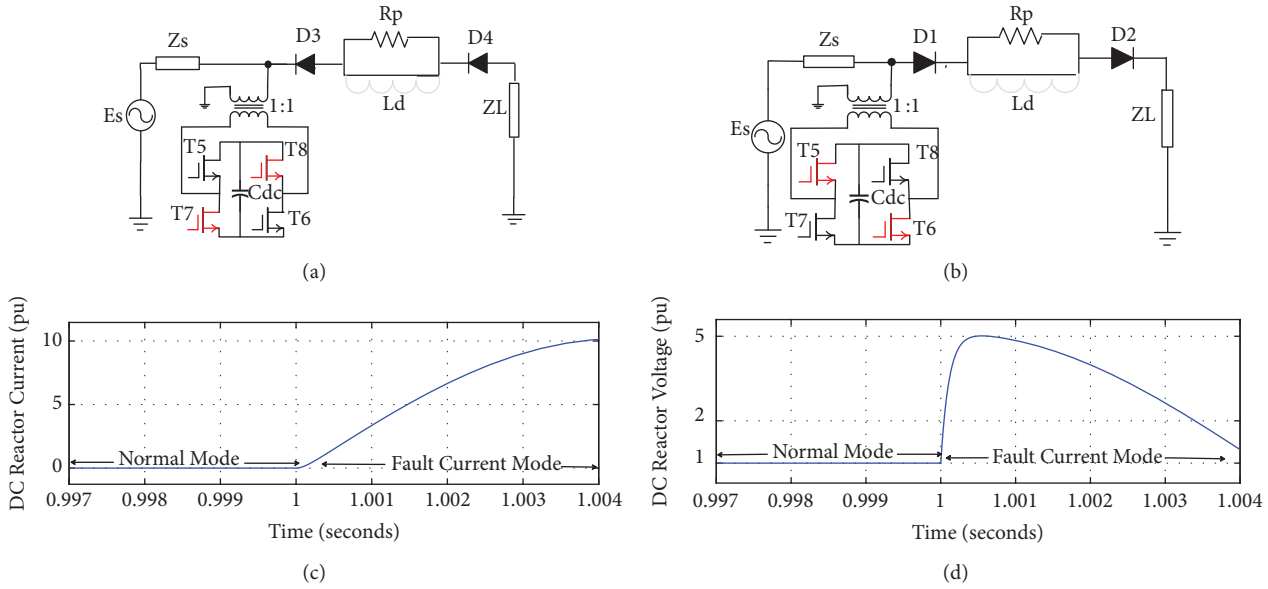


FIGURE 2: Schematic of the proposed structure in normal mode. (a) Negative cycle (inductor (L_d) is a short circuit). (b) Positive cycle (inductor (L_d) is a short circuit). (c) Inductor (L_d) current in normal and fault current modes (d) Inductor (L_d) voltage in normal and fault current modes.

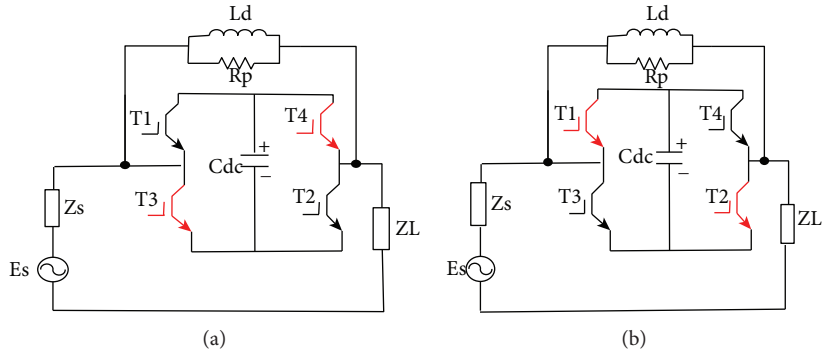


FIGURE 3: Circuit diagram of the proposed structure in the voltage fault compensation mode. (a) For negative half cycles. (b) For positive half-cycles.

modes, and the control system regulates its charge or discharge rate. In addition, the capacitor is charged and discharged through the energy exchange with the network, and thus counteracts the voltage rise or drop. If the grid is exposed to a voltage surge, the capacitor (C_{dc}) is entered to the circuit in series with opposite polarities to the voltage source (Figure 3(a)) and when a voltage drop is occurred with a polarity corresponding to the voltage source (Figure 3(b)). The positive and/or negative polarities are identified and measured by cycles of the network voltage waveform. Inserting a capacitor (C_{dc}) with opposite polarity to the network means that when the network voltage is in the positive half cycle, the negative polarity of the capacitor (C_{dc}) moves to the voltage source, as shown in Figure 3(a). If it is agreeing with the polarity of the network according to Figure 3(b), the positive polarity of the capacitor (C_{dc}) is towards the voltage source. The capacitor's polarity can be easily changed by using a transistor bridge ($T_1 - T_4$). Transistors T_1 and T_2 for positive half cycles and transistors T_3 and T_4 for negative half cycles are activated to place the capacitor in the circuit with network-agreeing polarities. On the other hand, transistors T_1 and T_2 for negative half cycles and transistors T_3 and T_4 for positive half cycles are switched to place the capacitor with opposite polarity. In this circuit, transistors ($T_5 - T_8$) remain inactive in both positive and negative half cycles of the voltage waveform.

According to Figure 3, and following a voltage fault in the network, the line current is changed and the inductor (L_d) gets out from short circuit status and injects a reactance to the circuit proportional to the frequency and current ripple in the diode bridge. In fact, in this case, if the resistor R_p and the inductor L_d are parallel to the network, the voltage sag/swell are effectively damped. The proposed model actually consists of two parts: controlled and self-controlled. In the first part, the series impedance acts as self-control, and in the second part, the voltage source or

capacitor (C_{dc}) is placed in series in the network, which is used to place its polarities using the proposed new control system. In general, the proposed model works so that a variable series impedance is entered into the network when a voltage disturbance occurs, and according to the current, it changes its value. Then, a capacitor (C_{dc}), as a source of generating/absorbing electrical energy which is controlled by a transistor bridge, is put into the network. As shown in Figures 3(a) and 3(b), using the proposed control system, its polarity is controlled to improve the system's performance from the viewpoint of voltage. Charging and discharging the DC link can be done by proper and timely reactions of the control system. In fact, when the network experiences a voltage swell, the capacitor (C_{dc}) in the charge state acts in accordance with the network half cycles. On the other hand, if the network is faced with a voltage sag, the DC link capacitor will act according to the network half cycles in the discharge state. Moreover, when the capacitor is fully charged, the control system returns the excess voltage from the voltage swell to the power system opposite to the network cycles.

2.1.3. Fault Current Limiter Mode. When a short circuit fault occurs in the network, a heavy current is drawn from the power supplies, and if the current is not limited at the shortest time possible, it can cause serious damage to the network equipment and consumers. In such a situation, the FCL mode is quickly activated, and a series impedance proportional to the current deviation from the rated current is injected to the line. Figure 4 shows the network with the proposed model when subjected to a short circuit fault. In this mode, according to Figures 2(c) and 2(d), the inductor L_d comes out from the short-circuit state and injects a large series impedance into the network, causing the dangerous short-circuit current to a value corresponding to the impedance. In this mode, the diode bridge ($D_1 - D_4$) and the impedance (L_d and R_p) are used.

The fault current limiter is actually a structure that changes its output impedance in proportion to the network performance against heavy short circuit currents. In general, the function of the proposed FCL is that when a short circuit current occurs in the network , according to Figures 2(c) and 2(d), both voltage and current are changed which leads to get out of the inductor from short circuit condition. However, the above model is out of normal operation and in the positive and negative half cycles according to Figure 4, it inserts an impedance in proportion to the current fault level. Furthermore, the impedance of (L_d) is proportional to the changes in the network frequency and ripple current (i_{ripple}) in the diode bridge. The value of (L_d) can vary between the nominal and zero.

2.1.4. Ferroresonance Overvoltage Limiter Mode. When a ferroresonance overvoltage phenomena has occurred in the network, the proposed structure quickly goes out of normal operation and the ferroresonance overvoltage limiter mode is activated. This operation mode is shown in Figure 5. According to the figure, in this mode of operation, a single transformer is used to insert the capacitor (C_{dc}) as an impedance parallel to the network. The transistor bridge ($T_5 - T_8$) is also used to control the capacitor's polarity. Moreover, the diode bridge ($D_1 - D_4$) is used to control the direction of the inductor polarity. This inductor acts as a series impedance and reduces the ferroresonance current.

In fact, in this operating mode, the capacitor (C_{dc}) is put in the circuit such that its voltage is in opposite polarity respect to the network voltage half-cycles (positive or negative) as shown Figure 5. In addition, the series impedance ($R_p \| j\omega L_d$) is entered into the network to reduce and control the ferroresonance current. In this condition, transistors ($T_1 - T_4$) are inactivated.

In this operating mode, the proposed model reacts against the overvoltage through two different mechanisms, entering the series impedance (Z_m) into the network and switching the transistor bridge. The latter puts the DC capacitor in the circuit in opposite polarity with respect to the network voltage waveform, in positive and negative half cycles (see Figure 5). Table 1 summarizes the status of transistors ($T_1 - T_8$), diodes ($D_1 - D_4$), inductor L_d, capacitor C_{dc}, and resistor R_p in all four operating modes.

3. Mathematical Description

This section presents the mathematical relationships governing the performance of the proposed multifunctional protection device. In circuit modeling, the upstream network seen from the load bus is represented by a synchronous voltage source (E_S) series with an impedance (Z_S). The load impedance is also denoted by Z_L. In addition, fault or disturbance that can be modeled according to the circumstances of the event is also given in each mode.

3.1. Dynamic Voltage Compensation Mode. One of the functions of the proposed protection device is to compensate and amend the voltage profile in order to improve the voltage quality in the network. Therefore, the output of this compensator must be changed in such a way that the network quantities are maintained and controlled within the allowable range. In the proposed compensator, the power flow control is affected by the direct control of the voltage.

It is assumed that the source of voltage disturbances is on the consumer or load side hence the proposed compensator is installed in the load bus. In fact, following a voltage disturbance, the control system identifies the type and size of the fault. Then, this mode of operation is activated to amend the system's operation and prevents propagating the pollution to other load buses.

As shown in Figure 6, when a voltage disturbance occurs, the compensator acts like a dependent voltage source whose voltage is a function of the system impedance Z_s and the load impedance Z_L. This dependent voltage source in the range of zero to E_S can exchange active and/or reactive powers with the network and isolate the load side from the upstream network. The maximum value of this dependent source is determined based on the degree of voltage sag and swell V_L. K is the ratio of load impedance size to the network

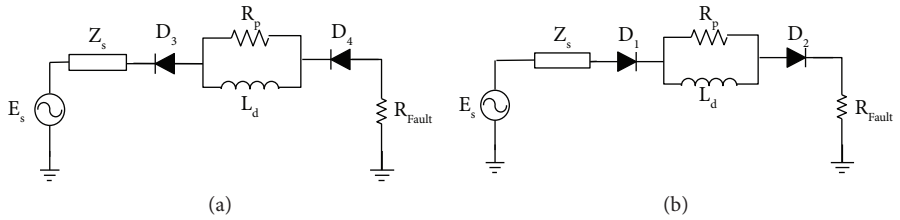


Figure 4: Schematic of the model for FCL mode. (a) Positive half cycle. (b) Negative half cycle.

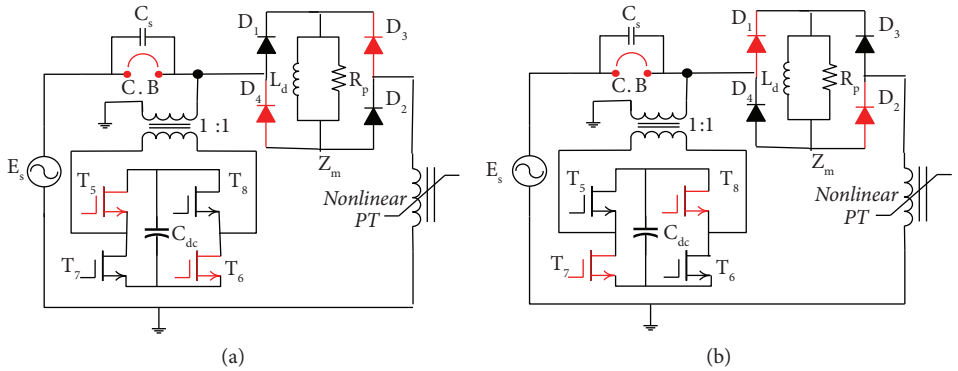


Figure 5: Schematic of the proposed model in Ferroresonance overvoltage mode for (a) positive half-cycles and (b) negative half-cycles.

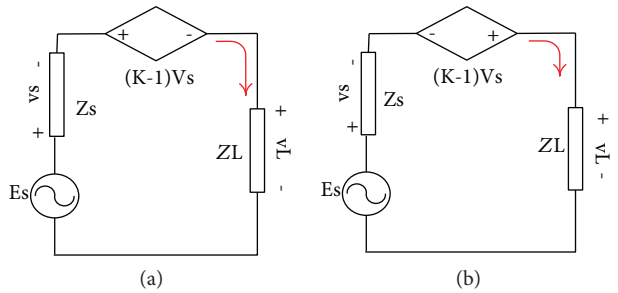


Figure 6: Equivalent circuit of voltage fault compensator. (a) Active and reactive power absorption mode. (b) Active and reactive power injection mode.

Table 1: Status of the elements used in the proposed model in different operating modes.

	D_1	D_2	D_3	D_4	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	C_{dc}	L_d	R_p
Normal	✓	✓	✓	✓	✗	✗	✗	✗	✓	✓	✓	✓	✓	✓	✗
FCL	✓	✓	✓	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗	✓	✓
DVR	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
FRL	✓	✓	✓	✓	✗	✗	✗	✗	✓	✓	✓	✓	✓	✓	✓

impedance ($K = |Z_L/Z_S|$&$0 < K < 2$). The voltage disturbance is also determined by the amount of deviation K from 1. For instance, if $Z_L > Z_S$, then K will be greater than 1 and the control system recognizes a voltage swell. Subsequently by using Table 1, it gives the command to activate the compensation. In this case, the DC capacitor is inserted into the circuit in the reverse polarity to compensate for the load bus voltage fluctuations. The amount of the active and reactive powers absorbed or injected by the voltage compensator for a maximum of one minute depends on the amplitude of E_s [39]. In fact, the capacitor (C_{dc}) acts as a dependent voltage source that corrects the voltage disturbances, as shown by Figure 6. When the compensator is used as a voltage swell compensator, the circuit shown by Figure 6(a) is applied. By using Kirchhoff's voltage law and considering Figure 6(a), equation (1) can be written as:

$$-E_s + V_s + (K-1)V_s + V_L = 0. \quad (1)$$

K can be calculated from equation (1) as follows:

$$K = \frac{E_S - V_L}{V_s}. \quad (2)$$

On the other hand, according to Figure 6(b), equation (3) can be derived:

$$-E_s + V_s - (K-1)V_s + V_L = 0. \tag{3}$$

The value of K according to Figure 6(b), when the voltage compensator is in the active or reactive power absorption or injected state, can be obtained by:

$$K = \frac{V_L + 2V_s - E_s}{V_s}. \tag{4}$$

3.2. Fault Current Limiter Mode. The equivalent circuit of the proposed protection system under fault current limiting mode is shown in Figure 7.

In the proposed model, the constraint is imposed in both positive and negative half cycles. Moreover, a very small fault resistance is chosen to flow a heavy short circuit current through the line. By applying KVL in Figure 7, the following equation can be derived:

$$-E_s + Z_s I_f + \frac{R_p j\omega L_d}{R_p + j\omega L_d} I_f + R_{fault} I_f = 0. \tag{5}$$

Then, the fault current can be determined from equation (6):

$$I_f = \frac{E_s\left(R_p + j\omega L_d\right)}{R_p\left(Z_s + R_{fault}\right) + j\omega L_d\left(Z_s + R_{fault} + 1\right)}. \tag{6}$$

According to equation (6), the larger the impedance L_d, the smaller the amount of the current. It can also be concluded that it is necessary to limit the fault current by the resistor. When a short circuit occurs in the network, the fault current limiter injects a suitable impedance and reduces the short-circuit current level to the maximum current ($i_{\max}$) passing through the inductor in the normal mode. This injected impedance consists of two parts, L_d and R_p. The size of the L_d inductor will be obtained by equation (10) through solving equation (7) as well as assuming equations (8) and (9) in the charge and discharge modes, respectively.

$$i_{DC} = i_{\max} - i_{ripple}, \tag{7}$$

$$i_{ripple} = \left(1 - \left(\frac{R_p}{L_d}\right)(\Delta T)\right) i_{\max}, \tag{8}$$

$$\Delta T = t_2 - t_1 = \frac{T}{2} = \frac{1}{2f}, \tag{9}$$

$$L_d = \frac{R_p i_{\max}}{2 i_{DC} f}. \tag{10}$$

The current ripple (i_{ripple}) oscillates between t_1 and t_2, where t_1 is the start time of the inductor charging (L_d) and t_2 is the start time of discharging.

(i) i_{ripple}: current ripple in charging and discharging mode

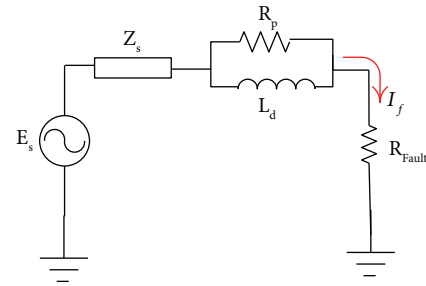


Figure 7: Equivalent circuit of the fault current limiter.

(ii) i_{DC}: direct current in diode bridge

(iii) $i_{\max}$: the maximum current flowing through the inductor in normal mode

According to equation (10), the value of resistance R_p is directly related to the value of L_d.

3.3. Ferroresonance Overvoltage Limiter Mode. The phenomenon of ferroresonance in power transformers can occur following the saturation of its core. In such cases, the appearance of unacceptable overvoltages can damage and outage the network equipment. From this point of view, the overvoltage limiter can be considered as a protective device. Figure 8 shows the equivalent circuit of a power transformer [28, 31, 40] along with the proposed model when the ferroresonance phenomenon occurs.

As per the figure, the core of the power transformer acts as a completely nonlinear inductor and is modeled with a parallel resistor with a very small value that lets to flow nonlinear currents. Now, the proposed device employs a series variable impedance to limit or eliminate ferroresonance overvoltage. Furthermore, in the proposed transformer model, according to Ref. [40], a parallel capacitor (C_{sh}) is used to model the capacities equivalent of the network (capacitive banks, cable capacities, etc.). In addition, a series capacitor (C_s) is employed to provide conditions for the occurrence of ferroresonance phenomenon. In order to investigate the proposed circuit from this viewpoint, the following relations can be considered:

$$\begin{aligned}
\lambda &= N\varphi, \\
v_T &= \frac{d\lambda}{dt}, \\
i_l &= a\lambda + b\lambda^q, \\
E_s &= \sqrt{2}E \sin \omega t, \\
\frac{d\lambda}{dt}(0) &= \sqrt{2} \,\&\, \lambda(0) = 0, \\
Z_T &= \frac{R_p L_d \left(R + L_{trans}\right) + R L_{trans}\left(R_p + L_d\right)}{\left(R_p + L_d\right) + \left(R + L_{trans}\right)}.
\end{aligned} \tag{11}$$

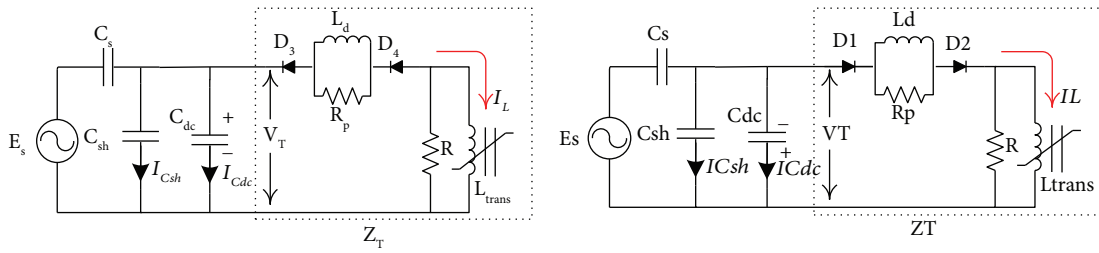


FIGURE 8: Schematic of the proposed device in Ferroresonance mode (a) in negative half cycles and (b) in positive half-cycles.

where N stands for the turns ratio, φ is the amount of the flux, IL is the amount of ferroresonance current, a and b are constant, q is a number that causes the amount of ferroresonance current to be nonlinear and varies between 2 and 13 [31]. By applying KCL in Figure 8:

$$\mathbf{C_S}\frac{\mathbf{d}\left(\mathbf{E_s}-\mathbf{V_T}\right)}{\mathbf{dt}}=\left(\mathbf{C_{sh}}+\mathbf{C_{dc}}\right)\frac{\mathbf{dV_T}}{\mathbf{dt}}+\frac{\mathbf{V_T}}{\mathbf{Z_T}}. \tag{12}$$

The following equation can also compute the system voltage:

$$\sqrt{2}E\cos\omega t=\frac{\mathrm{d}^2\lambda}{\mathrm{d}t^2}\left(\frac{C_s+C_{sh}-C_{dc}}{C_s}\right)+\frac{1}{C_sZ_T}\frac{\mathrm{d}\lambda}{\mathrm{d}t}. \tag{13}$$

According to equation (13), when the series impedance (resistance R_p parallel with inductor L_d) and the DC link capacitor with reverse polarity with the network voltage are put in the circuit, the network voltage is limited to an acceptable value.

4. Control System Design

The task of the control system can be divided into two independent stages; function activation control or master part and function control or slave part. The master part, as Figure 9 illustrates, consists of three important units: sampling and data processing (measurement), feature extraction and mode determination (mode selection), and function activation (function selection). Once one function is activated, the master part is blocked and the slave part operates to put the relevant function control into the circuit. On the other hand, since the duration and magnitude of variables following these function activation are different, a single control scheme cannot cope with these three faults. Three particular control schemes should be designed named; DVR, FCL, and FRL control systems. It should be noted that these control systems have no chance to operate simultaneously.

Moreover, although some suitable control schemes are available in the literature, the control systems presented here are designed conceptually to offer more flexibility to adopt different control strategies.

4.1. Function Activation Control Scheme. Figure 9 illustrates the conceptual control structure of the proposed multifunctional protection device, which consists of three units: measurement, operating mode determination, and control function selection and activation.

In the measurement unit and using Ref. [39], data from the network are collected and then processed to extract the main feature of the signals. The waveforms of the bus voltage and the line current are filtered by BPF to eliminate the extra nose, then rectified to extract the positive and the negative half cycles, and then sampling is carried out at a rate of 1 KHz. The optimum sampling rate depends on the maximum frequency component. The bus voltage and/or the line current is compared with its reference value ($\mathbf{V_{ref}}, \mathbf{I_{ref}}$) to form the deviation of X in Table 2. The reference values are assumed to be 1 per unit based on the rated values.

Based on the extracted features along with the prespecified priorities according to Table 1 and also the measures made according to Table 2, the correct mode can be recognized in the mode selector unit.

On the other hand, the control system must be designed to offer minimum time to respond to the system faults. Hence, both negative and positive half cycles need to be captured and analyzed. To achieve such a requirement, both half cycles of the voltage and current waveforms of the network are employed and if any fault occurs, the control system responds at less than half cycle whether in positive or in negative polarities. This means that the control system is alert and ready to operate at the minimum possible time in the measurement unit. However, to have a satisfactorily control scheme, two other units must also employ suitable control strategies and intelligent and efficient algorithms.

In the next step, measured signals are inserted into the function selection unit to activate the corresponding function according to Table 3 and block other functions. The mode determination unit is in fact an interpreter that intelligently determines fault type, separates it, and provides the necessary commands for the next unit.

The output of the measurement unit according to Table 2 generates three indicators 0, 1, and 2. In proportion to this indicator, the type of fault can be identified in the interpreter and then necessary switching is performed to form the appropriate topology and put it in the circuit.

Furthermore, it is necessary to know which half cycle (positive/negative) of the network voltage we are in. It must also be noted that as soon as one function is activated, the other functions are deactivated and it is not possible to reidentify any fault until it is fixed and the protection system is

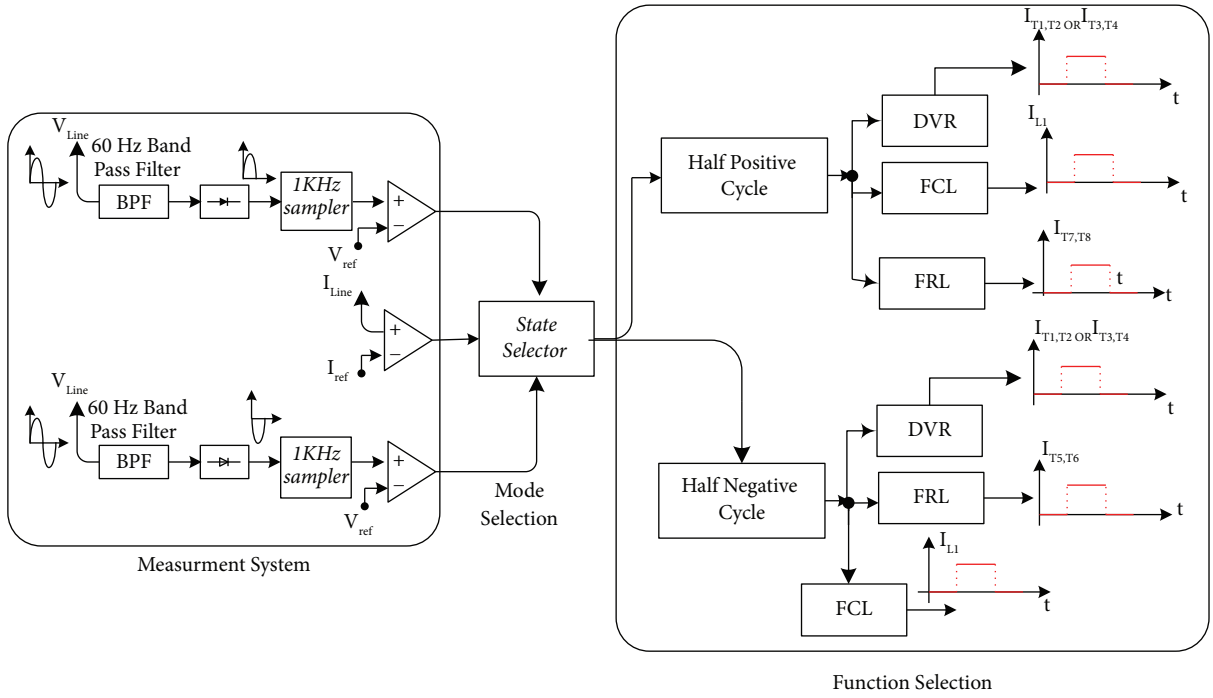


Figure 9: Conceptual structure of the control system.

Table 2: Measurement and detection the type of occurred fault.

Ref X	$-2 < X < -0.1 + 0.1 < X < +2$	$X > -0.1$ $X < +0.1$	$X < -2$ $X > +2$
Voltage (V)	1	0	2
Current (A)	1	0	2

Table 3: Selection of the protective topology based on the measured signals.

Mode state	Voltage			Current		
	$\mathbf{X_v} = 0$	$\mathbf{X_v} = 1$	$\mathbf{X_v} = 2$	$\mathbf{X_c} = 0$	$\mathbf{X_c} = 1$	$\mathbf{X_c} = 2$
Fault current limiter	✗	✓	✗	✗	✗	✓
Dynamic voltage compensator	✗	✓	✗	✗	✓	✗
Ferroresonance limiter	✗	✗	✓	✗	✓✗	✓✗
Normal mode	✓	✗	✗	✓	✗	✗

✓✗: It may or may not include ✓: Only includes ✗: Does not include.

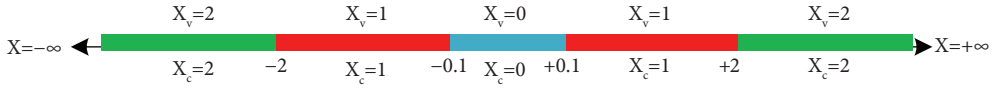
reset to the normal mode. Therefore, although sampling is done permanently and continuously, the control system does not use these samples as long as one function is active.

Figure 10 shows the activation and selection diagram of all functions of the proposed device according to Tables 1–3. By measuring the current and voltage, the value of X are generated according to Table 2. Then, the proper function is activated based on Table 3.

In order to give a comprehensive picture of all tasks, including the power circuit (protective structure) and the control system, a flowchart is arranged to provide a better understanding the relationships, as shown in Figure 11.

In addition, as the flowchart illustrates, the sampling and measurement are continuously carried out for two independent processes: (1) fault detection and function activation, and (2) after activating one function, putting the DC capacitor with correct polarity in the circuit in both DVR and FRL operating modes. Therefore, the control system shown in Figure 9 is initiated once either in positive or negative half cycles.

4.2. Fault Current Limiter Control Scheme. The control of this part is in fact performed automatically. It means that the control scheme uses half cycles of voltage and current waveforms of the network. If the network encounters an increase in the current, L_d enters into the network immediately and limits or modifies the fault current according to the error (Figure 4). The error is defined as a deviation of the fault current measured from its reference ($I_{ref.}$). It is interesting to note that such a limiting mechanism does contribute very well in other modes of operation, i.e.,



X_c: current information, generated by Table (2)
X_v: voltage information, generated by Table (2)

Figure 10: Measurement and detection of the type of occurred fault.

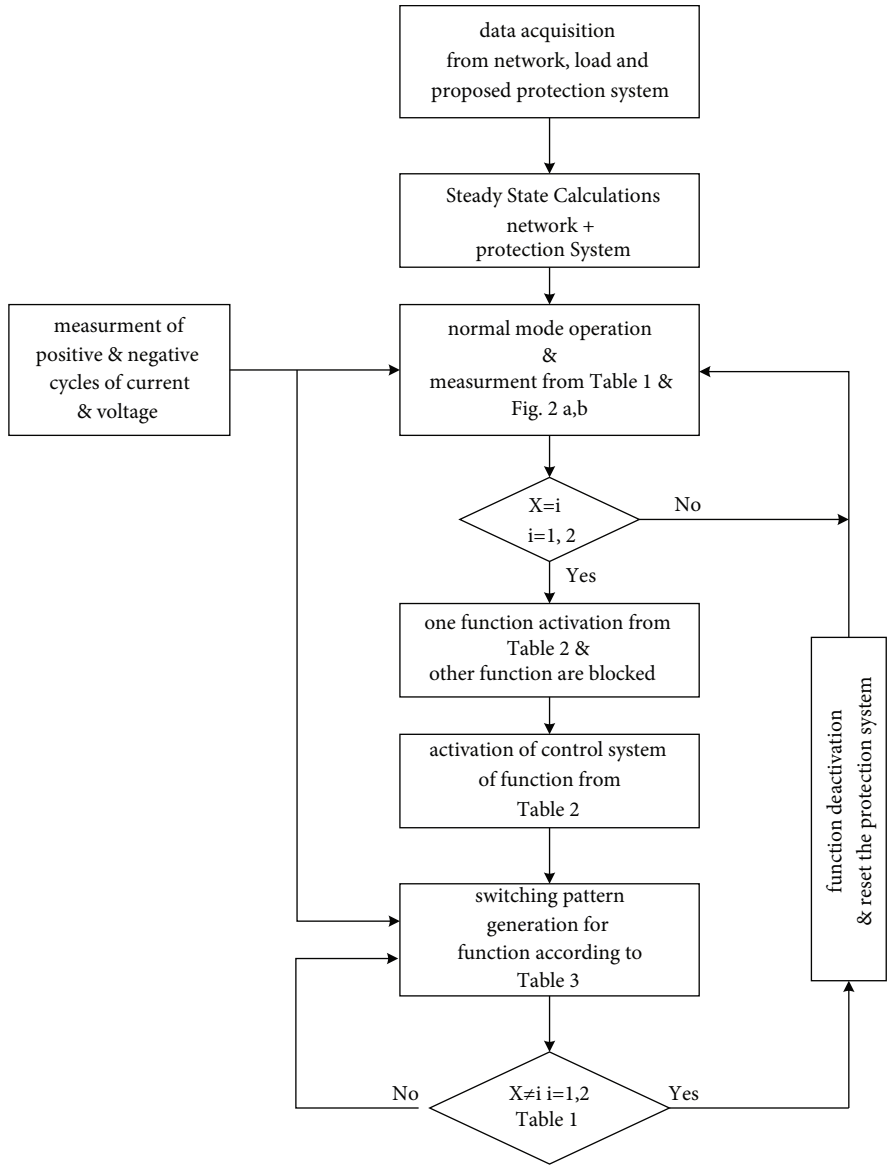


Figure 11: Flowchart of the different steps of the work.

ferroresonance overvoltage limiter and voltage sag/swell compensation, which can be considered a new idea. On the other hand, the circuit shown in Figure 4 automatically operates in all three modes in proportion to the current deviations and offers a suitable reaction.

Based on the above explanations, the current limiting in this operating mode is done naturally. However, to illustrate the idea behind the current limiting, a conceptual control scheme is given in Figure 12.

4.3. Dynamic Voltage Compensator Control. Figure 13 shows the conceptual control system for overvoltage (due to voltage swell) limiting and voltage sag (or dip) compensation.

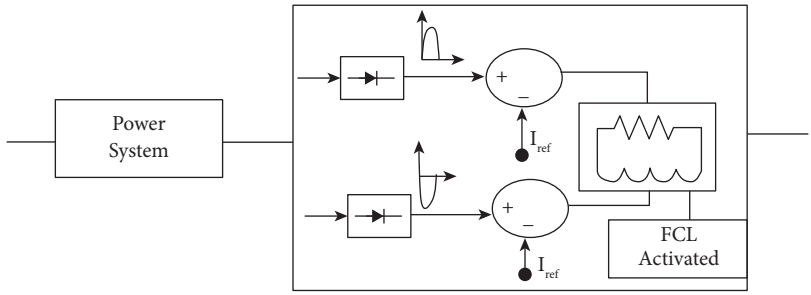


Figure 12: Conceptual control design for the fault current limiter.

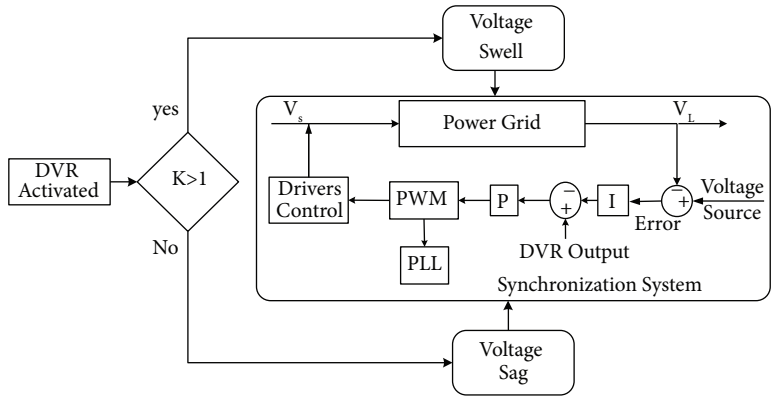


Figure 13: Conceptual control diagram for voltage sag/swell compensator.

In Figure 13, the voltage deviation VS from VL is first calculated. If this deviation is larger than a prespecified threshold, transistors (T_1, $T_2 - T_3$, T_4) are switched on and the DC link capacitor is entered into the circuit in phase with the network voltage polarity. Now the DC link is placed in the same or in the opposite direction of the voltage polarity to charge or discharge, respectively. An integral block is also used, because the output of the control system is affected by faults that have happened in the past. So long as the error is not zero, the output signal is changed to force the error to become zero, and when the error becomes zero, the output is fixed at a constant value. In addition, the output of the voltage source converter must be synchronized with the network by employing a phase lock loop (PLL) unit. Then, the difference between the output of the integral controller and the converter's output voltage is calculated. A proportional control block is then used to improve the voltage synchronization because one of the main features of this control block is the accuracy in disconnecting and connecting two-state processes [40]. The precision and sensitivity of the process control can be enhanced by intelligently adjusting the gains of the controllers. The corresponding gain (K) is calculated from equation (2). The output is applied to the PWM module, which generates voltage converter switching pulses.

It must be noticed that the voltage sag/swell is detected based on a ratio of the network and the load impedances that can be considered as a proposed index. This index can also be used to form the firing pulses of the power electronic switches.

4.4. Ferroresonance Overvoltage Limiter Control Scheme. Following a ferroresonance phenomenon in the network, overvoltage and overcurrent faults occur simultaneously. Hence, both the fault current limiter and the DC link voltage in antiphase with the system voltage according to Figure 5 must be activated by the appropriate action of the control system. Therefore, the control scheme's key task is changing the DC capacitor's polarity by switching (T_5, $T_6 - T_7$, T_8) sequentially. Changing the polarity of the DC capacitor opposite to the positive and negative half cycles of the network voltage can alleviate the ferroresonance phenomenon and limit the overvoltage. As previously explained, the control inputs are the network voltage and the chaos current, which are provided by the measurement unit and also the fault detection system.

It is interesting to know that the DC link capacitor is used with the aim of voltage compensation (Figure 3) and Ferroresonance overvoltage limiter (Figure 5). If the capacitor is entered in the network with incorrect polarity and value, it can intensify the fault.

One of the advantages of this limiter is the use of a series impedance (including a resistor series with an inductor) along with a DC capacitor with a reverse polarity that reacts in the face of ferroresonance overvoltage. Using such a series impedance can limit fault and be recognized as one of the best ways to place the elements in the network. Figure 14 shows the conceptual control scheme when the FRL mode is activated.

Another feature of the presented scheme is the simultaneous measurement of the flux of the voltage transformer

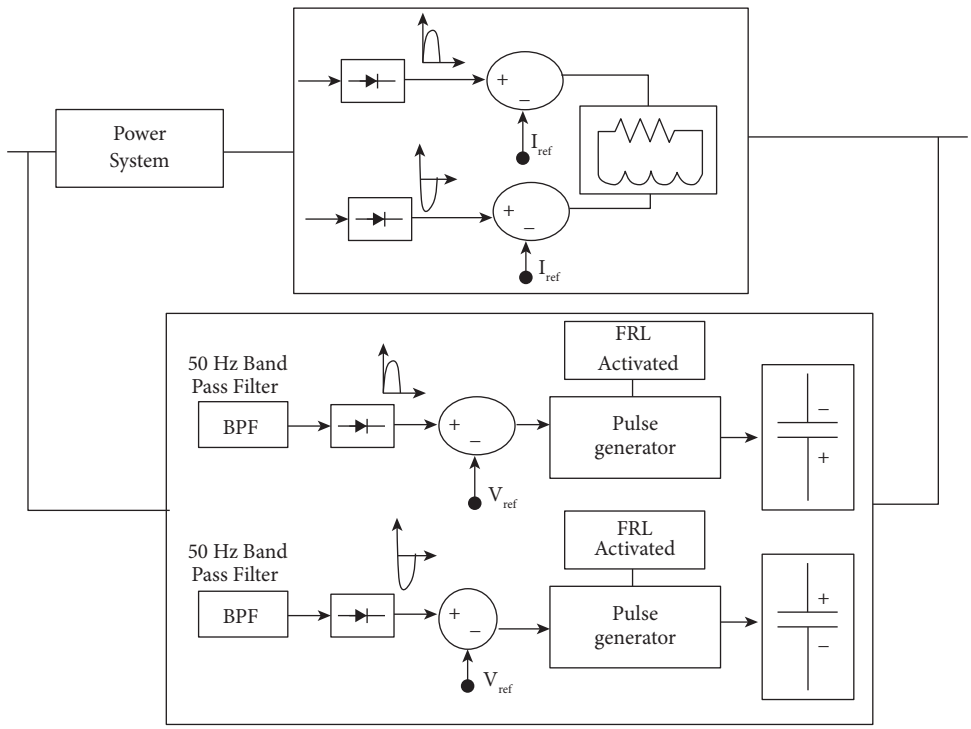


Figure 14: Conceptual control design for FRL operating mode.

and the line current in the network to prevent any maloperation in function activation.

5. Simulation Results

In this section, the performance of the closed-loop control system in different operating modes is implemented in the Matlab/simulink environment and the obtained results are analyzed. As shown in Figure 15, the proposed multifunctional structure is a two-part device, a shunt part that is connected to Bus A, and a series part that is inserted to the line. The technical information of the parameters and equipment are given in Table 4 which are taken from Refs. [10, 30, 40]. In addition, the load is considered as a constant impedance. The simulation results are obtained with and without the multifunctional controller.

The triple functions of the structure are implemented using Tables 1 and 2. In order to identify the network behaviors, it is necessary to measure and compare the required quantities for decision-making by the control system. Hence, as per Figure 15, the magnetic flux in the core of the voltage transformer and the transient current in the line are measured by a flux meter and a current transformer, respectively. The voltage transformer also measures the transient voltage of the network.

It should be noted that since there is no article that addresses such a triple function protective system in the literature, a fair comprehensive comparison with previous works cannot be made. However, the idea and other achievements are verified through comparison of the performances of the study system with and without the proposed structure when the system is faced with different events. In addition, several dual-function structures are selected to examine the performance of the proposed triple functional system. Based on the best knowledge of the authors, there is not any triple function protective device introduced in the literature, so the comparisons are carried out with those dual functions. Moreover, for a fair and valid comparison, the obtained results for each function are compared with the best and closest results given by the relevant articles.

5.1. Dynamic Voltage Compensation Mode. Voltage fault compensator and limiter are the protection functions of the proposed model, using the information given in Table 4. The technical information is taken from Refs. [10, 30, 40] to have a better comparison from the viewpoint of simulation output results.

A voltage swell can be caused by a reduction in the load, an outage of a motor, or a single line to ground fault. Figure 16(a) shows the result of inserting a synchronous voltage source which causes a 20 percent swell at the load bus. This voltage source is disconnected when the voltage is in the range of interest. As shown in Figure 16(b), the voltage disturbance is alleviated by using the proposed device.

On the other hand, a voltage sag is often observed due to events such as temporary and transient short circuits, large electric motors starting, and transient changes in the operating condition of large loads.

In the study system, a voltage sag is manipulated by connecting an impedance $Z_{enter} = 0.7 + j0.0005\,\Omega$ parallel to the load for 200 ms. The network experiences a voltage sag at the load terminal, as shown in Figure 17(a). The bus voltage and line current are measured and the type of

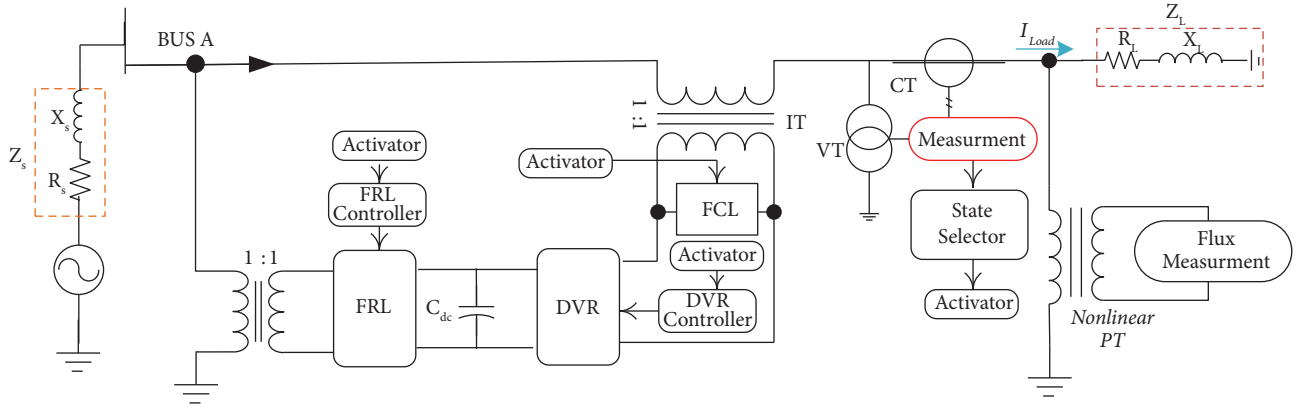


Figure 15: The proposed multifunctional structure along with the control system.

Table 4: Values of equipment and network parameters.

Elements	Normal state
Source voltage	20 kV
L_d	200 mH
R_p	500 Ω
Z_S	$1 + j0.01$ Ω
Z_L	$2 + j0.02$ Ω
Frequency	60 Hz
Switching frequency	1 kHz
C_{dc}	15 mF
DC link voltage	1 kV
C_{sh}	1.1 nf
C_s	0.5 nf
R_{fault}	0.0001 Ω
a	3.42
b	0.41
q	7–13

disturbance is identified. Then, the capacitor (C_{dc}) is entered to the network according to Figure 3(b), as shown by Figure 6(b).

The control system activates the compensator based on the voltage and current waveforms, and the result is shown in Figure 17(b). The proposed device can satisfactorily cope with the voltage sag. In addition, one of the important tasks of the control system is to check the status of K, which is less than one in the voltage sag phenomenon. The obtained results show more accuracy and faster performance in comparison with Ref. [30]. This is due to the reduction of the number of switches and also the increase of the speed of operation of the control system.

5.1.1. DVR Mode-Comparison with Refs. [12, 36]. An interline dynamic voltage restorer (IDVR) for sag mitigation, which is made of several dynamic voltage restorers (DVRs) with a common DC link, where each DVR is connected in series with a distribution feeder, is presented in Ref. [12]. During the sag period, the active power is interchanged between the feeders that casues voltage sag mitigation. Figure 18 compares the performances of the proposed protection structure with those given in Ref. [12]. The superiority of the proposed protection system is that it uses the charge of the DC capacitor as an independent voltage source that can operate bidirectionally to mitigate both voltage sag and swell. While in Ref. [12], the IDVR operates only for voltage sag by transferring the active power from one feeder to another, which means the DVRs are not independent.

On the other hand, for the evaluation of the proposed system performance during a voltage swell, Ref. [36] is selected, as shown in Figure 18. It should be noted that although a satisfactory result has been obtained by using the idea introduced in Ref. [36], the proposed system performance illustrates a relative superiority from identifying voltage swell and high speed response viewpoints.

5.2. Ferroresonance Overvoltage Limiter Mode. The phenomenon of ferroresonance overvoltage in the network occurs when an iron-cored inductor in an a.c. circuit can in certain circumstances result in a phenomenon known as "ferroresonance," considering the capacitor of the circuit breaker C_s (see Figures 1 and 8). The occurrence of the ferroresonance phenomenon in Figure 19(a) is an independent line with feeding from one end. A grid-independent line means a transformer located between the consumer of the grid and the transformers located in the transmission line. In the simulation, the series capacitor (C_s) is used to provide the conditions for the phenomenon to occur. For this purpose, by suddenly disconnecting the switch and increasing the voltage at the end of the line (transient overvoltage due to capacitive properties), the transformer operating point is moved on the curve and is located in the saturation zone of the curve. In the saturation zone, the magnetizing current of the transformer is significantly increased and the magnetizing current is established through the line with a high capacitance nature. The relationship between the saturation of the transformer core and the terminal voltage value examines the ratio of the flux of the magnetic core to the transformer voltage. Figure 19 depicts the variations of the terminal voltage versus time and core flux.

Figure 19(b) also shows that the core saturation generates a nonlinear inductance in the circuit, which in turn results in nonlinear voltage in the network. Furthermore, by inspecting the relationship between the core flux and the

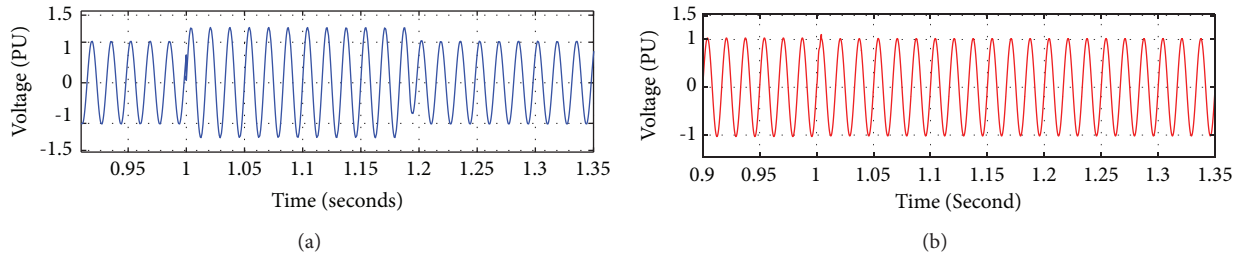


Figure 16: The voltage at Bus A following entering a capacitor series with the load in the period of (1.0–1.2) second (a) without the compensator (b) in the presence of the proposed voltage compensator.

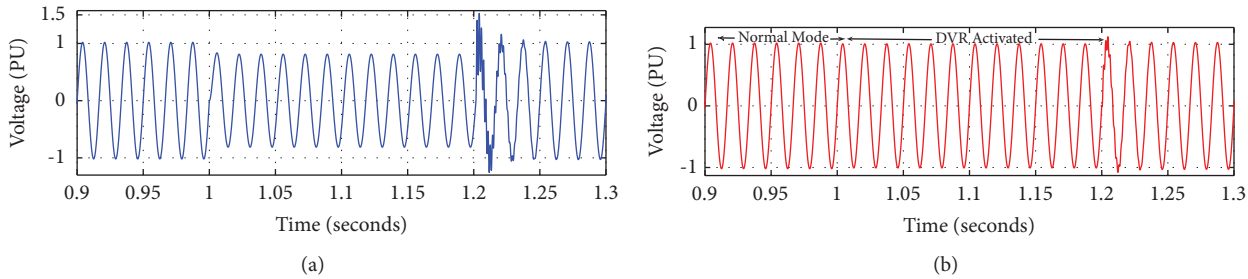


Figure 17: The voltage at Bus A following a shunt connection at an impedance to the network for 200 ms. (a) Without the compensator. (b) In the presence of the proposed voltage sag compensator.

terminal voltage, the ferroresonance can be detected. It should be noted that during the phenomenon, the voltage and current transformers are saturated which shows the occurrence of overvoltage due to the ferroresonance phenomenon in the network.

Now, by using the proposed limiter, the measurement unit measures the transformer core flux, the terminal voltage, and the line current, and in the case of the ferroresonance phenomenon, the corresponding function is activated. The obtained results show that the limiter successfully copes with the nonlinearities and alleviates the ferroresonance overvoltage, as seen in Figure 20. The equipment and network parameters are given in Table 4.

5.2.1. FRL Mode-Comparison with Refs. [32, 40]. When the ferroresonance phenomenon is initiated, nonlinear oscillations with amplitude up to 5 per unit may be observed and compensation is needed. Figure 21 compares the results obtained using the proposed protection scheme in the FRL mode and those given by the serious dual function competitors. Since the structure and parameters of the topology introduced in Ref. [32] are slightly similar to the proposed system in the FRL operating mode, this comparison can reveal that the idea presented in this paper does work satisfactorily. As per Figure 21, Ref. [32] can solve the overvoltage problem although a slight overvoltage still remains in the compensated PT voltage waveform. On the other hand, the proposed structure in the FRL mode can easily mitigate the dangerous overvoltage without any swell, although at the beginning and ending of the phenomenon, some distortions occurred.

The comparison is also performed with Ref. [40] to ensure the suitability of the proposed system. As the figure illustrates, the limited voltage in Ref. [40] is distorted and its amplitude is more than 2.5 times the rated value, so it needs to be seriously improved while the voltage limited by the proposed structure shows a suitable consistency with the preferroresonance waveforms. This can be because of the superiority of the proposed structure over the protection system introduced in Ref. [40], which is due to the integration of FCL and FRL that in turn results in a satisfactory limited voltage waveform.

5.3. Fault Current Limiter Mode. Short circuit current is one of the most serious threats to the health of the network equipment and should be identified and stopped as soon as it occurs. One of the capabilities of the proposed equipment is to limit the fault current, which, by adjusting its structure according to Figure 4 and using equation (6), puts a temporary impedance in the path of this current to control the current within the allowable range.

In this subsection, the performance of the proposed FCL in the face of a 100 ms single-phase to ground short circuit at the load side through a very small resistor (R_{fault}) is examined. R_{fault} value is given in Table 4.

Figure 22(a) indicates the current when the network experiences the fault while no limiter is in operation. As can be seen, the short circuit current flows about ten times the nominal value. Meanwhile, the control system considers all steps related to Tables 2 and 3 and measures the transient state of the current transformer, which indicates the saturation. In addition, the value of K is approximately equal to

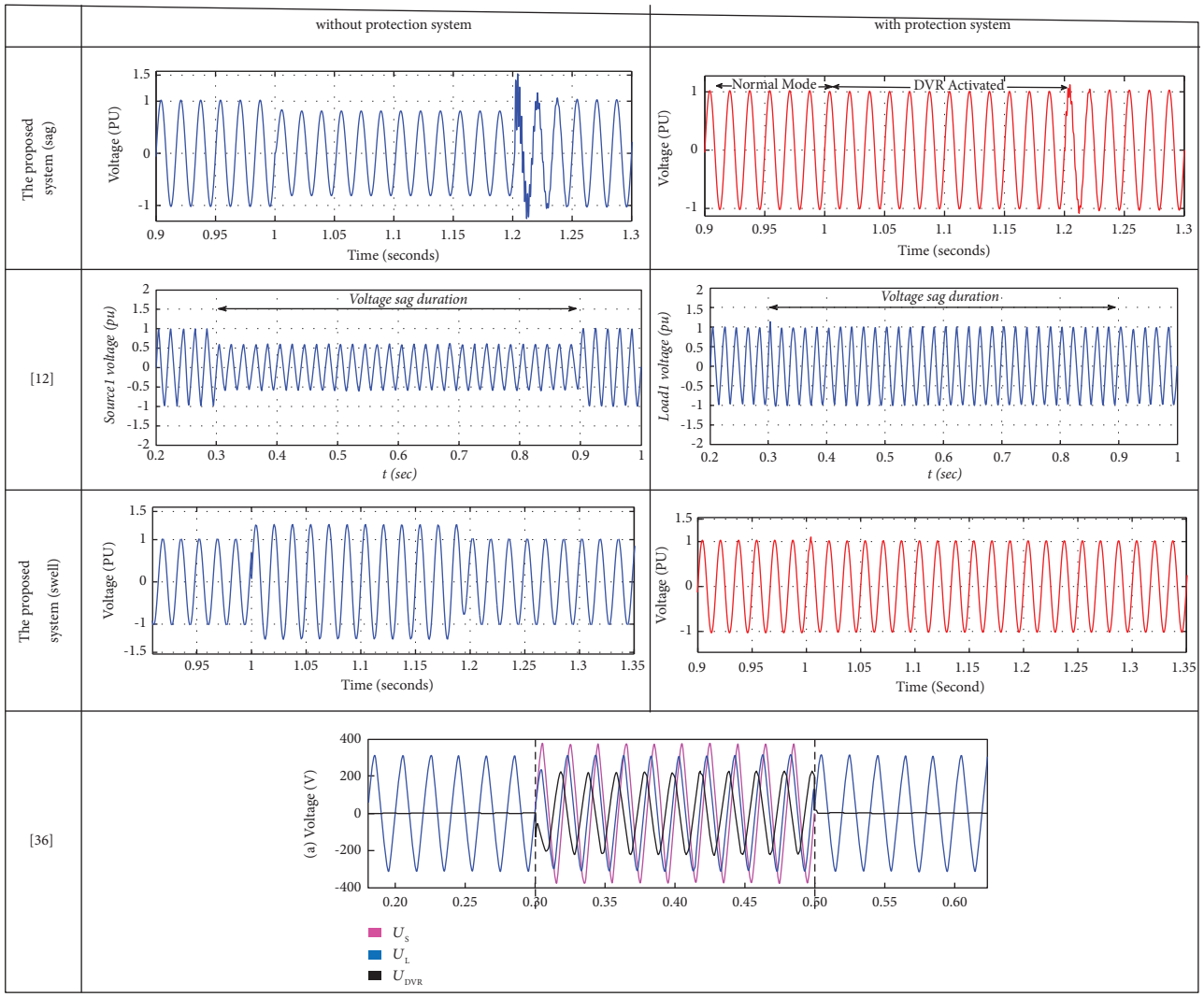


Figure 18: Comparison of the performances of the proposed system and results given in Refs. [12, 36] following a voltage sag/swell event.

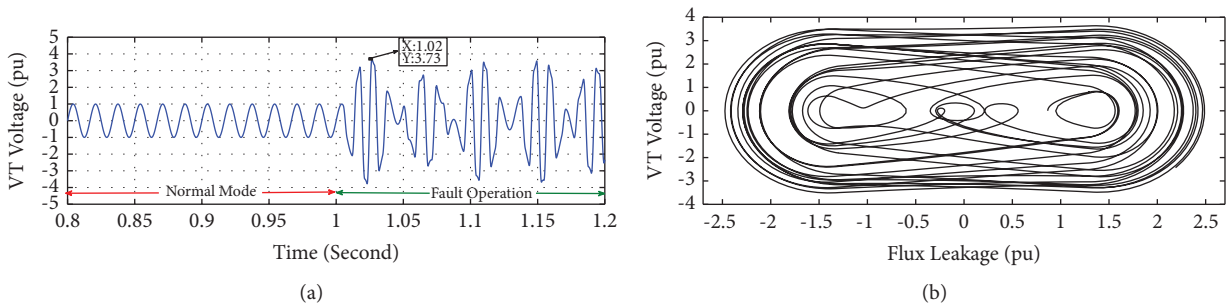


Figure 19: Variations of the terminal voltage following a ferroresonance phenomenon in the absence of the proposed limiter (a) versus time (b) versus core flux leakage.

zero and the network voltage is almost zero. Upon entering the proposed FCL, the obtained results show that the fault current is completely controlled as Figure 22(b) illustrates. Moreover, compared with Ref. [30], the proposed FCL using a paralleled resistor and inductor injected in series into the circuit shows a superior performance from accuracy and response speed viewpoints.

5.3.1. FCL Mode-Comparison with Refs [17, 36]. The simulation results obtained by using the proposed system when operating in the FCL mode can be compared with those given by the competitors. According to the results shown in Figure 23, the proposed system limits the fault current at the rated value while Ref. [17] sets it at zero. This is because the mechanisms of limiting the fault current in the proposed

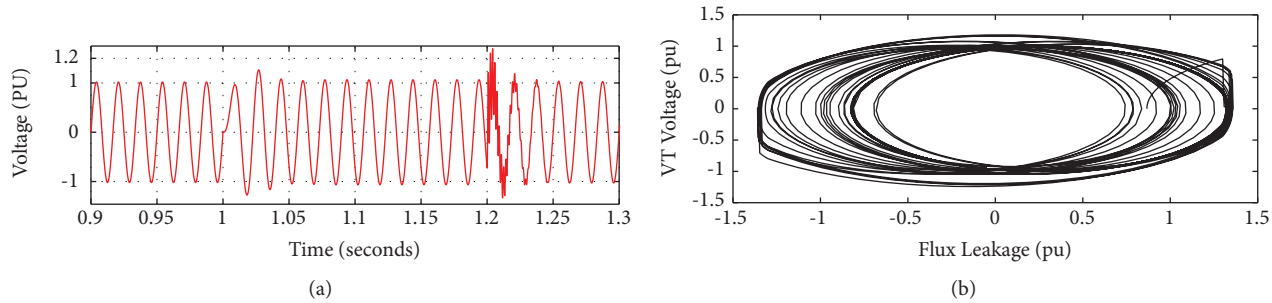


FIGURE 20: Variations of the terminal voltage following a ferroresonance phenomenon in the presence of the proposed limiter (a) versus time (b) versus core flux leakage.

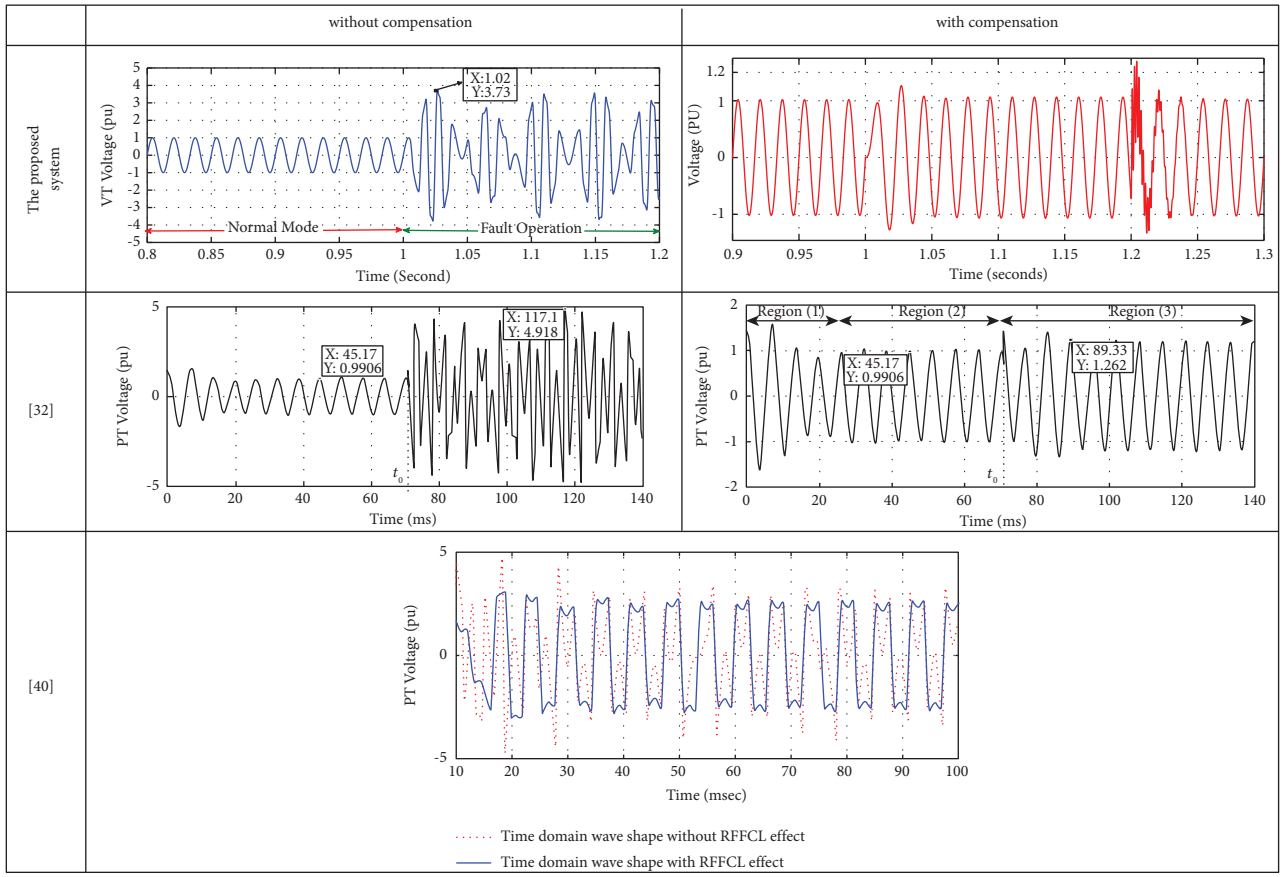


FIGURE 21: Comparison of the proposed protection system performance in the FRL mode and those presented in Refs [32, 40] from the voltage waveform viewpoint.

structure and Ref. [17] are completely different. The former puts a parallel RL circuit in series with the line while the later inserts a parallel LC resonance tank in series with the line. As we know, putting a parallel LC resonance circuit in series with the line causes an open circuit and the current becomes zero. On the other hand, in the proposed system, a parallel RL is used which depends on the parameters' amount, and the fault current can be changed in a wide range of interest except zero. Of course, this is not a serious concern because limiting the fault current by the FCL is enough to be a fraction of the rated current, and there is no need to set it to zero.

Furthermore, the simulation result obtained by the proposed structure is compared with that presented in Ref. [36] when both are in the FCL operating mode. In Ref. [36], a phase to ground fault occurs at 0.605 s and lasts for 10 cycles which creates a current slightly larger than the rated value, so the short circuit current is not very destructive and therefore it cannot seriously examine the FCL-DVR performance. In addition, the FCL-DVR is not very successful in limiting the short circuit current when conceptually compared with the protective system introduced in this paper.

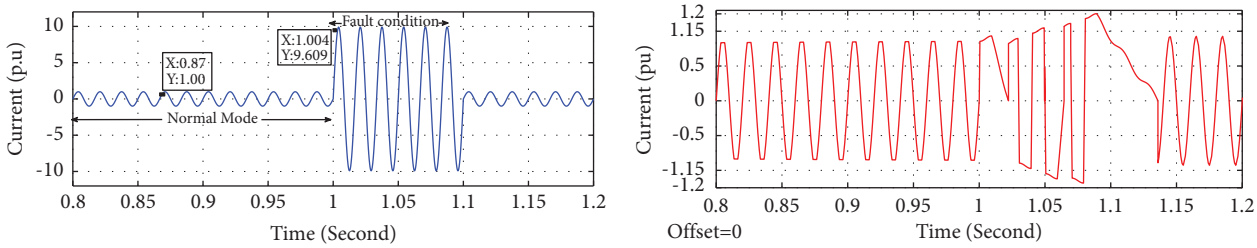


Figure 22: Waveforms of short circuit current of one phase to ground (a) without fault current limiter activation (b) with fault current limiter activated.

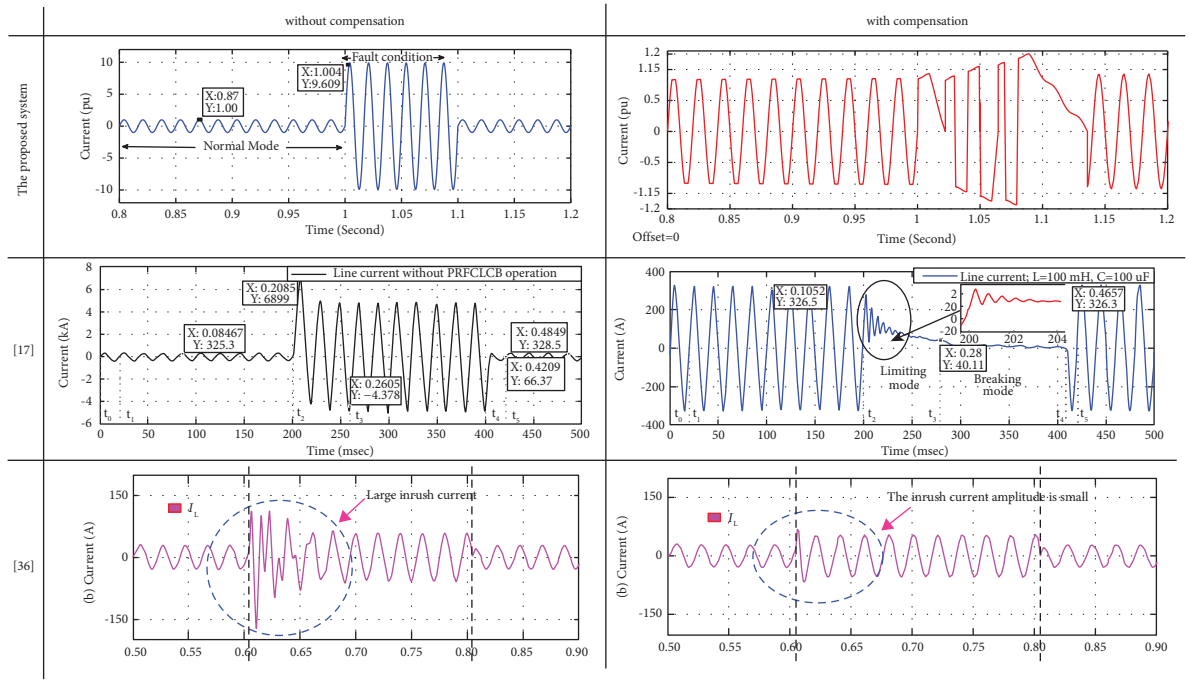


Figure 23: The line current following a short circuit fault at the load bus with and without the proposed system in the FCL mode is compared with Refs [17, 36].

6. Considerations of Prototype Model

From the viewpoint of the prototype model, the following key points should be considered:

(i) Technical characteristics of the elements used in the protective structure, e.g., the operational rating of the components have to be able enough to offer all triple functions and also should be in coordination with the short circuit level of the power supply

(ii) In order to protect the prototype model, the power supply must be equipped with a current limiter

(iii) The sampling frequency of the A/D module should be at least twice the highest frequency contained in the signals (Nyquist–Shannon sampling theory)

(iv) The specification of the digital computer as a data processor (hardware part) and also computational algorithms must be compatible with the speed of the phenomena studied in the paper

(v) Selecting the rate and the manufacturers of the power switches affect the cost and the overall performances of the protective system, hence they must be used with care

(vi) Control strategy must be quick enough to respond to the naturally fast transients phenomena

7. Conclusion

In this paper, a novel and unified power electronic-based multifunctional structure is introduced to limit fault current, compensate the voltage sag/swell, and alleviate ferroresonance overvoltage from the viewpoint of conceptual ideation. The proposed structure successfully aggregates three functions in one protection device with less power electronic components in comparison with dual function competitors and therefore less construction cost and also less losses. In addition, the functions can be satisfactorily identified and discriminated using the ratio of load and

system impedances and then activated by an elaborated control scheme. Each function is equipped with a predesigned control scheme that is activated with its corresponding mode. The performance of the protective system is verified by a set of numerical simulation results that show that the idea works appropriately. However, the supplementary discussions about practical implementation and technical points as well as optimization are left to be studied in a separate article.

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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