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Research Article

An Enhanced Modified Multiport Interleaved Flyback Converter for Photovoltaic-Shunt Active Power Filter (PV-SHAPF) Applications

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This paper presents a newly designed modified multiport interleaved flyback converter (MMPIFC) to transfer the photovoltaic (PV) power to the DC bus of the parallel-connected multilevel inverter-based shunt active power filter (SHAPF). The proposed modified multiport interleaved flyback converter (MMPIFC) is designed to interconnect N number of input power sources into the DC bus of the SHAPF to fix the problems with the partial shadow and improve the SHAPF's ability to compensate. Compared to the commonly used interleaved flyback converter (IFC), the proposed MMPIFC has a larger boost factor toward the DC voltage input. The flow of power between the different power sources and SHAPF is controlled by varying the duty ratio of the main switches. The working principles of the proposed MMPIFC-operated PV-SHAPF are explored in this paper, and essential design concerns are highlighted. A prototype model with 1 kVA, 400 V, and 50 HZ is built and tested under various conditions to validate the theoretical analysis, design, and control method.

1. Introduction

The installation of renewable power generation systems on the level of microgrids and medium power grid-connected applications has increased dramatically, in recent years [1–4]. The employment of power electronics converters in the renewable power generation system offers various benefits including small size, good dynamic response, and high reliability. The converters are more frequently switched on to transfer the power from the input source. These converters have highly nonlinear characteristics and result in huge harmonics in power systems. The traditional solution for this problem is to use passive LC filters to remove the harmonics imposed by the power converters into the grid. The passive LC filters can reduce the most prominent harmonics and compensate for some reactive power. However, when frequency deviations occur, its use tends to deteriorate. Furthermore, issues such as the possibility of resonance, heavyweight, huge size, and fixed tuning limit the usage of passive filters in the power network.

Power electronics-based custom power devices such as shunt active power filters (SHAPFs) and series active power filters (SAPFs) have been developed to address these issues [5]. SHAPFs are becoming increasingly significant in addressing harmonic issues. SHAPF was first used exclusively to mitigate the current harmonics caused by nonlinear loads. The SHAPF powered by the DC link capacitor cannot compensate long-term issues caused by the nonlinear loads. Hence, photovoltaic (PV) interfaced SHAPFs were developed and implemented to perform multiple functions. The integration of the PV system with the DC link of SHAPFs needs a DC-DC converter to offer the DC voltage with the demanded magnitude. The conventional DC-DC converter may not provide enough boosting gain for the PV voltage due to its low boosting gain, higher active and passive components, and lower conversion efficiency. The boost

converter topologies such as flyback, switched capacitor, switched inductor, interleaved, and Z-source converters were developed to provide the demanded boost factor [6–10].

A modified three-port interleaved flyback converter with a PV array tied to it is built to power a SHAPF [11]. The modified three-port interleaved flyback converter is made to send power from a PV source to a SHAPF to make up for the current harmonics that happen when a nonlinear load is connected to the power distribution system. To enhance power quality and provide clean electricity, a photovoltaic-integrated SHAPF was designed and implemented. It uses more number of active switches which leads to DC ripple and low efficiency. A system that employs maximum power point tracking based on an adaptive neuro-fuzzy inference system and control of synchronous reference frame theory-based SHAPF compensates for the current harmonics as well as the conventional SHAPF [12]. An empirical mode decomposition control approach has been used to extract the fundamental component and establish the reference for harmonic extraction in a cascaded multilevel inverter-based SHAPF. A unique empirical mode decomposition approach is used to find the basic component of load current from nonlinear load current samples. The intrinsic mode function is extracted via spline interpolation [13]. A method developed for increasing the input power factor of a single-phase rectifier followed by an inductive filter has been presented in [14]. It entails connecting the output side of the diode bridge to a two-quadrant active power filter based on a typical bidirectional DC-DC converter. This technology enables the functioning of the rectifier range in the continuous conduction mode to be extended. A SHAPF coupled with a solar source for significant harmonic reduction, energy management, and reactive power compensation has been suggested in reference [15]. To mitigate the current harmonics of a three-phase four-wire distribution system, a SHAPF powered by a PV array and battery-tied DC-DC boost converter has been implemented. Its intended function is to improve the system's power factor by reducing the source current's harmonics. The instantaneous p-q theory-based control algorithm has been incorporated with the suggested PV-supported SHPAF to enhance the compensation ability [16].

To overcome the limitations of capacitor-supported SHAPF, numerous power converter topologies have been proposed. Classic DC-DC converter topologies utilized in the SHAPF front end deliver the maximum PV voltage gain, according to the literature. The PV-interfaced SHAPF is inactive on shadow days due to its limited boosting capabilities. The PV-SHAPF powered by the PV array needs a high boost, high-efficiency DC-DC converter to create regulated voltage. Interleaved flyback converters have been studied to increase conversion efficiency and boost gain. The conventional interleaved boost full-bridge three-port converter considered for the development of the proposed high boost converter is illustrated in Figure 1.

To improve the boosting gain and provide a high boost factor for the input voltage, a photovoltaic (PV) array interfaced modified multiport interleaved flyback converter

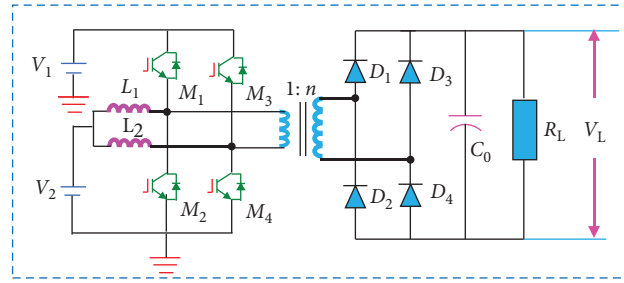


Figure 1: Conventional interleaved boost full-bridge three-port converter.

(MMPIFC) is proposed in this study. It increases the capability of accepting a wide range of DC input voltage and enhances the mitigation ability of the PV-SHAPF. The following are the primary contributions of this study:

(i) The PV array and SHAPF DC bus are connected via the proposed MMPIFC to enrich the current harmonics mitigation ability and the active power transfer ability of the conventional boost converter-powered SHAPF.

(ii) The proposed MMPIFC is designed to offer a high boost factor with a reduced duty ratio and switching losses.

(iii) The MMPIFC-powered SHAPF is switched using a simple control method based on the SRF theory. The computation of the reference compensation current has been proven to be simple and quick.

(iv) The system's operation in both fixed and dynamic load conditions are analyzed and described in depth. The behavior of the proposed PV-SHAPF under load fluctuation, constant load, and constant and variable insolation is determined to be good and in conformity with an IEEE-519 standard. The capability of the proposed MMPIFC boost converter-connected SHAPF is thoroughly examined.

In the following sections, the design and architecture of the newly developed MMPIFC are presented. The simulation and experimental results obtained from the prototype model of the proposed MMPIFC boost converter-powered PV-SHAPF are presented to verify the theoretical analysis. A comparison with the simulation and experimental model findings is offered at the end of this manuscript to demonstrate the potential benefits of the proposed MMPIFC boost converter fed PV-SHAPF.

2. System Architecture and Design of the Proposed PV-SHAPF

The system architecture of the proposed PV-SHAPF consists of a PV array, proposed MMPIFC boost converter, DC bus, shunt active power filter (SHAPF), three-phase rectifier nonlinear load, shunt reactor, utility grid, and simple synchronous reference frame (SRF) control strategy which is shown in Figure 2. The interconnection of nonlinear load into the three-phase utility grid introduces unwanted frequency

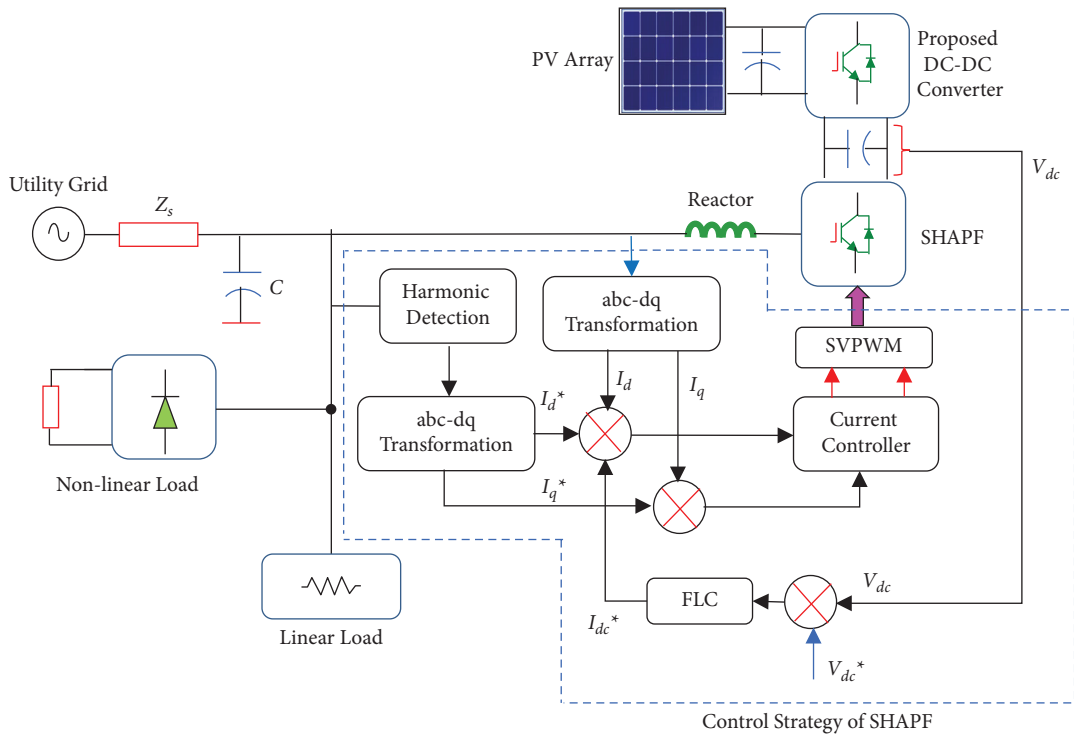


Figure 2: System architecture of the proposed MMPIFC boost converter operated SHAPF.

components into the power line. The harmonic detection algorithm extracts the fundamental frequency components required for the generation of the reference current.

The power circuit topology of the PV-connected MMPIFC boost operated SHAPF is depicted in Figure 3. The proposed MMPIFC depicted in Figure 3 is derived from the conventional interleaved boost converter topology presented in Figure 1 [17] and the quasi-Z-source converter presented in reference [18]. The proposed modified multiport interleaved flyback converter (MMPIFC) works based on combining an additional multi-input high-frequency transformer with the single switched-capacitor branch C_{x1} and C_{x2} utilized in each input stage. The proposed configuration allows the integration of N number of input sources into the DC bus of the SHAPF via a multi-input high-frequency transformer. The $N+1$ number of windings is required to integrate N number of input sources. The proposed converter achieves a higher output voltage gain by combining the switched-capacitor cell with the multi-input high-frequency transformer. Inserting the switched-capacitor configuration in each input port enables the independent maximum power point tracking (MPPT) and control over the input voltage.

To simplify the complexity of understanding the distinct modes of operation of the proposed MMPIFC, the following assumptions are made:

(1) The number of input sources or PV array connected with the proposed MMPIFC converter is considered as 2.

(2) The parasitic effect and switching losses are considered negligible. All the power semiconductor devices, capacitors, and inductors are assumed to be ideal.

(3) The capacitors C_{A1}, C_{A2}, C_{B1}, C_{B2}, and C in the input port of the proposed MMPIFC are equal. The circuit diagram of the proposed modified two input interleaved flyback converter (MTIIFC) is presented in Figure 4.

The proposed MTIIFC boost converter fed three-phase three-level inverter-based SHAPF is operated under twelve modes of operation. The switching position of the MTIIFC and SHAPF decides the mode of the proposed system. The equivalent circuits of twelve modes of operations are presented in Figures 5–10 and and Figures 11(a)–11(f).

2.1. Modes of Operation of the Proposed MTIIFC Boost Converter Fed SHAPF. At $t=0$, during mode 1, S_A and S_B are switched on, and the input inductors L_A and L_B are charged by PV source 1 and 2 as illustrated in Figure 5. The amount of energy that is held in the input inductors LA and LB is dependent on the duty ratio. This relationship can be represented as

$$E_{LA} = \int_{t_0}^{t_1} L i_{pv1} di_{pv1} = \frac{1}{2} L i_{pv1}^2, \quad (1)$$

$$E_{LB} = \int_{t_0}^{t_1} L i_{pv2} di_{pv2} = \frac{1}{2} L i_{pv2}^2. \quad (2)$$

The amount of energy that is stored on the input inductors L_A and L_B is mostly determined by the length of time that the power switches S_A and S_B are turned on for their respective circuits. The primary winding 1 of the high-

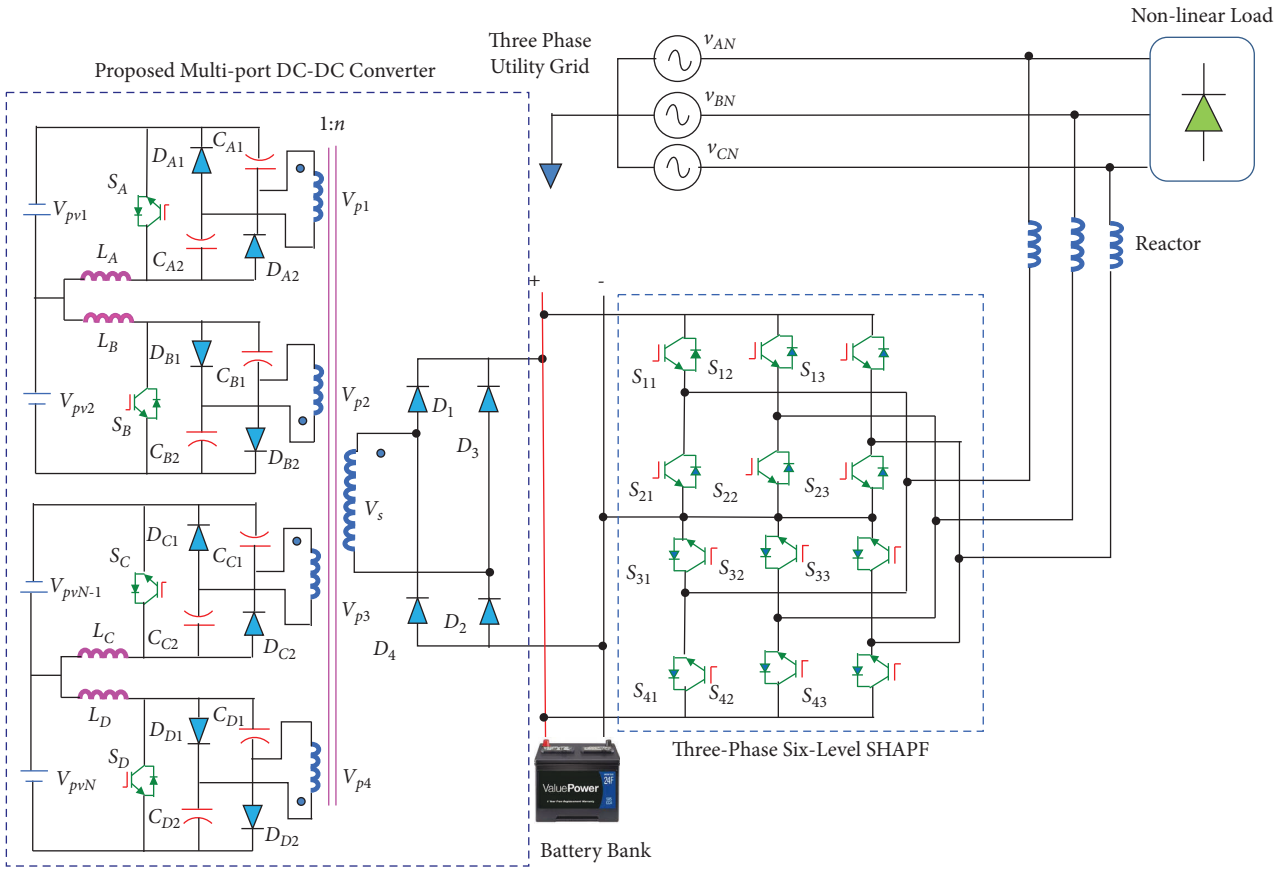


Figure 3: Power circuit of the proposed N-port interleaved flyback converter fed SHAPF.

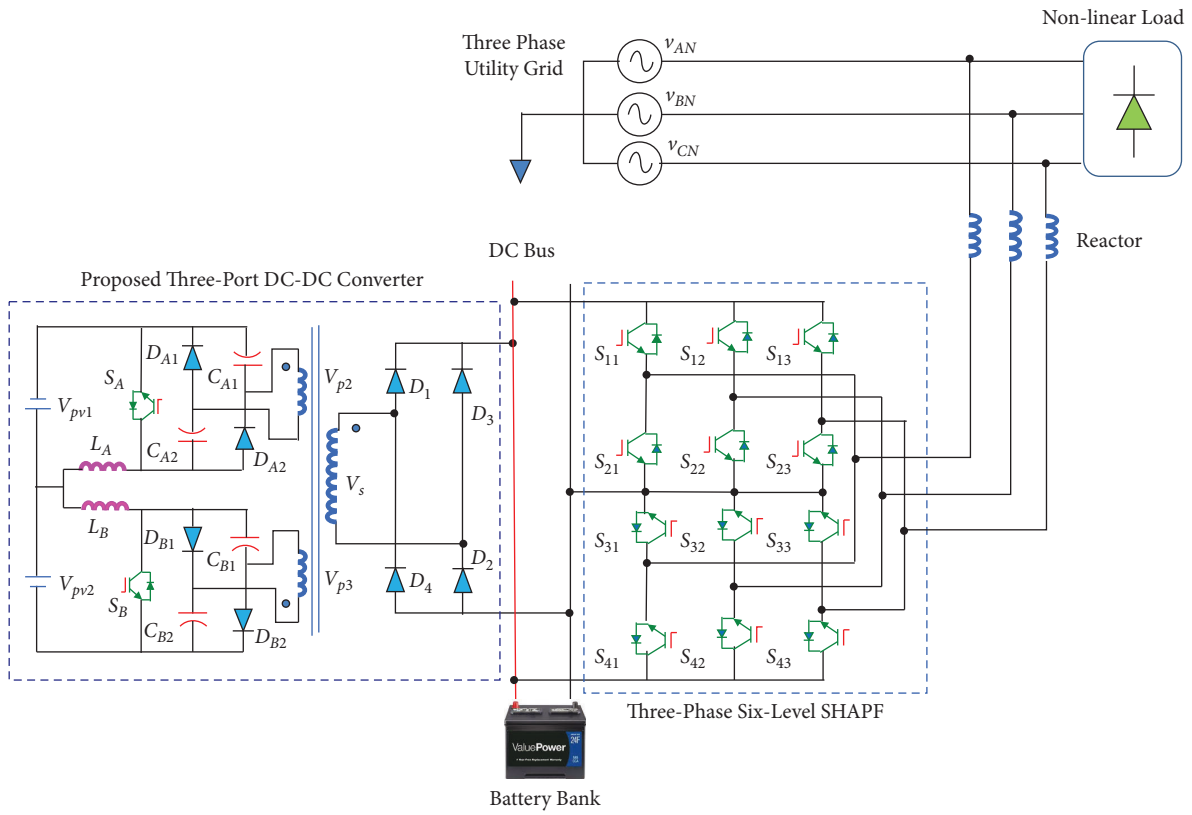


Figure 4: Circuit diagram of the proposed PV-tied MTIIFC powered SHAPF.

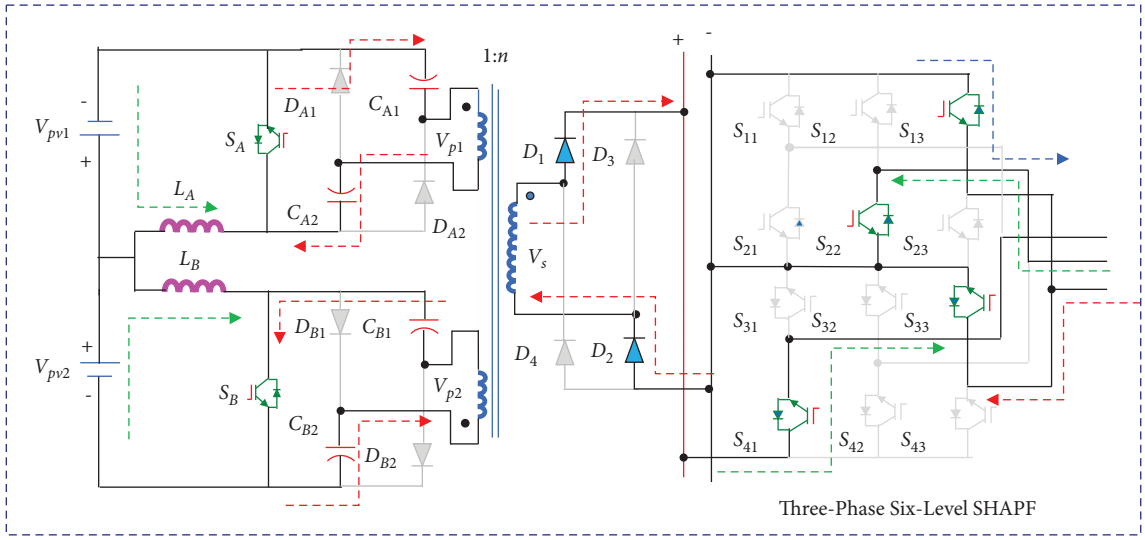


Figure 5: Equivalent circuit of mode 1 operation.

frequency transformer is connected in series with the capacitors C_{A1} and C_{A2}. The diodes D_{A1} and D_{A2} are biased in the opposite direction by the voltage that exists across the capacitors C_{A1} and C_{A2}. In a manner analogous to that of port 1 of the MTIIFC, port 2 sends the energy that has been stored in the capacitors C_{B1} and C_{B2} to primary 2 of the high-frequency transformer by means of switch S_B. The voltage equations for the input inductors L_A and L_B are shown in (2) and (3), respectively.

$$V_{LA}^{I} = L\frac{di_{pv1}^{I}}{dt}(t_1 - t_0), \tag{3}$$

$$V_{LB}^{I} = L\frac{di_{pv2}^{I}}{dt}(t_1 - t_0). \tag{4}$$

The voltage supplied by the series connection of the capacitors C_{A1} and C_{A2} and the series combination of the capacitors C_{B1} and C_{B2} are expressed as

$$V_{p1}^{I} = V_{C_{A1}} + V_{C_{A2}}, \tag{5}$$

$$V_{p2}^{I} = V_{C_{B1}} + V_{C_{B2}}. \tag{6}$$

The voltage supplied by the secondary of the high-frequency transformer to the DC bus of the SHAPF can be expressed as

$$V_S^I = \left(V_{p1}^I + V_{p2}^{II}\right) * n. \tag{7}$$

The system will transition into its second mode of operation whenever all the switches have been turned off at the same time, which is $t = t_1$. Figure 5 displays the comparable circuit of mode 1. In order to provide six different levels of compensating current for the purpose of current harmonics mitigation, the inverter switches S_{13}, S_{22}, S_{33}, and S_{41} are maintained in the on state. There are three levels formed at the output terminals of the TPSL multilevel inverter, and they are as follows: $V_{ab} = 2V_{dc}$, $V_{bc} = V_{ca} = -V_{dc}$, and $V_{bc} = V_{ca} = -V_{dc}$.

As shown in Figure 6, the charge that was stored in the input inductor L_A while the device was operating in mode 1 is then discharged to the capacitors C_{A1} and C_{A2} by way of the diodes D_{A1} and D_{A2}. In a manner analogous to port 1, the energy that was stored in the input inductor L_B was transferred to primary 2 of the high-frequency transformer. Inductors L_A and L_B, which are part of the input circuit, are set up to release the energy they have stored until time t_2. Both capacitor C_{A2} and capacitor C_{A1} receive their DC power from the input photovoltaic source V_{pv1} and the input inductor L_A, respectively, via the diodes D_{A1} and D_{A2}. The voltage that can be measured across capacitors C_{A1} and C_{A2} can be expressed as

$$V_{C_{A1}}^{II} = V_{pv1} + V_{L_A}^{I}, \tag{8}$$

$$V_{C_{A2}}^{II} = V_{pv2}^{II} + V_{L_B}^{I}. \tag{9}$$

The voltage provided to the capacitors C_{A1},C_{A2}, C_{B1}, and C_{B2} is the function of the duty cycle, and it is expressed in

$$V_{C_{A1}}^{II} = V_{C_{A2}}^{II} = \frac{V_{pv1}}{1 - D_{S_A}}, \tag{10}$$

$$V_{C_{B1}}^{II} = V_{C_{B2}}^{II} = \frac{V_{pv2}}{1 - D_{S_B}}. \tag{11}$$

When the timer reaches $t = t_1$, the SHAPF inverter switches S_{12}, S_{23}, S_{32}, and S_{41} are turned on. There are three levels that are produced for the voltage that has three phases: $V_{ab} = V_{bc} = V_{dc}$ and $V_{ca} = -2V_{dc}$.

When time equals t_2, the switches S_A and S_B are activated, and the photovoltaic sources 1 and 2 begin to charge the input inductors L_A and L_B, as depicted in Figure 7. This mode is comparable to mode 1, which is discussed in Section 2.1. The length of time that switches S_A and S_B are turned on is directly proportional to the quantity of energy that is stored on the input inductors L_A and L_B. The high-frequency transformer has its primary 1 linked in series

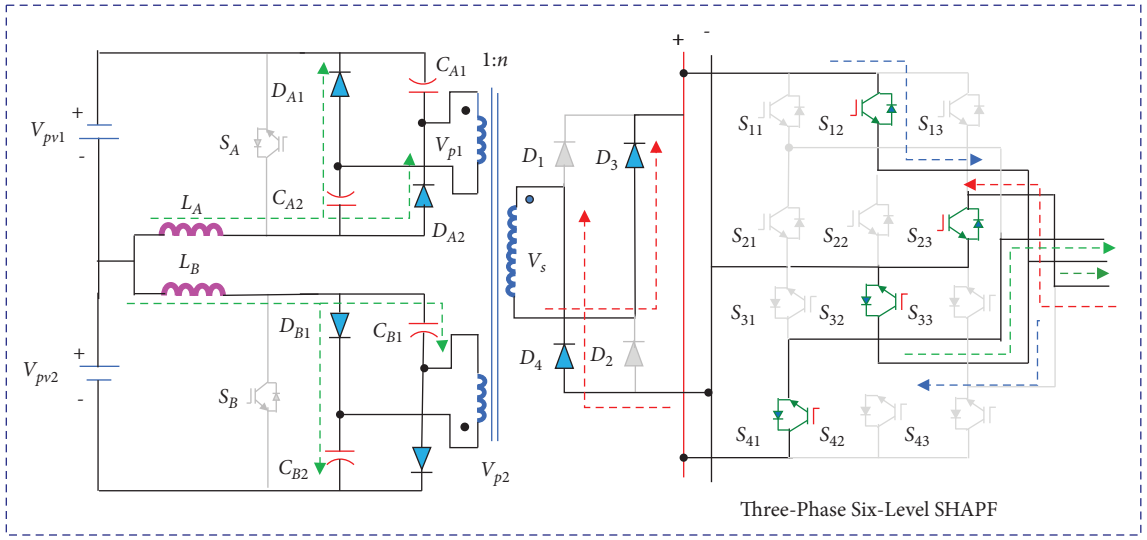


Figure 6: Equivalent circuit of mode 2 operation.

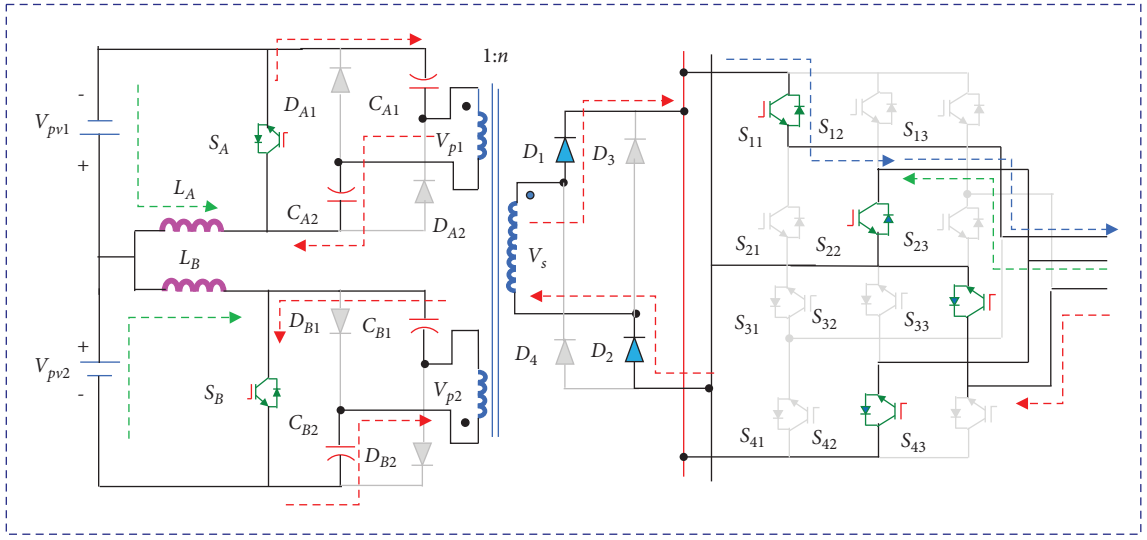


Figure 7: Equivalent circuit of mode 3 operation.

with both C_{A1} and C_{A2}. It is possible to invert the bias of the diodes D_{A1} and D_{A2} by reversing the voltage that is present between the capacitors C_{A1} and C_{A2}. The energy that is stored in the capacitors C_{B1} and C_{B2} is transferred by switching S_B from port 2 of the MTIIFC to primary 2 of the high-frequency transformer. Equations (12) and (13) display the voltage equations for the input inductors L_A and L_B, respectively.

$$V_{LA}^{III} = L\frac{di_{pv1}^{III}}{dt}(t_3 - t_2), \tag{12}$$

$$V_{LB}^{III} = L\frac{di_{pv2}^{III}}{dt}(t_3 - t_2). \tag{13}$$

The voltage supplied by the capacitors C_{A1} and C_{A2} and the capacitors C_{B1} and C_{B2} is expressed as

$$V_{p1}^{III} = V_{C_{A1}}^{II} + V_{C_{A2}}^{II}, \tag{14}$$

$$V_{p2}^{III} = V_{C_{B1}}^{II} + V_{C_{B2}}^{II}. \tag{15}$$

The output voltage of the high-frequency transformer can be expressed as

$$V_s^{III} = \left(V_{p1}^{II} + V_{p2}^{II}\right) * n. \tag{16}$$

The system enters the fourth mode of operation when switches S_A and S_B are switched off at $t = t_3$. The corresponding circuit of mode 3 is shown in Figure 7.

In order to provide six levels of compensatory current for the reduction of current harmonics, the inverter switches S_{11}, S_{22}, S_{33}, and S_{42} are maintained in the "on" position. At the terminals of the TPSL multilevel inverter's output are formed the following three levels: $V_{ab} = V_{bc} = V_{dc}$, and $V_{ca} = -2V_{dc}$.

As shown in Figure 8, the input inductor L_A charged during mode 3 operation is discharged to the capacitors C_{A1} and C_{A2} through the diodes D_{A1} and D_{A2}. Similar to port 1 operation, the input inductor L_B released its stored energy to the primary 2. L_A and L_B, the input inductors, are set to distribute their stored energy until t_4. The DC power is supplied to the capacitors C_{A2} and C_{A1} through the diodes D_{A1} and D_{A2}, respectively, by the input PV source V_{pv1} and the input inductor L_A.

The voltage between capacitors C_{A1} and C_{A2} is denoted as

$$V_{C_{A1}}^{IV} = V_{pv1}^{IV} + V_{L_A}^{III}, \tag{17}$$

$$V_{C_{A2}}^{IV} = V_{pv2}^{IV} + V_{L_B}^{III}. \tag{18}$$

The voltage supplied to the capacitors C_{A1}, C_{A2}, C_{B1}, and C_{B2} is a function of the duty cycle and is

$$V_{C_{A1}}^{IV} = V_{C_{A2}}^{IV} = \frac{V_{pv1}}{1 - D_{S_A}}, \tag{19}$$

$$V_{C_{B1}}^{IV} = V_{C_{B2}}^{IV} = \frac{V_{pv2}}{1 - D_{S_B}}. \tag{20}$$

At the time equivalent to t_4, the SHAPF inverter switches S_{13}, S_{21}, S_{33}, and S_{41} are turned on. The three-phase voltage can be broken down into three different voltage levels: $V_{ab} = V_{bc} = -V_{dc}$ and $V_{ca} = 2V_{dc}$.

At time $t = t_4$, switches S_A and S_B are activated once more as part of mode 1 and mode 3, and the PV sources 1 and 2 begin to charge the input inductors L_A and L_B, as depicted in Figure 9. This mode operates in a manner that is comparable to modes 1 and 3, as explained before, with the exception that the three-phase, three-level inverter switches. The quantity of energy that has been stored on the input inductors L_A and L_B is then discharged to primary 1 and primary 2 of the high-frequency transformer. The voltage equations for modes 1 and 3 are very similar to one another. At the time equivalent to t_5, the SHAPF inverter switches S_{13}, S_{23}, S_{33}, and S_{41} are turned on. The three-phase voltage can be broken down into three different voltage levels: $V_{ab} = V_{ca} = -V_{dc}$ and $V_{bc} = 2V_{dc}$.

The mode-6 operation starts at $t = t_5$ or when the switches S_A and S_B are turned off as presented in mode 2 and mode 4. The operation and voltage balance equations are similar to mode 2 and mode 4 except for the operation of the SHAPF inverter. The SHAPF inverter switches S_{13}, S_{21}, S_{33}, and S_{42} are activated to create a three-phase voltage: $V_{ab} = -2V_{dc}$, $V_{bc} = -V_{dc}$ and $V_{ca} = V_{dc}$. Equivalent circuit of mode 6 is shown in Figure 10.

The operation of the remaining six modes and related mathematical equations are similar to the modes presented from mode 1 to mode 6. Mode 7, mode 9, and mode 10 are similar to mode 1, and mode 8, mode 10, and mode 12 are similar to mode 2. The equivalent circuit of modes 7 to 12 is illustrated in Figures 11(a)–11(f) The inverter switches are switched as per the requirement of the output voltage. The switching sequence and their corresponding output voltage are tabulated in Table 1.

2.2. Voltage Gain Calculation of the Proposed MTIIFC Boost Converter. When the main switches of the MTIIFC boost converters S_A and S_B are switched on as shown in Figure 5, then the voltage across the input inductors L_A and L_B are equal to the PV source voltage V_{pv1} and V_{pv2}. It is expressed as

$$V_{L_A} = V_{pv1}, \tag{21}$$

$$V_{L_B} = V_{pv2}. \tag{22}$$

When the switches of the MTIIFC boost converters S_A and S_B are turned off, then the input PV source 1 and 2 and the input inductors charges the capacitor C_{A1}, C_{A2}, and C_{B1} and C_{B2} are charged to $(V_{pv1} + V_{LA})$ and $(V_{pv2} + V_{LB})$, respectively. The voltage across the capacitive elements C_{A1}, C_{A2}, and C_{B1}, and C_{B2} are expressed as

$$V_{C_{A1}} = V_{C_{A2}} = V_{pv1} + V_{L_A}, \tag{23}$$

$$V_{C_{B1}} = V_{C_{B2}} = V_{pv2} + V_{L_B}. \tag{24}$$

The capacitive elements utilized in the input port 1 and 2 boost the voltage to twice the value of input voltage. The voltage fed to the primary 1 and 2 by the capacitive elements is expressed as

$$V_{p1} = \left(V_{pv1} + V_{L_A}\right) * 2, \tag{25}$$

$$V_{p2} = \left(V_{pv2} + V_{L_B}\right) * 2. \tag{26}$$

The output of the high-frequency transformer for the input presented in equations (25) and (26) is

$$V_s = \left(\left(V_{pv1} + V_{L_A}\right) * 2\right) + \left(\left(V_{pv1} + V_{L_A}\right) * 2\right) * n. \tag{27}$$

When both the PV panel voltages are same ($V_{pv1} = V_{pv2} = V_{pv}$), then the output voltage of the secondary winding can be expressed as

$$V_s = \left(V_{pvx} + V_{L_x}\right) * 4 * n. \tag{28}$$

One possible rewrite of the output voltage of the MTIIFC boost converter is as follows:

$$V_{dc} = \left(\frac{V_{pvx}}{1 - D_{Sx}}\right) * 4 * n. \tag{29}$$

When the V_{pv1} and V_{pv2} are not equal, then the output voltage of the MTIIFC can be expressed as

$$V_{dc} = \left(\left(\frac{V_{pv1}}{1 - D_{SA}}\right)2 + \left(\frac{V_{pv2}}{1 - D_{SB}}\right)2\right) * n. \tag{30}$$

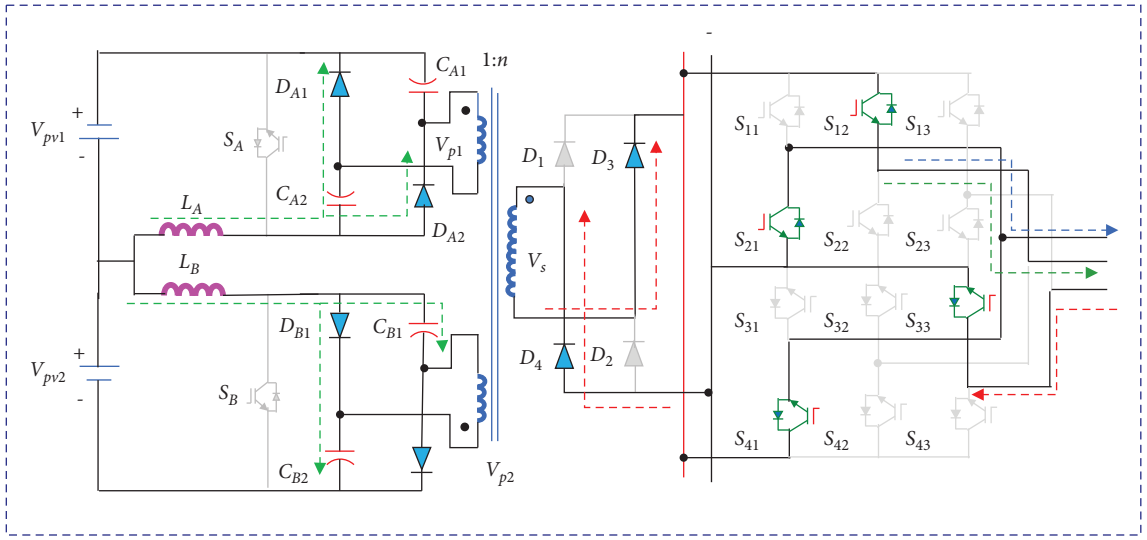


Figure 8: Equivalent circuit of mode 4 operation.

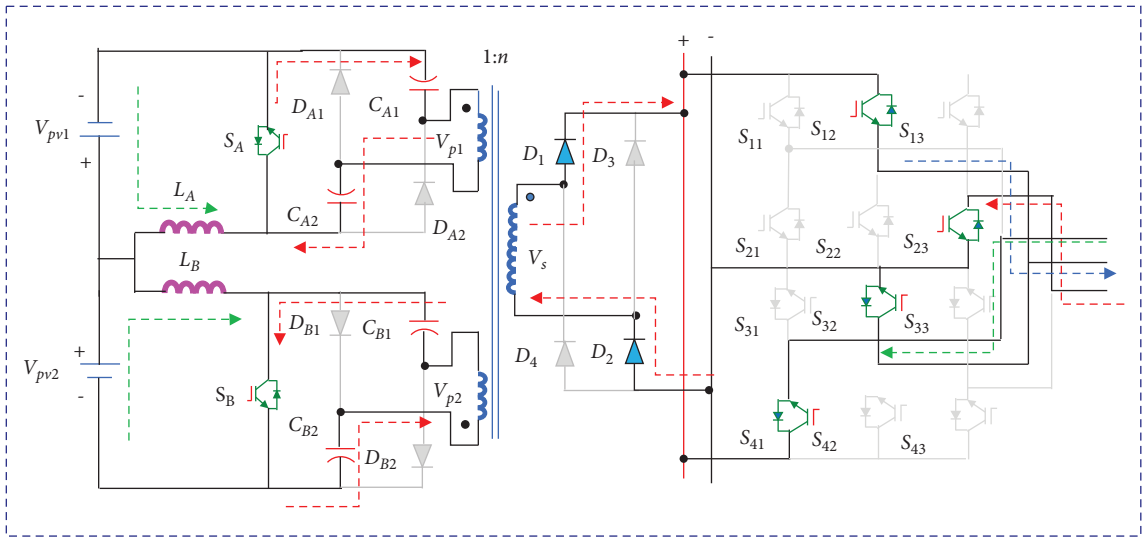


Figure 9: Equivalent circuit of mode 5 operation.

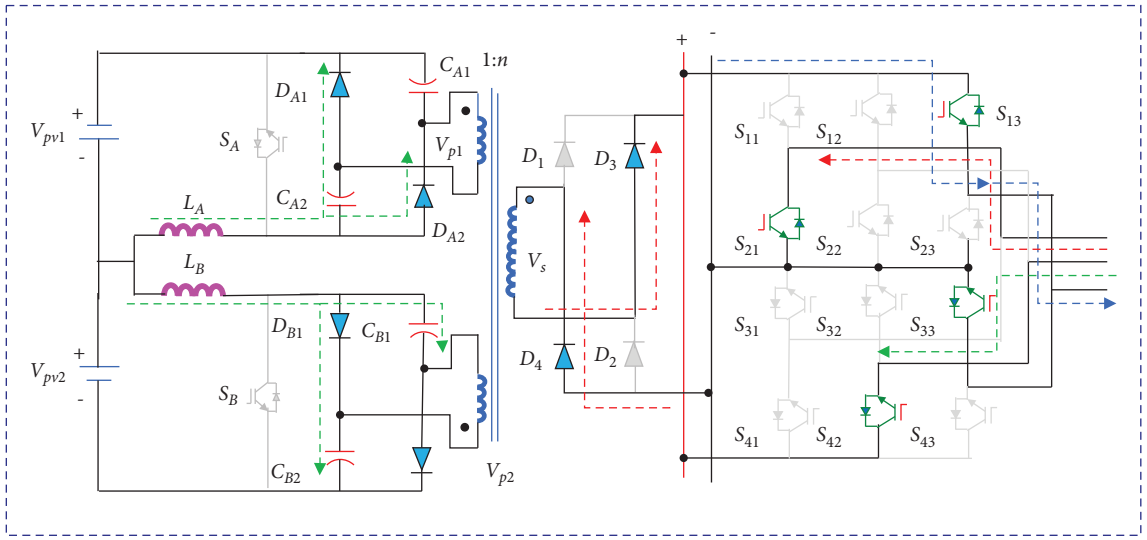
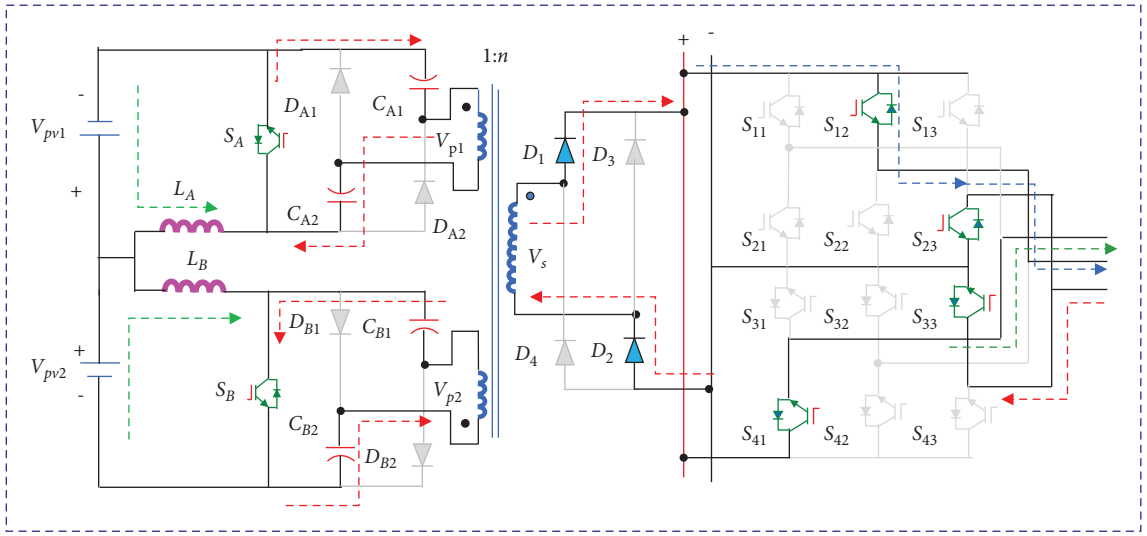
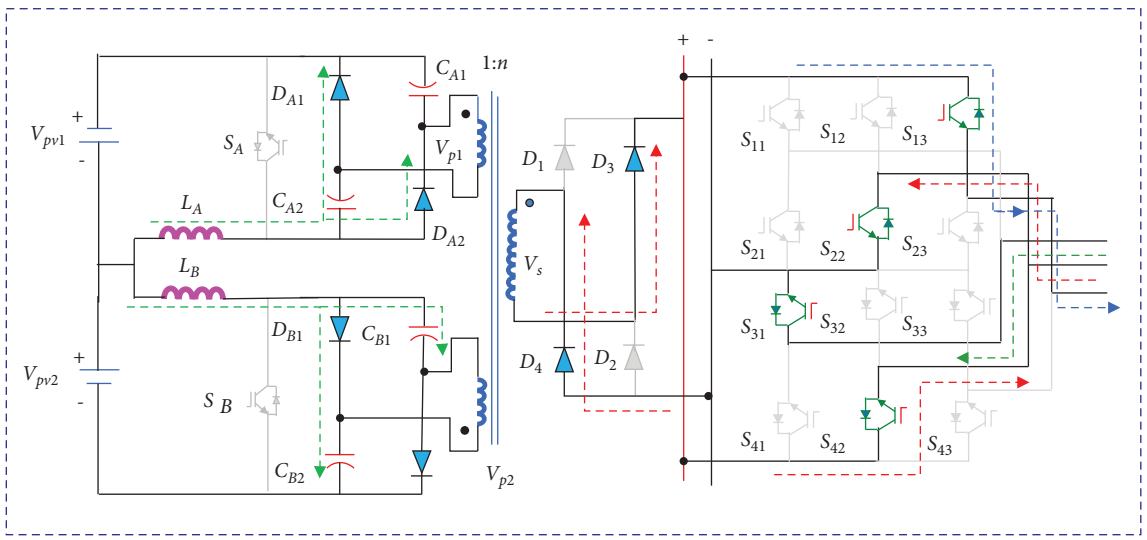


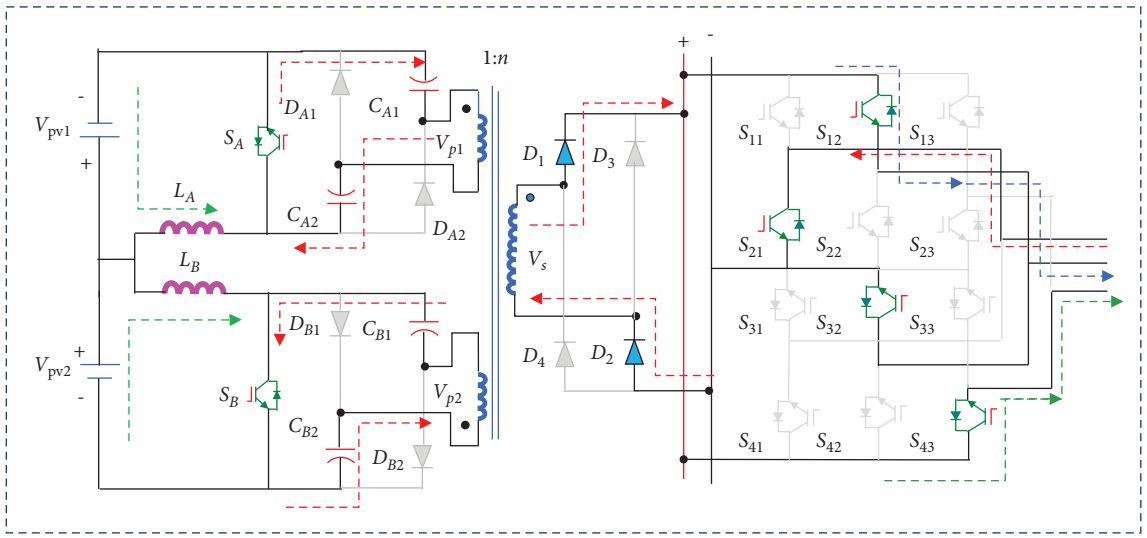
Figure 10: Equivalent circuit of mode 6 operation.



(a)

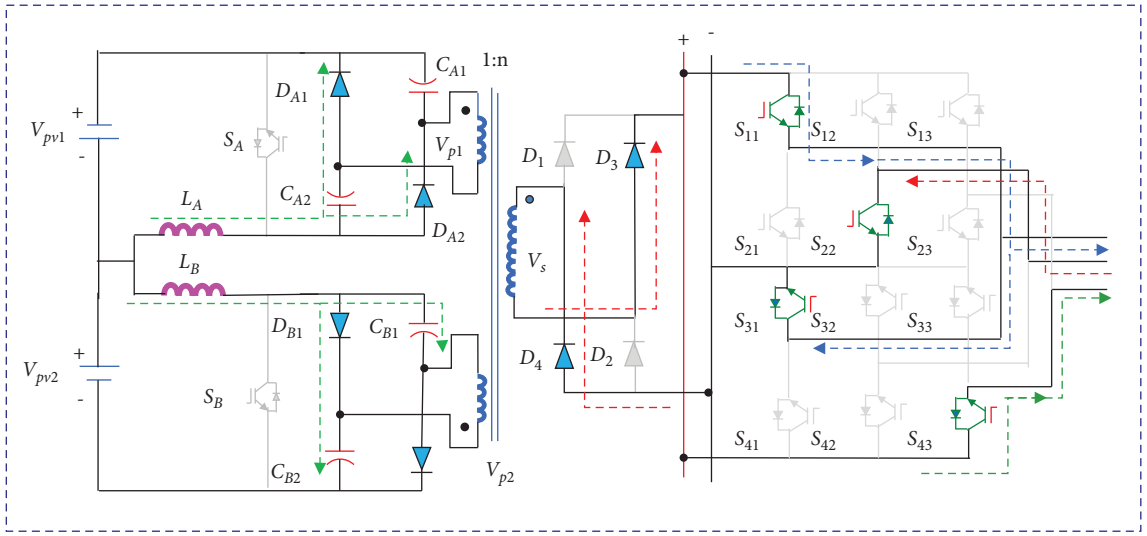


(b)

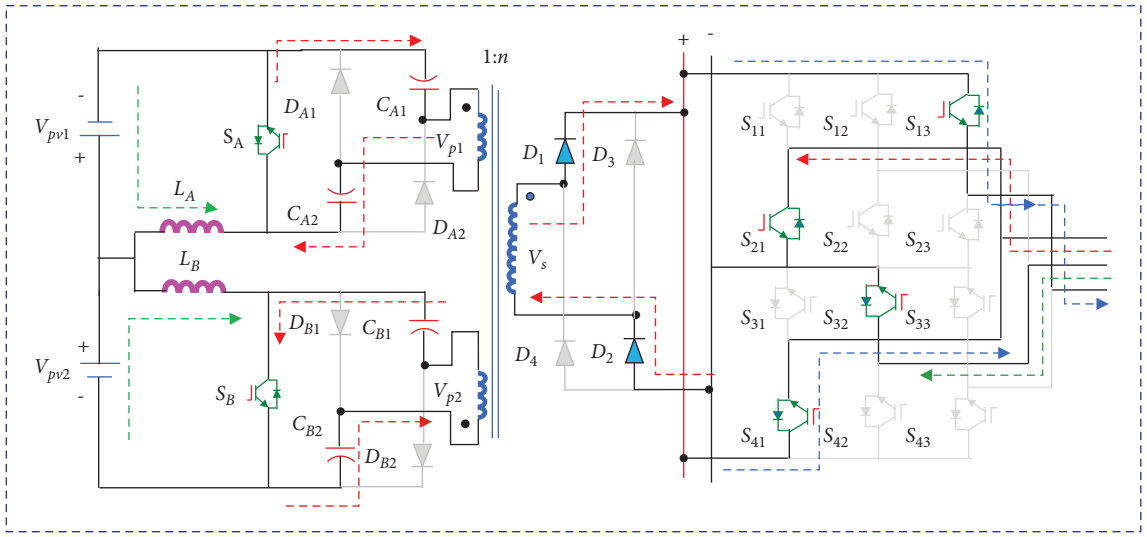


(c)

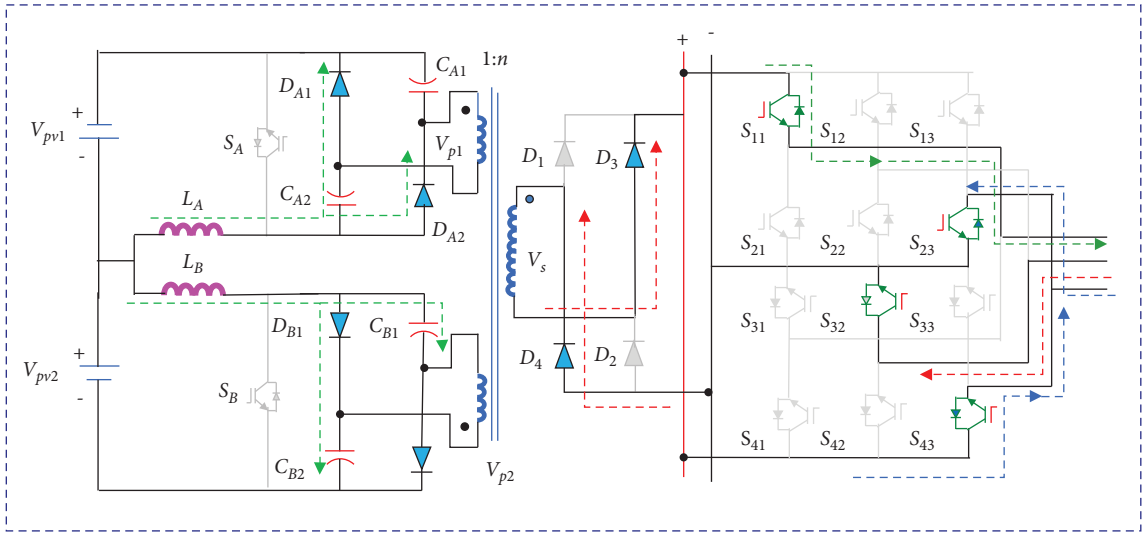
Figure 11: Continued.



(d)



(e)



(f)

FIGURE 11: Equivalent circuit and current flow path for mode 7 to mode 12 operation. Equivalent circuit of (a) mode 7 operation, (b) mode 8 operation, (c) mode 9 operation, (d) mode 10 operation, (e) mode 11 operation, and (f) mode 12 operation.

Table 1: Switching table for the proposed PV-SHAPF.

Modes	MTIIFC		Three-phase three-level SHAPF												V_{inv}		
	S_A	S_B	S_{11}	S_{12}	S_{13}	S_{21}	S_{22}	S_{23}	S_{31}	S_{32}	S_{33}	S_{41}	S_{42}	S_{43}	V_{ab}	V_{bc}	V_{ca}
Mode 1	1	1	0	0	1	0	1	0	0	0	1	1	0	0	$2V_{dc}$	$-V_{dc}$	$-V_{dc}$
Mode 2	0	0	0	1	0	0	0	1	0	1	0	1	0	0	$2V_{dc}$	$-V_{dc}$	V_{dc}
Mode 3	1	1	1	0	0	0	1	0	0	0	1	0	1	0	V_{dc}	V_{dc}	$-2V_{dc}$
Mode 4	0	0	0	1	0	1	0	0	0	0	1	1	0	0	$-V_{dc}$	$2V_{dc}$	$-V_{dc}$
Mode 5	1	1	0	1	0	0	0	1	0	1	0	1	0	0	$-V_{dc}$	$2V_{dc}$	$-V_{dc}$
Mode 6	0	0	0	0	1	1	0	0	0	0	1	0	1	0	$-2V_{dc}$	$-V_{dc}$	V_{dc}
Mode 7	1	1	0	1	0	0	0	1	0	0	1	1	0	0	$2V_{dc}$	V_{dc}	V_{dc}
Mode 8	0	0	0	0	1	0	1	0	1	0	0	0	1	0	$-V_{dc}$	$-V_{dc}$	$2V_{dc}$
Mode 9	1	1	0	1	0	1	0	0	0	0	1	0	0	1	$-V_{dc}$	$-V_{dc}$	$2V_{dc}$
Mode 10	0	0	1	0	0	0	1	0	1	0	0	0	0	1	V_{dc}	$-2V_{dc}$	V_{dc}
Mode 11	1	1	0	0	1	1	0	0	0	1	0	1	0	0	V_{dc}	$-2V_{dc}$	V_{dc}
Mode 12	0	0	1	0	0	0	0	1	0	1	0	0	0	1	$2V_{dc}$	$-V_{dc}$	$-V_{dc}$

After simplification, equation (30) can be rewritten as

$$V_{dc} = \left(\frac{V_{pv1}}{1 - D_{SA}} + \frac{V_{pv2}}{1 - D_{SB}}\right) * 2 * n. \tag{31}$$

The output-to-input ratio of the proposed MTIIFC may be stated as

$$V_{\text{gain}} = \frac{V_{dc}}{V_{\text{in}}} = \frac{V_{dc}}{V_{pv1} + V_{pv2}} = \left(\frac{1}{1 - D_{SA}} + \frac{1}{1 - D_{SB}}\right) * 2 * n, \tag{32}$$

where V_{gain} is the voltage gain of the proposed MTIIFC boost converter, D_{SA} and D_{SB} are the duty cycle of the switches S_A and S_B, n is the turn's ratio of the high-frequency transformer, L_A is the input inductance of port 1, L_B is the input inductance of port B. V_{pv1} is the PV array 1 voltage, V_{pv2} is the PV array 2 voltage, and V_{dc} is the DC bus voltage, V_{LA} and V_{LB} are the voltage across the input inductors L_A and L_B, n is the secondary to primary turns ratio of the high-frequency transformer, i_{pv1} and i_{pv2} are the PV array 1 and 2 currents, respectively. The switching states of the MTIIFC fed PV-SHAPF are listed in Table 1. The comparison of the proposed MTIIFC with the conventional interleaved flyback converter (IFC) is shown in Figure 12.

The comparison shown in Figure 12 has proved the superior performance of the proposed MTIIFC boost converter in terms of boost factor, voltage stress, and current stress of the main switches. The voltage gain of the MTIIFC that has been proposed is eight times higher than that of a regular IFC. The voltage and current stresses imposed by MTIIFC switches are somewhat greater than those imposed by traditional IFC switches.

3. Control Strategy

In this section, the control strategies used in the proposed PV-SHAPF are presented. The SHAPF is operated as a current-controlled source to compensate for the harmonic currents caused by the interconnection of nonlinear load. The two distinct control logics, namely, DC bus voltage control and SHAPF control are used to generate the gating pulses for the MTIIFC boost converter and PV-SHAPF. The control strategy consists of a harmonic detection block, abc-dq transformation, current controller, space vector pulse width modulation (SVPWM), and a fuzzy logic controller (FLC) illustrated in Figure 13.

The SHAPF control scheme generates the reference compensation current by measuring the harmonic order in the load voltage. The SHAPF control strategy utilizes the implemented synchronous rotating reference frame theory to generate the reference current. The abc-dq transformation blocks convert the total harmonic current reference and sensed output current to the dq frame variables by park transformation. A current controller developed with the parallel proportional and integral (PI) and repetitive controllers is adopted to offer better compensating performances under transient and steady-state conditions [19]. The voltage error between the set value of DC bus voltage and actual DC bus voltages is processed through the fuzzy logic controller (FLC) and produces I_{dc}^*. The switching signals for each insulated gate bipolar transistor (IGBT) of the PV-SHAPF are generated using a space vector pulse-width modulation (SVPWM) technique. An FLC is used to regulate the PV-SHAPF's DC bus voltage to a set reference value of 600 V.

The block diagram of the harmonic current reference generating algorithm is shown in the upper part of Figure 13. The harmonic compensation current reference is derived from the load current. Current transducers are used to measure the three-phase load currents. Using a recursive discrete Fourier transform technique, the prominent harmonic current components are extracted from the measured load currents and then put together to generate the harmonic compensation current reference. Only the prominent harmonic components have been extracted and corrected, such as the 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonic currents. This type of selective harmonic compensation makes the proposed PV-SHAPF more adaptable to various scenarios. The harmonic compensation current reference can be expressed as

$$i_{lh} = i_{i5} + i_{i7} + i_{i11} + \cdots\cdots i_{ilk}. \tag{33}$$

The equation used for calculating the k^{th} harmonic current with N number of sampling cycles is

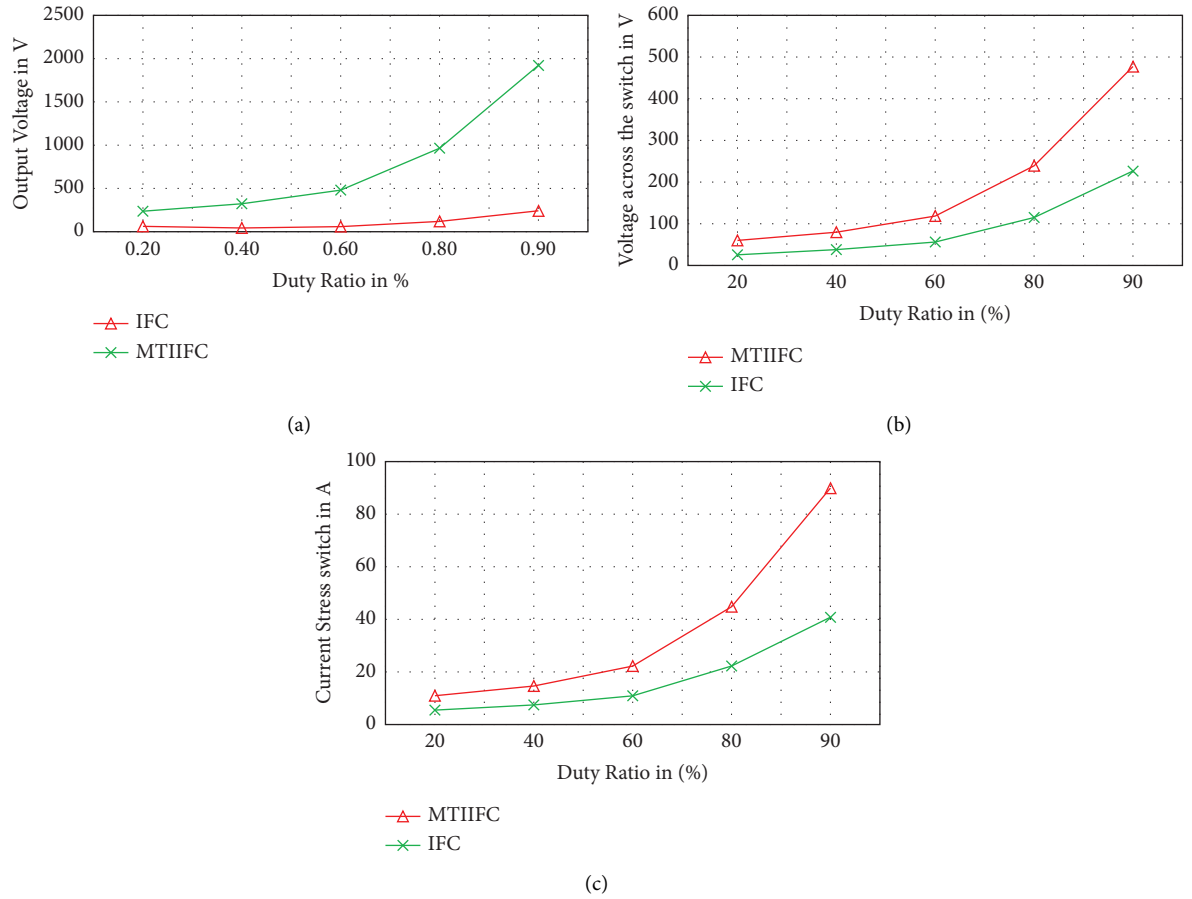


FIGURE 12: Comparison of the proposed MTIIFC with the conventional IFC. (a) Output voltage vs. duty cycle. (b) Voltage stress vs. duty cycle. (c) Current stress vs. duty cycle.

$$H = \frac{i_{lk}}{i_l} = \frac{1 - Z^{-N}}{1 - e^{j2\pi k/N} Z^{-1}}. \tag{34}$$

The voltage error (e) obtained by the comparison of set value of DC bus voltage and actual DC bus voltages can be expressed as follows:

$$e = V_{dc}^{*} - V_{dc}. \tag{35}$$

The synchronous reference frame (SRF) theory is used to achieve the abc-dq transformation. The equations that were utilized to convert the abc variables into the dq variables are shown in equations (36) and (37), respectively.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}, \tag{36}$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix}. \tag{37}$$

4. Simulation Results and Discussion

The suggested parallel-connected multilevel inverter-based shunt active power filter (SHAPF) operated by a photovoltaic (PV) array interfaced modified multi-port interleaved flyback converter (MMPIFC) is modeled and simulated in MATLAB using the power system blockset of the Simulink toolbox. Under perfectly balanced mains voltage circumstances, several simulation results are produced. By executing the designed model in the MATLAB/Simulink environment, the PV array tied proposed MMPIFC is validated. The MMPIFC boost converter fed PV-SHAPF that has been proposed is going to be used to correct for the current harmonics that are present in a three-phase system that operates at 440 V and 50 Hz. Validation of the simulated model is performed both under conditions of constant and dynamic load. The following are the parameters of the models that were simulated: load resistance = 1050 Ω, three-phase load resistance = 240 Ω/480 Ω, supply frequency = 50 Hz, supply rated voltage (line-line) = 400 V, DC bus voltage = 600 V, DC bus capacitor = 1000 μ00B5F, SHAPF capacity = 1000 VA,

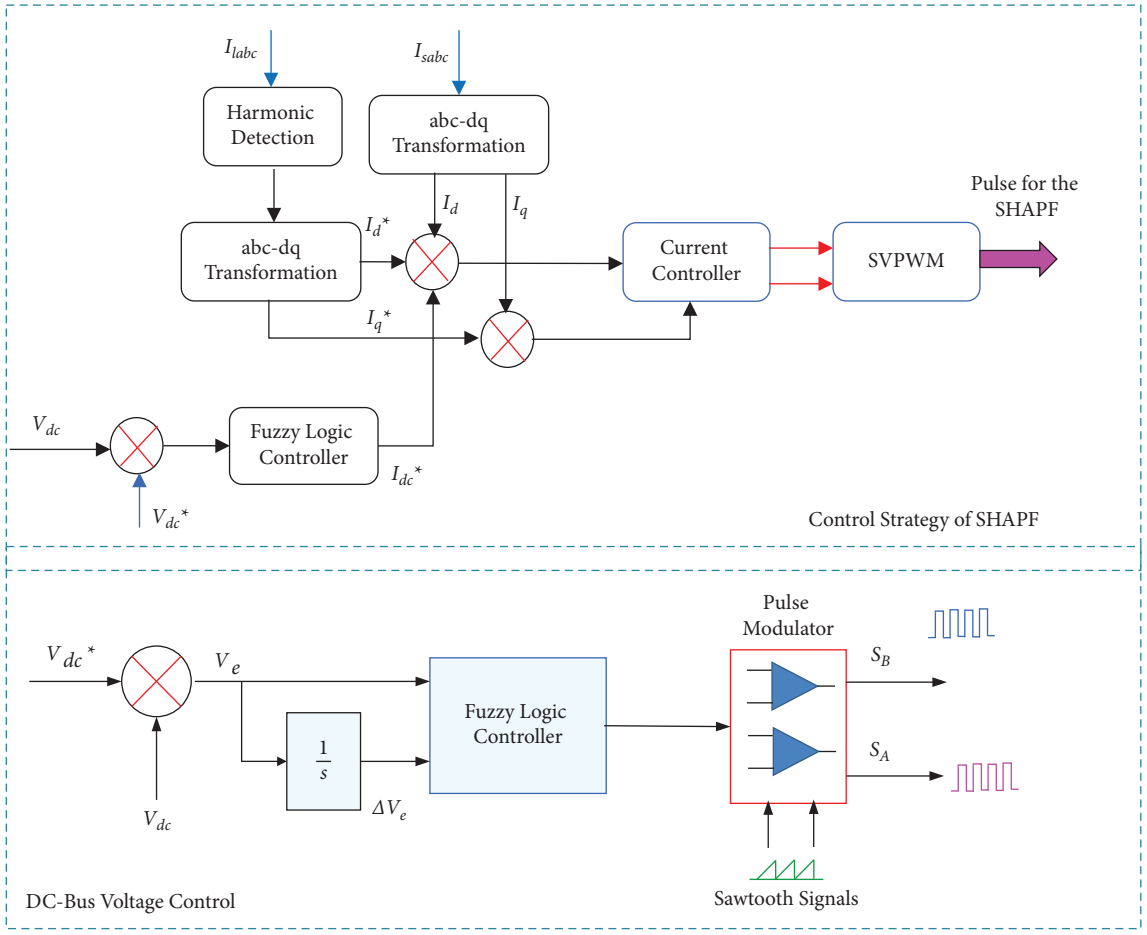


Figure 13: Control strategy of the proposed MTIIFC boost converter and PV-SHAPF.

SHAFP inductance = 1 mH, input inductor L_{Ax} and $L_{Bx} = 0.123\ \mu$H, Capacitor C_{Ax} and $C_{Bx} = 0.265\ \mu$F, MMPIFC boost converter switching frequency = 25 kHz, HF Transformer turns ratio = 2, power rating of HF transformer = 1000 VA, and switches = IGBTs. Table 2 shows system parameters of the simulated model.

4.1. Investigation 1: Appliance of Constant Illumination and Constant Load. The proposed PV-tied MMPIFC operated SHAPF is validated in by applying constant and varying solar illumination to the simulated model of the PV panels. Solar irradiation of 1000 W/m^2 is applied from 0 to 0.3 seconds for the first example, and the associated output voltage is displayed in Figures 14(a)–14(g), respectively. The voltage across the input inductors L_A and L_B, voltage across the capacitors C_{A1}, C_{A2}, $C_{B1,}$ and C_{B2}, voltages of the HF transformer, and DC bus voltage are measured by the voltage measurement and are depicted in Figure 14. The result illustrated in Figure 14(l) proved the ability of the proposed MMPIFC boost converter in step-up the PV voltage. The control loop presented in Section 3 of this manuscript regulated the output voltage of the MMPIFC at 600 V to enhance the compensation performance of the PV-SHAPF. The output voltage of a parallel-connected multilevel inverter, source current before and after the compensation, and injected currents are presented in Figure 15. The cascaded H bridge inverter offered a three-phase three-level voltage with variable magnitude to mitigate the load current harmonics caused by the interconnection of the three-phase uncontrolled rectifier. The voltage gain of the proposed MMPIFC boost converter is observed as 12.5. The duty ratio corresponding to the output voltage of 600 V is 0.7.

In the initial test, the current harmonics mitigation ability is tested by applying constant load and constant illumination to the simulated model of the proposed MMPIFC boost converter operated PV-SHAPF. Harmonics of the current are introduced into the source of the three-phase system by a three-phase uncontrolled diode rectifier that is connected at the source of the three-phase system. The control strategy of SHAPF extracts the fundamental and harmonic components from the source current and generates the reference compensating current required for the mitigation of current harmonics. The total harmonic distortion (THD) spectrum of the source current was measured both before and after the connecting of the proposed MMPIFC boost converter-powered PV-SHAPF, as shown in Figures 16(a) and 16(b), respectively. The total harmonic distortion (THD) content of phase A current is 30.3%, phase B current is 29.93%, and phase C current is also 29.93%. Following the application of current harmonic

Table 2: System parameters of the simulated model.

Description	Value	Description	Value
Rated power	500 W	Switching frequency	25 kHz
PV voltage	12 V	DC bus voltage	600 V
PV short circuit current	28.55 a	DC link capacitor	1000 μF
Supply frequency	50 Hz	Capacitors C_{Ax} and C_{Bx}	0.265 μF
Supply voltage	400 V	Inductors L_A and L_B	0.123 μH
Turns ratio	1 : 2	Power rating of the inverter	1000 VA
Primary 1 and 2 voltage	150 V	Inductor L_1 and L_2	11 μH
Secondary voltage	600 V	Load resistance	240 Ω/480 Ω

adjustment, the THD contents of the source currents were determined to be 2.87%, 2.89%, and 2.80%, respectively. As can be seen in Figure 16, when the proposed MMPIFC boost converter-powered PV-SHAPF injects compensatory current, the total harmonic distortion (THD) content of the source current is reduced to less than 5%. It was proved that the compensating performances of the recommended PV-linked MMPIFC boost converter fed PV-HAPF could be achieved.

4.2. Investigation 2: Appliance of Variable Illumination and Variable Load. The performance of the proposed MMPIFC boost converter fed PV-SHAPF is tested in investigation 2 by applying variable nonlinear load to the simulated three-phase uncontrolled rectifier. Figure 17 shows the results obtained during the investigation 2. The dynamic behavior of the proposed MMPFIC boost converter is tested by applying variable illumination and variable load. Solar illumination is increased from 500 W/m^2 to 1000 W/m^2 in a period of 0.15 seconds; the voltage variation in the PV output that results from this change is depicted in Figure 17(a). In order to provide the output while maintaining the rated voltage, the illumination on another panel is maintained at 1000 W/m^2. To achieve the desired level of voltage regulation at the output of the MMPIFC boost converter, the DC bus voltage controller generates a specific duty ratio. As seen in Figure 17(l), the output voltage is held constant at 600 V.

Initially, a star-connected three-phase loads made up of three 480 resistors are connected to draw a current of 0.75 A from a 400 V (line-line), 50 Hz three-phase supply. The resistance of the star-connected resistive load is lowered to 240 Ω/phase at time $t = 0.15$ sec in order to draw 1.5 A of current from the AC source. The simulated model is run by utilizing the MATLAB Simpower system toolbox. The simulation results of the proposed PV-SHAPF obtained for investigation 2 are shown in Figure 18. The proposed MMPIFC boost converter-powered PV-SHAPF contributes to the compensating current to reduce the source current THD from 30.63% (without compensation) to 2.26% (with compensation). Simulation results shown in Figures 17–19 shows that the proposed PV-SHAPF and its controller are precise enough to allow the real compensating current to track the reference compensating current. The normalized harmonic spectrum of the source current measured for five fundamental cycles is shown in Figures 19(a) and 19(b). THD spectrum of the source current before the compensation is identified as 30.63%, 30.24%, and 30.24%. After the interconnecting of the proposed PV-SHAPF, it is reduced to 2.61%, 2.29%, and 2.26% as shown in Figure 19(b). When compensatory current is injected by the suggested PV-SHAPF, the total harmonic distortion (THD) content of the source current is reduced to less than 5%.

5. Implementation of PV-SHAPF

A prototype test model for 400 V (line-line), 50 Hz three-phase utility has been created to validate the performance of the proposed MMPIFC boost converter-powered PV-SHAPF. The DSP TMS320LF2407 A is used to implement the whole control algorithm, including the reference compensating current calculation technique and the suggested DC bus controller. A three-phase diode bridge rectifier with a resistance of 1050 Ω acts as a nonlinear load for the PV-SHAPF. Figures 20–22 present the experimental results of a prototype model measured through a six-channel digital storage oscilloscope (DSO) and a fluke power quality meter. The PV array 1 voltage, voltage across the voltage doubling capacitor C_{A1}, C_{A2}, C_{B1}, and C_{B2}, input inductor L_A and L_B, transformer input and output voltages, and DC bus voltages are presented in Figure 20.

Figures 22(a) and 22(b) illustrate the harmonic spectrum of the source current measured by the fluke power quality meter. The proposed MMPIFC boost converter-powered PV-SHAPF delivers compensatory current to lower the source current THD from 26.6%, 26.4%, and 26.6% (without compensation) to 2.2%, 2.1%, and 2.2% (with compensation). The experimental results presented in Figures 21 and 22 indicate that the proposed PV-SHAPF and its controller are accurate enough to allow the real compensating current to mirror the reference compensating current.

Table 3 presents the comparison of the proposed MMPIFC boost converter-powered PV-SHAPF with the other conventional converter-powered PV-SHAPF. The simulation and experimental results presented in Table 3 have proved the performance of the proposed MMPIFC boost converter-powered PV-SHAPF in mitigating the source current harmonics. The photography of the experimental model is shown in Figure 23.

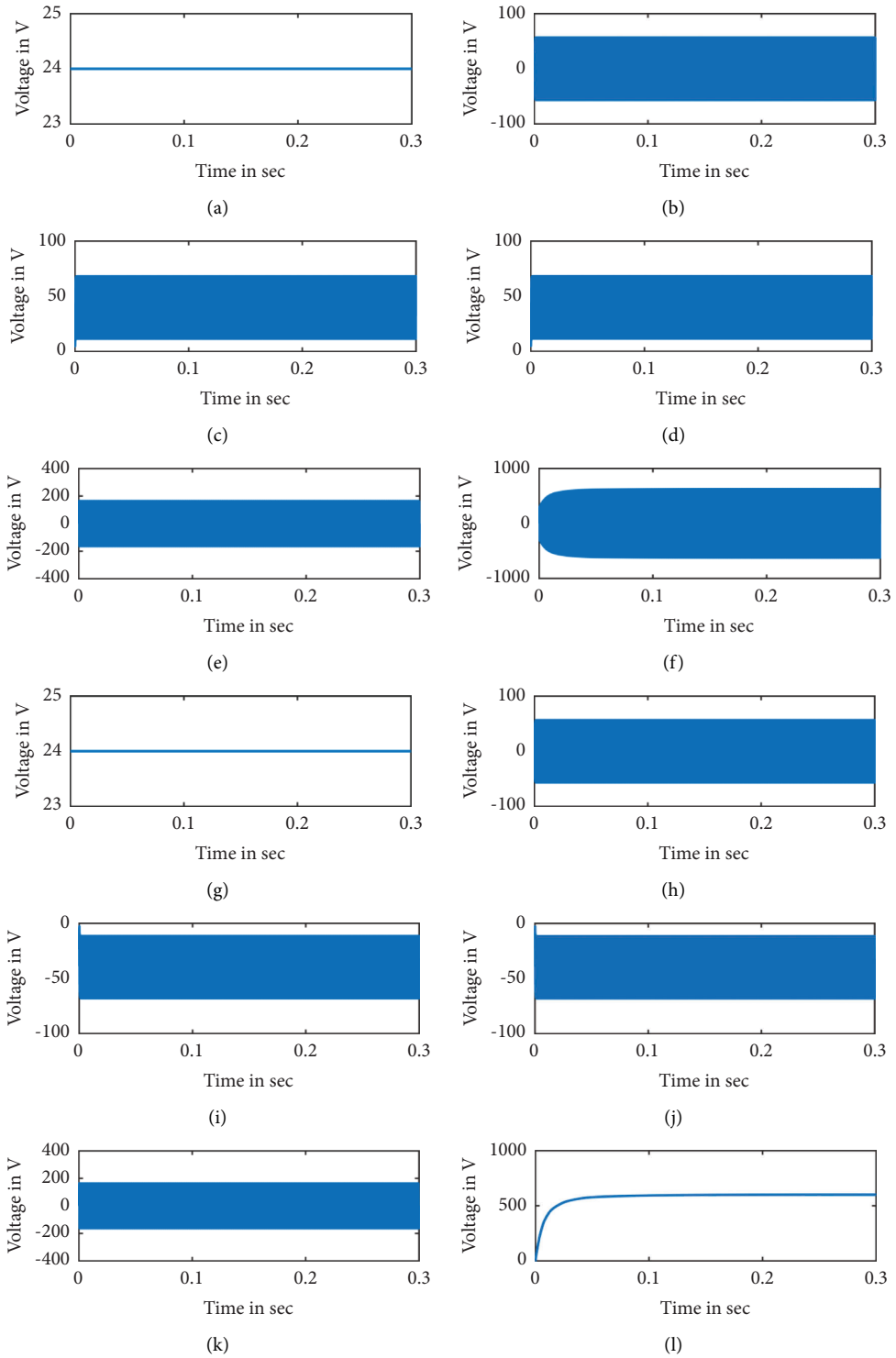


FIGURE 14: Simulation results of the proposed MMPIFC boost converter for investigation 1. (a) PV array 1 voltage. (b) Voltage across the input inductor L_A. (c) Voltage across the capacitor C_{A1}. (d) Voltage across the capacitor C_{A2}. (e) Primary 1 voltage HF transformer. (f) Secondary voltage of HF transformer. (g) PV array 2 voltage. (h) Voltage across the input inductor L_B. (i) Voltage across the capacitor C_{B1}. (j) Voltage across the capacitor C_{B2}. (k) Primary 2 voltage HF transformer. (l) DC bus voltage.

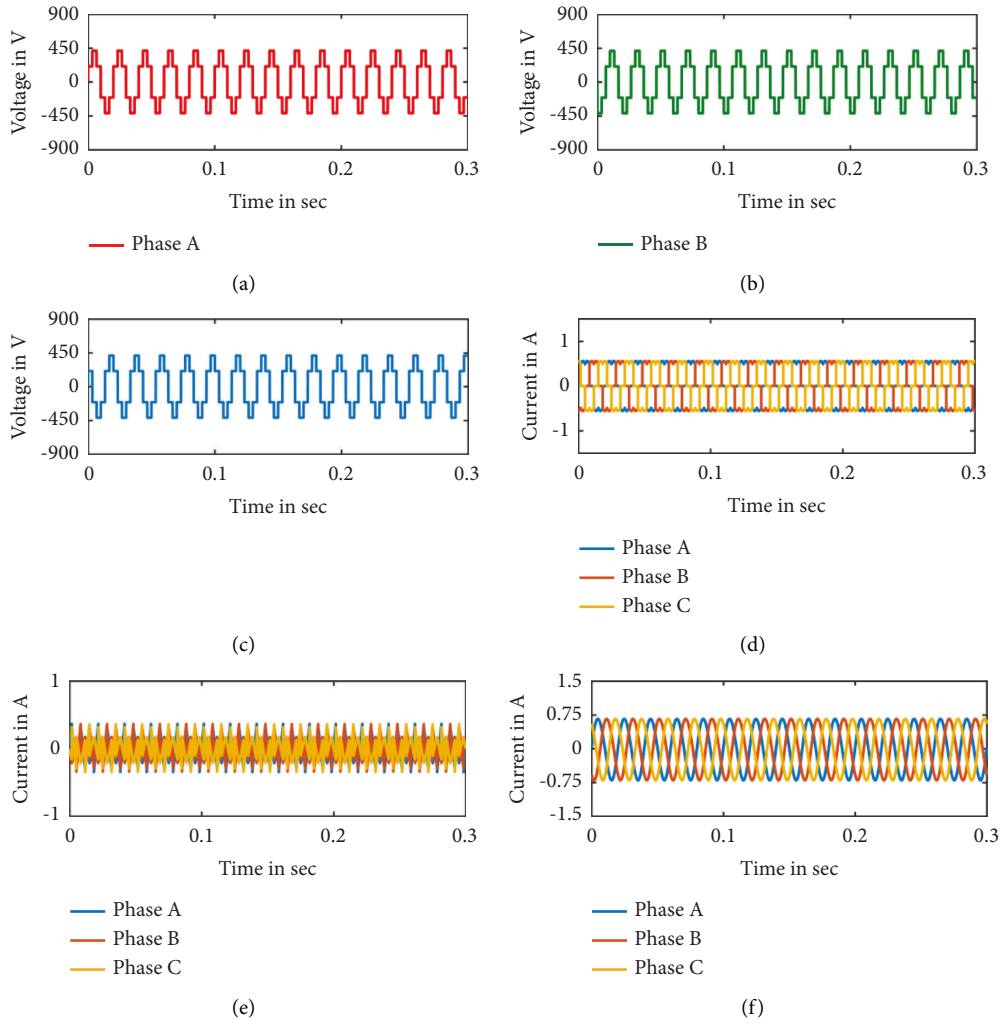


Figure 15: Simulation results proposed MMPIFC boost converter operated PV-SHAPF under constant load. (a) Phase A voltage of TPTL inverter. (b) Phase B voltage of TPTL inverter. (c) Phase C voltage of TPTL inverter. (d) Source current before compensation. (e) Injected current. (f) Source current after compensation.

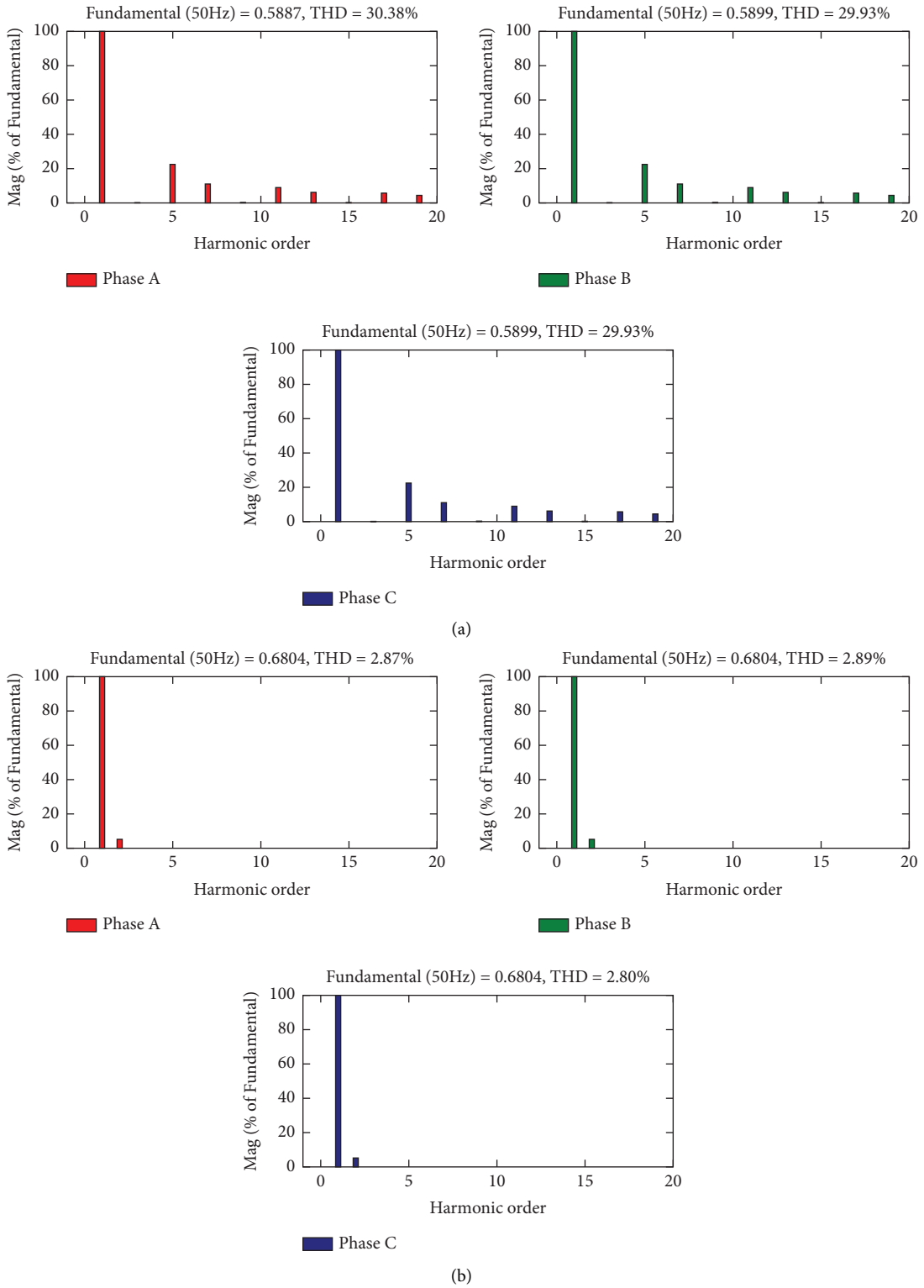


Figure 16: Source current THD spectrum before and after the interconnection of the proposed MMPIFC boost converter fed PV-SHAPF. (a) THD of source current before compensation. (b) THD of source current after compensation.

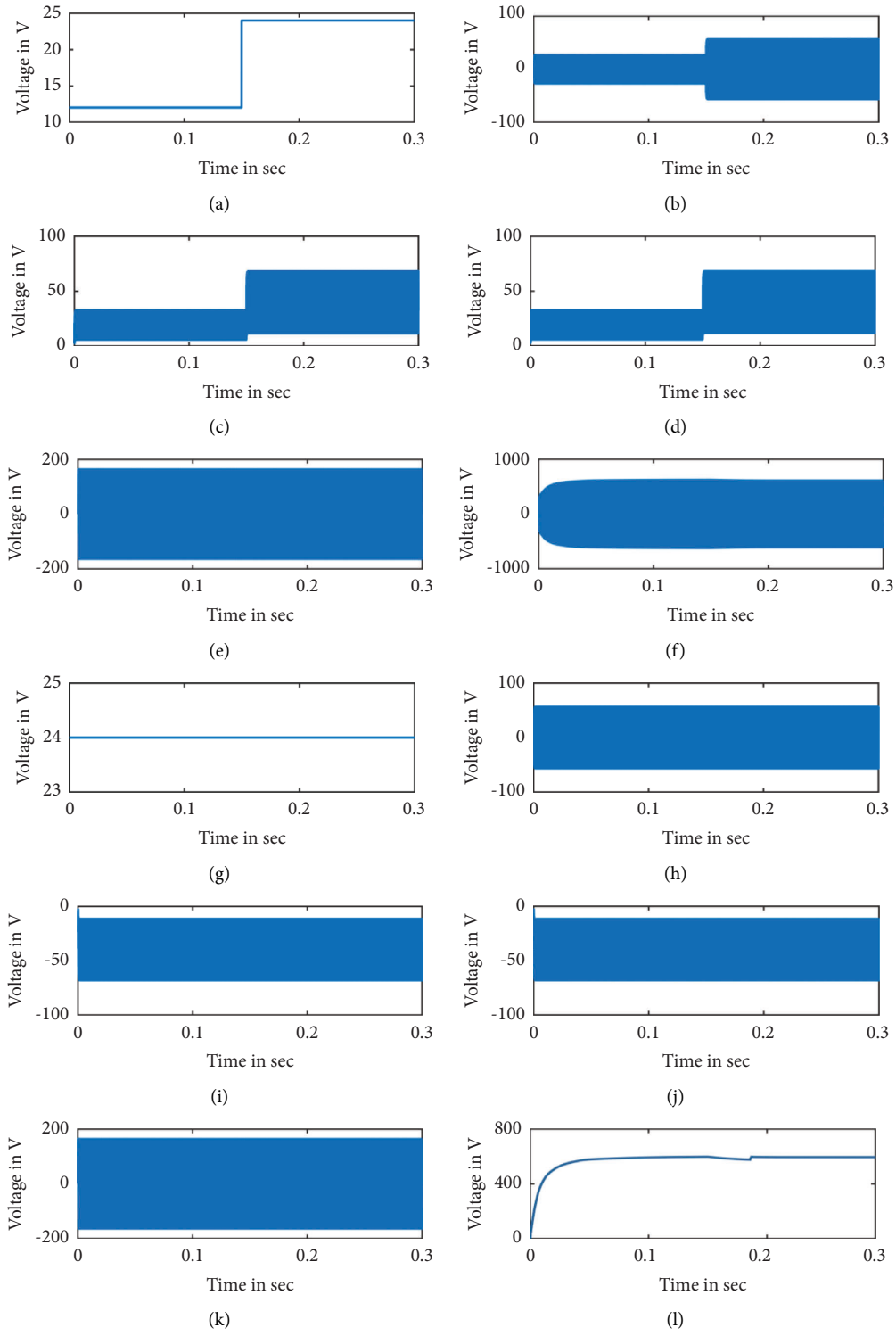


Figure 17: Simulation results of the proposed MMPIFC boost converter for investigation 2. (a) PV array 1 voltage. (b) voltage across the input inductor LA. (c) Voltage across capacitor CA1. (d) Voltage across capacitor CA2. (e) Primary 1 voltage HF transformer. (f) Secondary voltage of HF transformer. (g) PV array 2 voltage. (h) Voltage across the input inductor LB. (i) Voltage across capacitor CB1. (j) Voltage across capacitor CB2. (k) Primary 2 voltage HF transformer. (l) DC bus voltage.

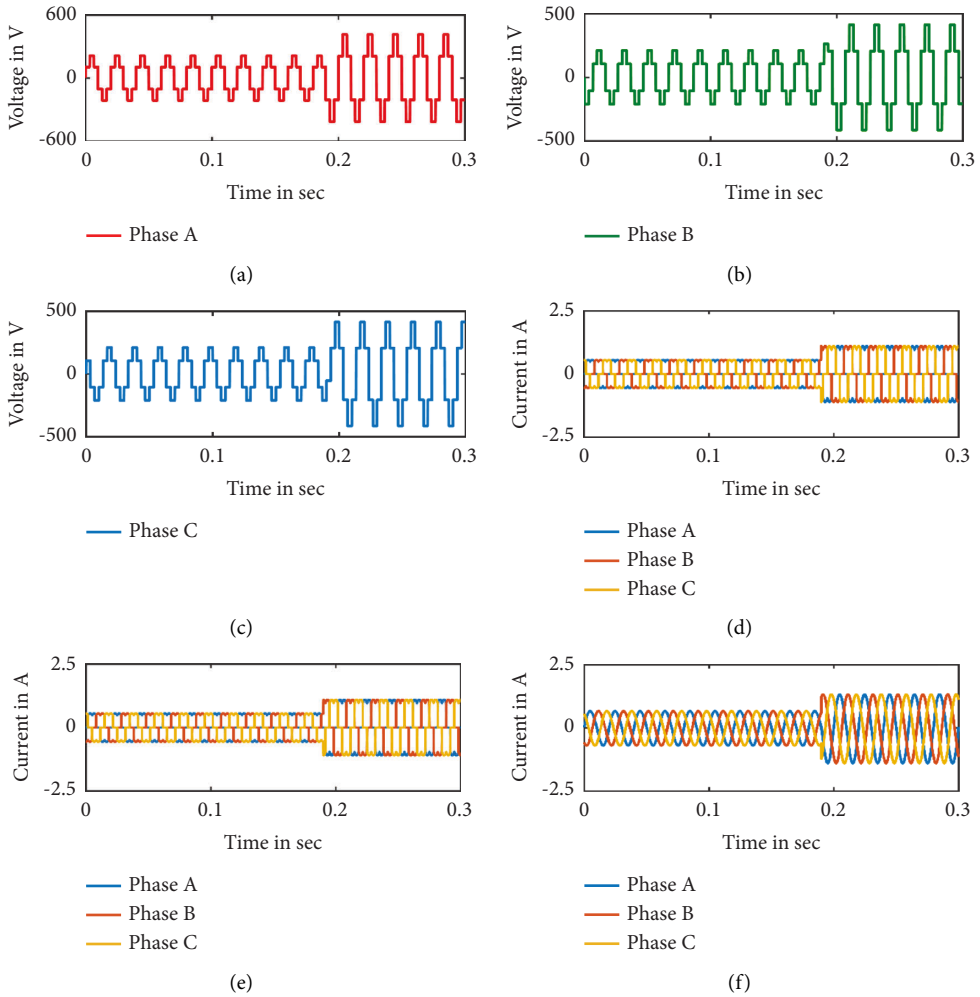


Figure 18: Simulation results proposed MMPIFC boost converter operated PV-SHAPF under variable load. (a) Phase A voltage of TPTL inverter. (b) Phase B voltage of TPTL inverter. (c) Phase C voltage of TPTL inverter. (d) Source current before compensation. (e) Injected current. (f) Source current after compensation.

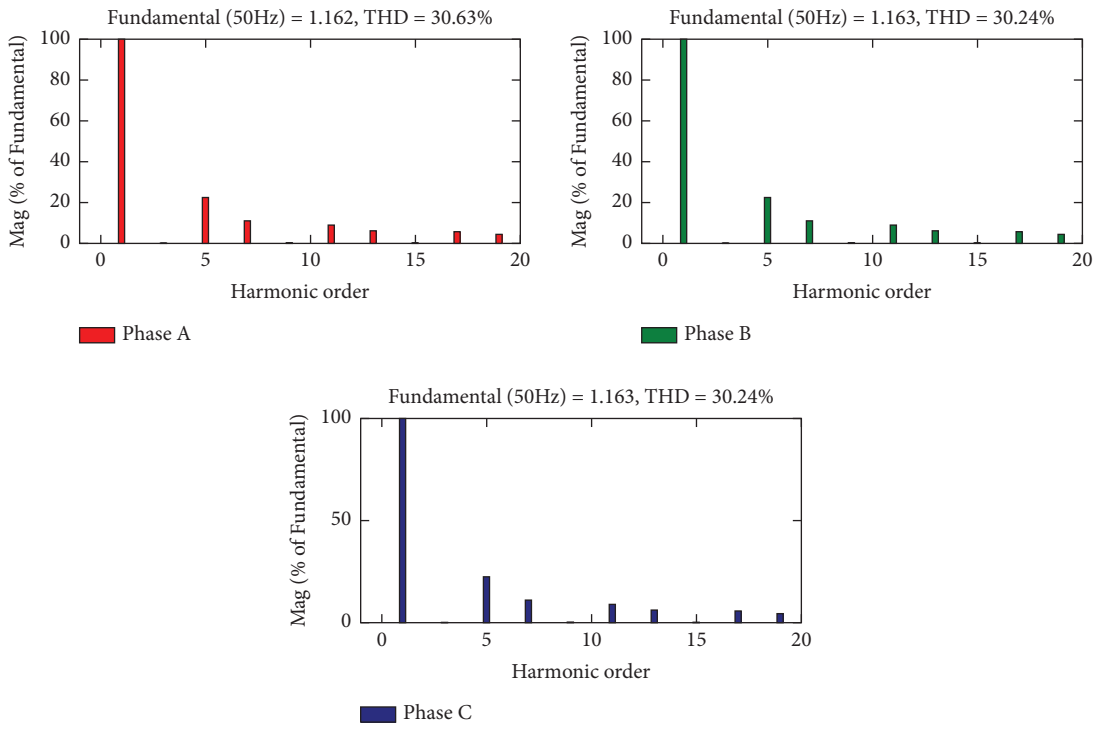
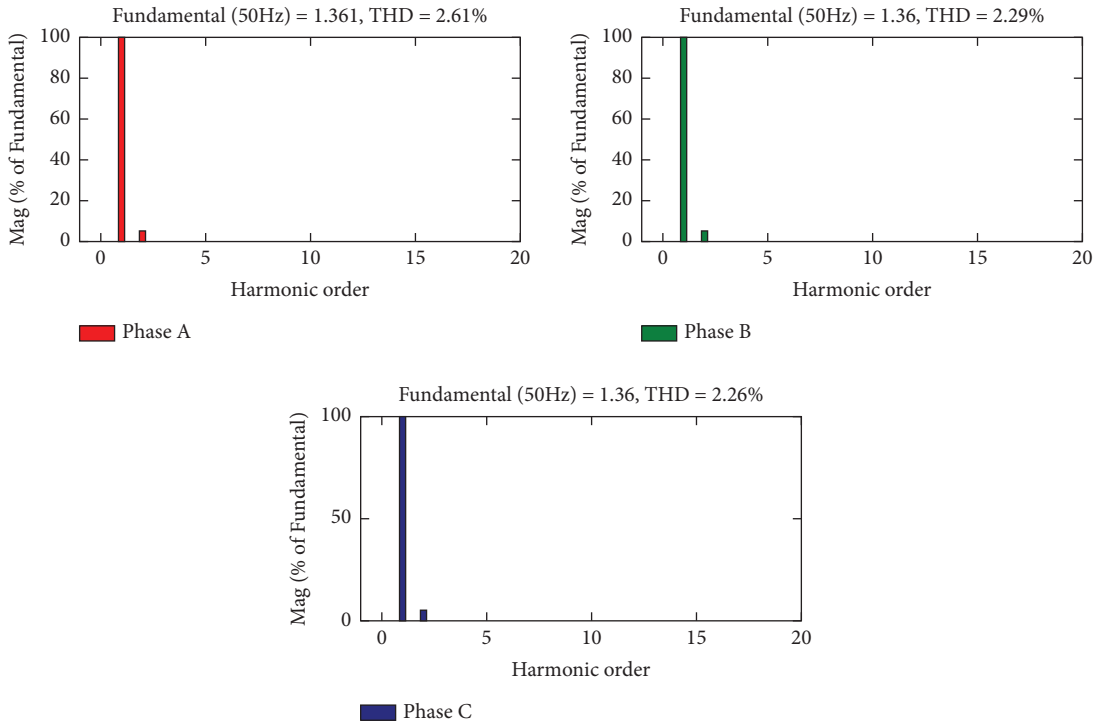


Figure 19: Continued.



(b)

Figure 19: THD spectrum of the source current before and after interconnection of PV-SHAPF. (a) Spectrum of THD of the source current prior to the connecting of PV -SHAPF. (b) After the connecting of PV-SHAPF, the THD spectrum of the source current.

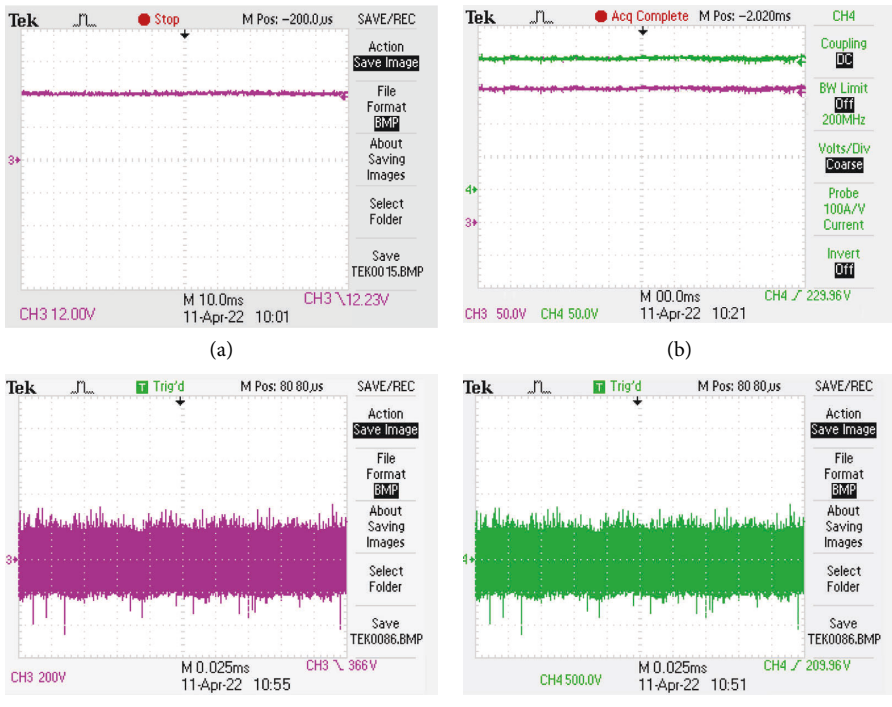


Figure 20: Continued.

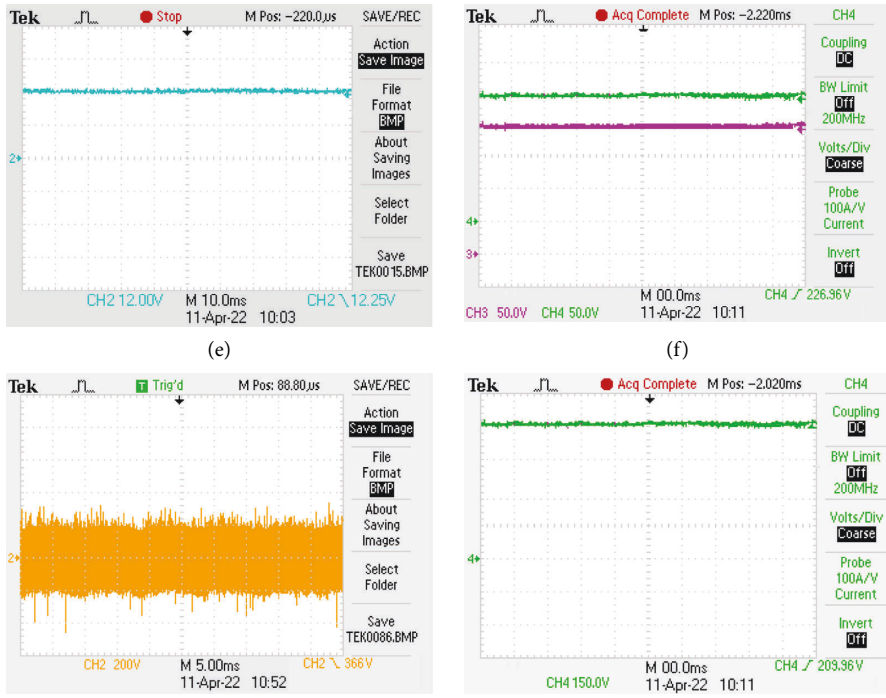


Figure 20: Experimental results of the proposed MMPIFC boost converter prototype model. (a) PV array 1 voltage. (b) voltage across capacitors C_{A1} and C_{A2}. (c) Primary 1 voltage. (d) Secondary voltage. (e) PV array 2 voltage. (f) Voltage across capacitors C_{B1} and C_{B2}. (g) Primary 2 voltage. (h) DC bus voltage.

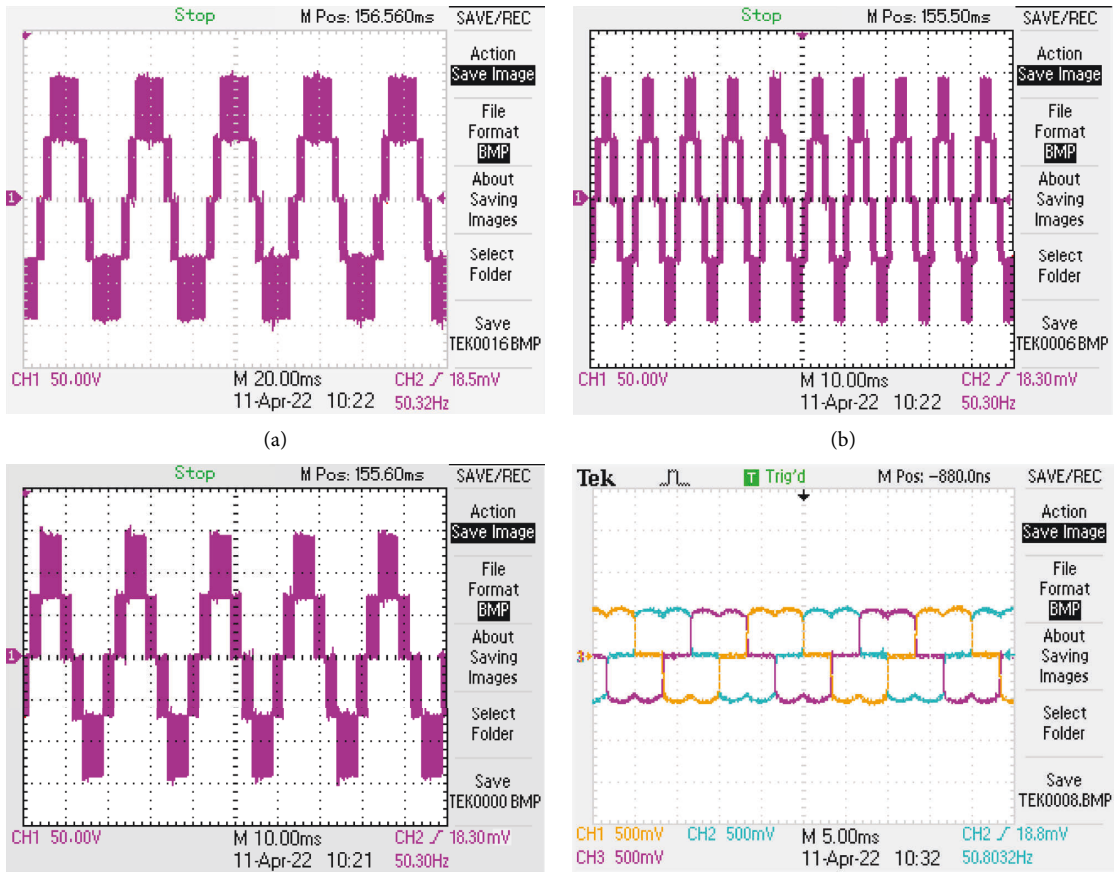
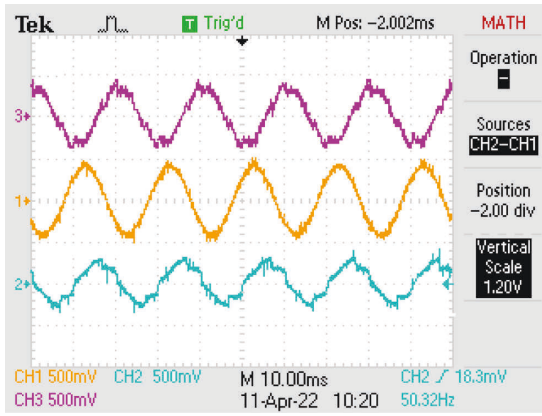
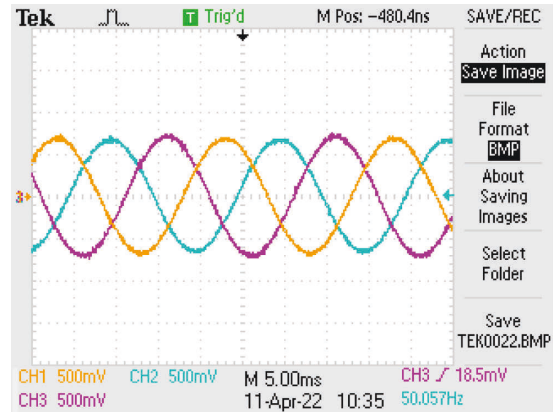


Figure 21: Continued.

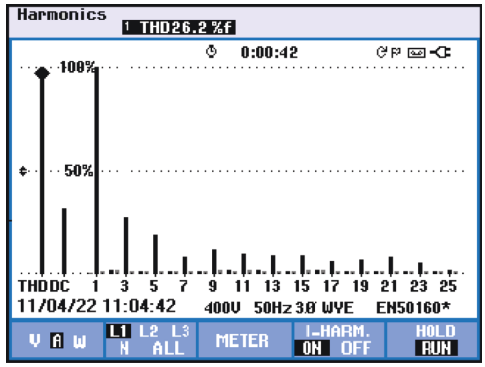


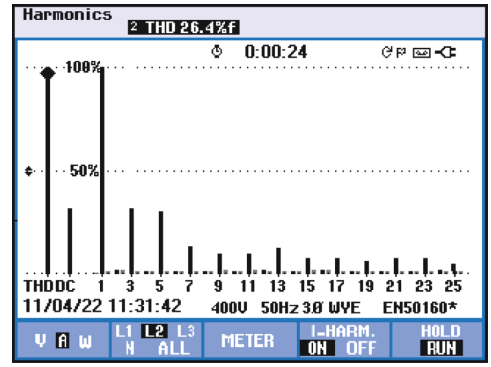
(e)

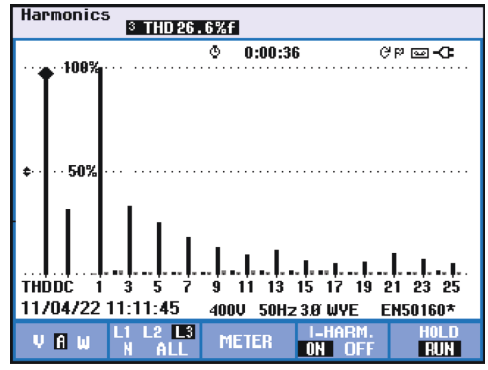


(f)

Figure 21: Experimental results of the proposed PV-SHAPF prototype model. (a) TPTL phase A output voltage. (b) TPTL phase B output voltage. (c) TPTL phase C output voltage. (d) Source current before compensation. (e) Source current, injected current, and load current. (f) Source current after compensation.

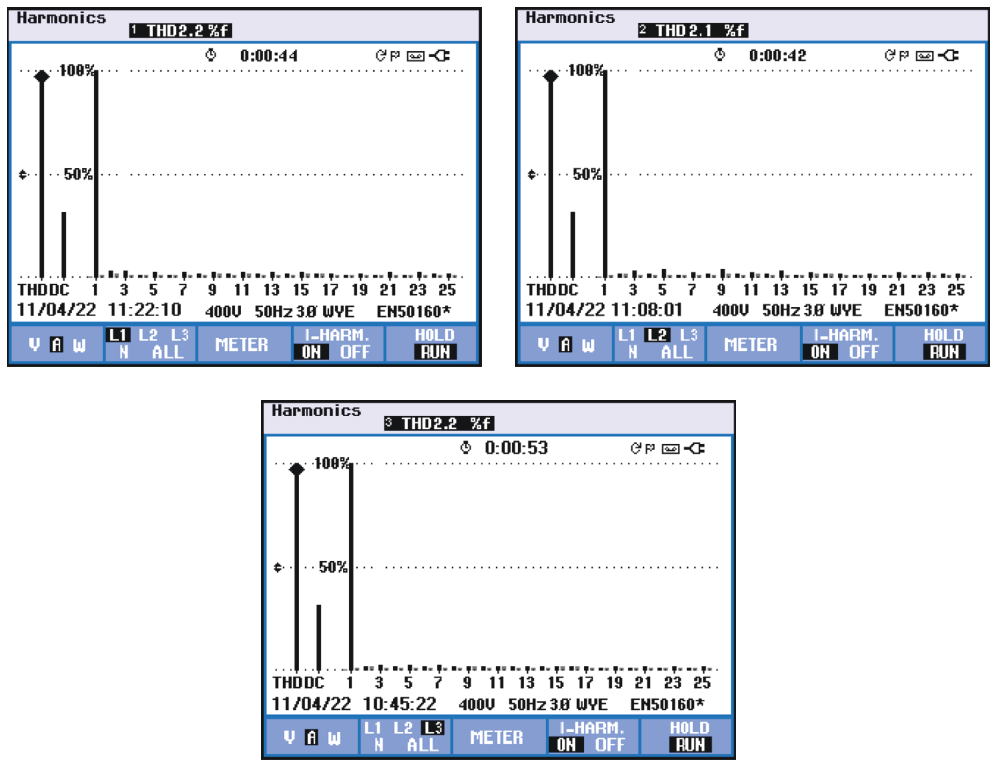






(a)

Figure 22: Continued.



(b)

Figure 22: The THD spectrum of the source current before and after the hookup of the PV-SHAPF prototype mode. (a) THD of source current before the compensation. (b) THD of source current after the compensation.

Table 3: Performance of the proposed MMPIFC boost converter-powered PV-SHAPF.

Investigation	Simulation investigation						Experimental investigation					
	Without SHAPF (THD in %)			With SHAPF (THD in %)			Without PV-SHAPF (THD in %)			With PV-SHAPF (THD in %)		
	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C
Investigation 1	30.38	29.93	29.93	2.87	2.89	2.80	26.20	26.40	26.60	2.20	2.10	2.20
Investigation 2	30.63	30.24	30.24	2.61	2.21	2.26	28.10	28.40	24.70	2.40	2.30	2.60

Phase	SHAPF [2]		PV-SHAPF [4]		MLISHAPF [20]		Proposed PV-MLISHAPF	
	Without SHAPF (THD in %)	With SHAPF (THD in %)	Without SHAPF (THD in %)	With SHAPF (THD in %)	Without SHAPF (THD in %)	With SHAPF (THD in %)	Without SHAPF (THD in %)	With SHAPF (THD in %)
Phase A	30.63	8.67	30.63	7.25	30.63	5.36	30.63	2.61
Phase B	30.24	8.97	30.24	7.56	30.24	5.82	30.24	2.21
Phase C	30.24	8.45	30.24	7.85	30.24	5.76	30.24	2.26

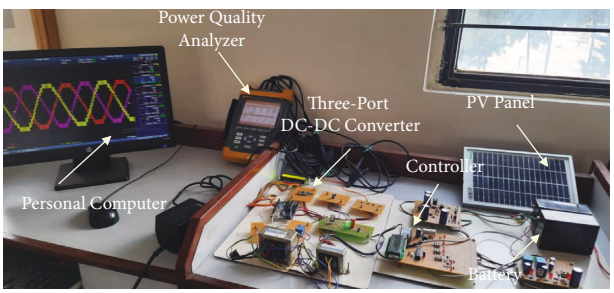


Figure 23: Photography of the experimental model.

6. Conclusion

In order to lessen the impact that current harmonics have the three-phase power distribution system, the authors of this paper propose a novel MMPIFC boost converter that is driven by PV-SHAPF. The power quality problems that are being caused by current harmonics in the power distribution network can be solved by implementing the suggested MMPIFC boost converter-powered PV-SHAPF. This solution also works for the SHAPF that is powered by the traditional boost converters. In order to demonstrate that they are superior in reducing the source current harmonics, the performance of the system is assessed for two separate investigations. The MMPIFC boost converter offered a voltage gain of 42 in relation to the input voltage of 48 V. The THD content of the source current was brought down to less than 2.1% thanks to an efficient decrease brought about by the synchronous reference frame theory-based control method and the space vector modulation scheme. It is less than what is permitted by the IEEE standard 519, which has been met. The experimental findings gleaned from prototype models developed in the laboratory are consistent with the viability of the proposed implementation. Additionally, the functionality of the system can be improved by switching out the fuzzy controller for an artificial neural network (ANN), adaptive neuro-fuzzy, or genetic algorithm. This will result in a higher level of overall performance.

Data Availability

No new data were created or analyzed in this study.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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