Hindawi
International Transactions on Electrical Energy Systems
Volume 2022, Article ID 1870727, 24 pages
https://doi.org/10.1155/2022/1870727

Research Article

Novel Modified High Step-Up DC/DC Converters with Reduced Switch Voltage Stress

Lingling Liu and Donghui Li

Tianjin University, Tianjin 300072, China

Correspondence should be addressed to Lingling Liu; 1016203017@tju.edu.cn

Received 11 January 2022; Revised 2 August 2022; Accepted 23 August 2022; Published 27 September 2022

Academic Editor: Faroque Azam

This paper presents the improved switched inductor unit and new step-up DC/DC converters with reduced switch voltage stress and high voltage gain. The proposed switching-inductor unit is composed of 1 switch, 2 diodes, and 2 inductors, which can realize the step-up function. Through comparison, the better topology is selected from the proposed converters, which is named the double-switch high step-up (DS-HS) converter. The CCM operating principles and voltage gain of the DS-HS converter are analyzed. Then, the influences of nonideal components, efficiency analysis, small signal modeling and control, and design criteria of components are discussed. The comparison of the converters is given, and the loss of the DS-HS converter is lower through theoretical derivation, which shows that the DS-HS converter has the advantages of high voltage gain, low voltage stress, and high efficiency. Finally, in order to verify the effectiveness of the DS-HS converter, simulation and experimental results are given, and the efficiency of the DS-HS converter can reach 96.15%.

1. Introduction

In recent years, the world's attention to the adhibition of renewable energy for power generation has greatly increased. Photovoltaic cells and fuel cells are sources of renewable energy power generation and have received sufficient attention. Because of the low output voltage of these renewable energy sources, it is not enough to be used in many applications [1]. Therefore, it is necessary to need an efficient and high boost DC/DC converter to achieve step-up. High-boost DC/DC converters can be applied to photovoltaic and fuel cell energy conversion systems, DC microgrids, automobiles, uninterruptible power supplies, high-intensity light ballasts, LEDs, and hybrid vehicles [2, 3]. Since the output DC voltage of solar photovoltaic power generation and fuel cell power generation is low, generally less than 50 V, the low DC voltage needs to be boosted to the 380 V DC bus voltage of input of the grid-connected full-bridge inverter. Therefore, the nonisolated high-gain DC converter is an important link to ensure the normal operation of the entire photovoltaic power generation system and fuel cell power generation system and has a very important impact on the entire system.

For the classic boost converter [4], theoretically, it can achieve high voltage gain only as the duty cycle approaches 1. Recently, a number of DC/DC converters on account of several enhancement techniques have been proposed in [5]. Isolated step-up DC/DC converters can easily achieve high boost through transformers, such as H-bridge, push-pull, and others. However, due to the need for high-frequency transformers and supplementary circuits to handle leakage inductance energy [6, 7], these converters are bulky, large, and expensive. In addition, due to transformer leakage inductance, the voltage stresses of active switches on these converters are high. Therefore, additional energy regeneration technology and voltage clamping technology are needed to recover the leakage energy and reduce the voltage stress of the active switches [8, 9]. The boost DC/DC converters based on coupled inductors can achieve high step-up; however, additional voltage clamping techniques and input filters are needed to reduce ripple and leakage inductance energy recovery solutions, which lead to higher costs. In addition, authors in [10–12] also introduce additional losses related to the clamping circuit. However, these topologies are complicated, and the gain factor depends on the coupling

coefficient of the coupled inductor. The LLC resonant converter uses the principle of soft switching to realize zero-voltage (zero-current) switching of the switching device, which greatly reduces the switching loss of the converter and further improves the switching frequency of the converter [13–15]. The LLC resonant converter has the advantages of parasitic parameter compatibility and good soft switching performance, but it also has a certain complexity, and its energy transfer is realized by using a complex resonant circuit. The cascaded and secondary boost converters can be other ways to the problem, but high-voltage devices are still required, and the switch voltage stress is equal to the output voltage. The cascade of two or more DC/DC converter topologies brings about complex circuits and increased costs. Because the voltage gain is highly nonlinear, two or more switches are required to be synchronized [9, 16–18], and the control is complicated.

In order to solve the problems of the aforementioned converters, switched inductors (SIs), mixed switched inductors and capacitors, interleaved front-end structures, and multiplier-based converters are possible approaches recently [19–23]. However, multiple power levels are applied in many cases, and the voltage stress of the active switch is too high or even equal to the output voltage. In addition, using many multipliers will increase the measure and cost of the system. For the sake of reducing the voltage and current stress on the switch and obtaining a higher boost voltage gain, the DC-DC converters are proposed in [24, 25], when the duty cycle is not high. However, the converters in [23, 24] require a lot of reactive components and achieve high boost through the cascade. The geometric structure method is proposed in [26], which is a method to develop the DC conversion topology by constructing the geometric structure. However, the constructed geometric structure is only for a certain part of the topology, not for the whole topology, so it still cannot be unified in the character analysis, and the analysis process is too cumbersome.

In this paper, the improved switching-inductor unit and new high step-up DC-DC converters with reduced switch voltage stress and high voltage gain are proposed. Then, the better topology is selected from the proposed converters by comparison, named the double-switch high step-up (DS-HS) converter, in Section 2. Section 3 analyzes the CCM operating principles and voltage gain of the DS-HS converter so as to verify the accuracy of the DS-HS converter in Section 2. The impact of nonideal components on the output voltage and efficiency is analyzed in Section 4. A comparison with existing converters is shown in Section 5. Section 6 provides the design criteria for components. Small-signal models and control schemes are listed in Section 7. Sections 8 and 9 deal with the simulation and experimental results of the DS-HS converter. At last, Section 10 draws conclusions.

2. Proposed Switching-Inductor Unit and Step-Up Converters

Section 2 proposes the improved switching-inductor unit and new high step-up DC/DC converters with reduced switch voltage stress and high voltage gain, and the better boost converter is selected from the proposed converters.

2.1. Proposed Switching-Inductor Unit. Based on the switching-inductor unit in [16], a modified switching-inductor unit is proposed. The switching-inductor units and operating conditions are shown in Figure 1. Figure 1(a) is the existing switching-inductor unit, consisting of 3 diodes and 2 inductors. By replacing a diode in Figure 1(a) with a switch and changing the position of the switch, it helps to share the voltage stress on this branch of the switches, when combining the step-up DC converters. The improved switching-inductor unit of Figure 1(b) originated from Figure 1(a) is proposed, consisting of 2 diodes, 1 switch, and 2 inductors. Figures 1(c) and 1(d) are the operating conditions of the improved switching-inductor unit. The inductors are charged in Figure 1(c), when the switch is in the conductive state. The inductors are discharged in Figure 1(d), when the switch is turned off. Simultaneously, the current flows in the direction of the arrow in Figures 1(c) and 1(d).

2.2. Proposed High Step-Up Converters. Combining the proposed switching-inductor unit with the existing converters [27], four new step-up DC/DC converters with reduced switch voltage stress and high voltage gain are proposed in Figure 2. On the branch of the switches, two switches S1 and S2 can share the voltage stress with each other, as shown in Figure 2 marked with a red box, so the voltage stress of the switch can be much lower, compared with the DC/DC converter with only one switch in the branch. The characteristics of four proposed DC/DC converters are shown in Table 1, including voltage gain, voltage stress of switch, maximum of diode voltage, and the number of components. From Table 1, we can see that the converters of Figures 2(a)–2(d) have the same number of components. Compared with Figures 2(b) and 2(d), the converters in Figures 2(a) and 2(c) have higher voltage gain and lower voltage stress of the switches and diodes. The input current of the converters in Figures 2(a) and 2(d) is not pulsating but that of the DC/DC converters in Figures 2(b) and 2(c) is the opposite. By filtering the circuit with lower voltage stress and higher voltage gain, the converters in Figures 2(a) and 2(c) can be filtered out. In addition, the input current of the DC converter in Figure 2(a) is not pulsating, so its input current has less disturbance to the input power. All in all, by comparison, the proposed converter in Figure 2(a) is better, and the detailed analysis in the following section is carried out on the converter in Figure 2(a).

3. Operating Principle of the Proposed Converter

This section discusses the operating principles and voltage gain of the better converter in Figure 2(a), named the double-switch high step-up (DS-HS) converter. The continuous-conduction mode (CCM) for the DS-HS converter is shown in Figure 3, where D is the duty ratio, and T_S is a whole cycle. DT_S represents the time that the switch is turned

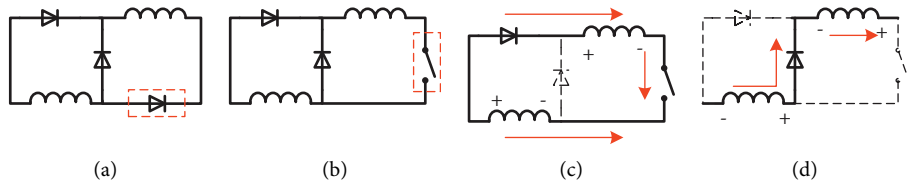


Figure 1: Switching-inductor units and operating conditions. (a) Switching-inductor [16]. (b) Improved switching-inductor. (c) The operating condition when the switch is turned on. (d) The operating condition when the switch is turned off.

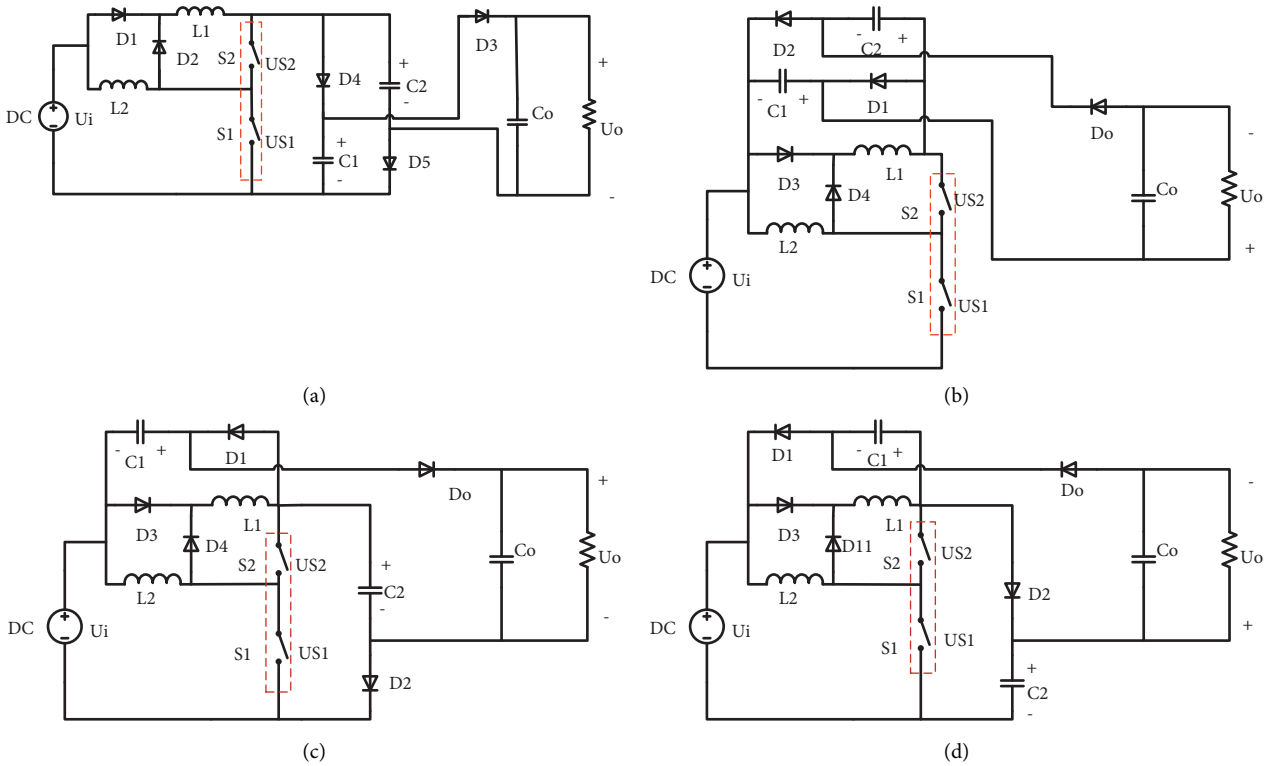


Figure 2: Proposed new DC converters. (a) Converter I. (b) Converter II. (c) Converter III. (d) Converter IV.

Table 1: Characteristics of the proposed converters.

	Figure 2(a)	Figure 2(b)	Figure 2(c)	Figure 2(d)
Voltage gain (G)	$2(1+D)/(1-D)$	$-(1+3D)/(1-D)$	$2(1+D)/(1-D)$	$-(1+3D)/(1-D)$
Switch voltage (U_{S1} and U_{S2})	$((G+2)U_o)/4G$ $((G-2)U_o)/4G$	$((G+3)U_o)/4G$ $((G-1)U_o)/4G$	$((G+2)U_o)/4G$ $((G-2)U_o)/4G$	$((G+3)Uo)/4G$ $((G-1)Uo)/4G$
Maximum of diode voltage	$(U_o/2)$	$((1+D)/(1+3D))U_o$	$(U_o/2)$	$((1+D)/(1+3D))Uo$
C/I/D/S/T	2/2/6/1/11	2/2/6/1/11	2/2/6/1/11	2/2/6/1/11
Pulsating input current(yes/no)	No	Yes	Yes	No

on, which is recorded as T_{on}, and (1-D) T_S represents the time that the switch is turned off, which is recorded as T_{off}.

The operating principle of the DS-HS converter in CCM is shown in Figure 4. The components connected by solid lines represent operation, but the components connected by dotted lines represent nonoperation in the circuit. Let us assume that the inductance of L_1 is equal to L_2, and the capacitance of C_1 is equal to C_2. The operation condition of the circuit during $t_0 - t_1$ can be shown in Figure 4(a). The inductors L_1 and L_2 are charged by the DC power supply, and in the meantime, the capacitors C_1 and C_2 charge the load. The operation condition of the circuit during $t_1 - t_2$ is shown in Figure 4(b). The DC power supply, L_1, and L_2 release energy to C_1 and C_2.

In Figure 4(a), the inductors L_1 and L_2 are charged during T_{on}, and their voltages are as follows:

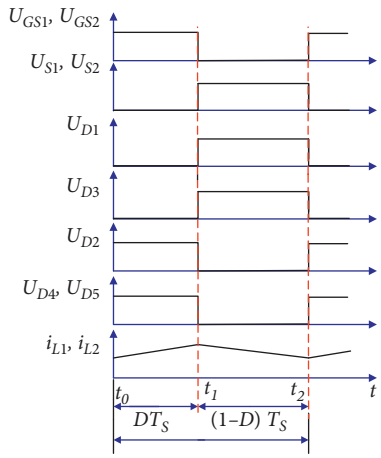


Figure 3: Switching condition and typical waveforms of CCM.

$$U_{L1} = U_{L2} = U_i, \tag{1}$$

C_1 and C_2 are discharged during the T_{on} period, and they are as follows:

$$U_{C1} = U_{C2} = \frac{U_o}{2}. \tag{2}$$

In Figure 4(b), the voltages at L_1 and L_2 are expressed during T_{off} as follows:

$$U_{L1} = U_{L2} = \frac{U_{C1} - U_i}{2} = \frac{U_{C2} - U_i}{2}. \tag{3}$$

On the basis of voltage-second balances of L_1 and L_2, the expression is as follows:

$$\int_{t_0}^{t_1} U_i \mathrm{d}t = \int_{t_0}^{t_1} \frac{U_{C1} - U_i}{2} \mathrm{d}t = \int_{t_0}^{t_1} \frac{U_{C2} - U_i}{2} \mathrm{d}t. \tag{4}$$

According to Figure 3 and equation (4), the voltages at C_1 and C_2 are as follows:

$$U_{C1} = U_{C2} = \frac{1 + D}{1 - D} V_i. \tag{5}$$

Combining the equations (2) and (5), the output voltage U_o is obtained as follows:

$$U_o = \frac{2(1 + D)}{1 - D} V_i. \tag{6}$$

According to equation (6), the voltage gain of the DS-HS converter in CCM can be expressed as follows:

$$G = \frac{2(1 + D)}{1 - D}. \tag{7}$$

4. Effect of Nonidealities on Output Voltage

The nonidealities of the DS-HS converter are considered in Figure 5 to discuss the nonideal effects of components on voltage gain. The equivalent series resistance (ESR) of the inductors L_1 and L_2 is the resistance r_L. The ON-state resistance of switches S_1 and S_2 is represented by the resistance r_S. The threshold voltage and the forward resistance of diodes D_1, D_2, D_3, D_4, and D_5 are indicated by the voltage U_{FD} and resistance r_D, respectively. The ESR of C_1 and C_2 is r_C, and the ESR of Co is shown by r_{Co}.

4.1. Nonideal Effect of Inductors L_1 and L_2 on Output Voltage. Considering the effect of ESR of the inductors L_1 and L_2, other parasitic parameters are neglected, i.e., $r_S = 0$, $r_D = 0$, $r_{Co} = 0$, $r_C = 0$, and $U_{FD} = 0$.

Considering the case mentioned above, during the T_{on} period, the voltages across inductors L_1 and L_2 are expressed as follows:

$$\begin{aligned} U_{L1} &\approx U_i - i_{L1} r_L, \\ U_{L2} &\approx U_i - i_{L2} r_L. \end{aligned} \tag{8}$$

During T_{off}, the voltages at L_1 and L_2 can be expressed as follows:

$$U_{L1} + U_{L2} \approx U_{C1} + i_{L1} r_L + i_{L2} r_L - U_i. \tag{9}$$

According to (8), add the voltages across inductors, and the following formula is obtained:

$$U_{L1} + U_{L2} \approx 2U_i - i_{L1} r_L - i_{L2} r_L. \tag{10}$$

On the basis of voltage-second balances on L_1 and L_2, the following formula is obtained:

$$(2U_i - i_{L1} r_L - i_{L2} r_L) D = (U_{C1} + i_{L1} r_L + i_{L2} r_L - U_i)(1 - D). \tag{11}$$

The ratio of the voltages of C_1 and C_2 to the input voltage U_i is as follows:

$$\frac{U_{C1}}{V_i}\Big|_{r_L} = \frac{V_{C2}}{V_i}\Big|_{r_L} = \frac{1 + D - (i_{L1} r_L + i_{L2} r_L)/V_i}{1 - D}. \tag{12}$$

Because $L_1 = L_2$, the currents through the inductors L_1 and L_2 are equal, i.e., $i_L = i_{L1} = i_{L2}$. Assume that the voltage drop across ESR of the inductor is U_{d-L}, i.e., $U_{d-L} = i_{L1} r_L = i_{L2} r_L$. Thus, (12) can be re-expressed as follows:

$$\frac{U_{C1}}{V_i}\Big|_{r_L} = \frac{U_{C2}}{V_i}\Big|_{r_L} = \frac{1 + D - 2U_{d-L}/V_i}{1 - D}. \tag{13}$$

The relationship between the output voltage U_o and the voltages of C_1 and C_2 is as follows:

$$U_o = 2U_{C1} = 2U_{C2}. \tag{14}$$

Combining the formulas (13) and (14), the voltage gain of the DS-HS converter can be deduced as follows:

$$\frac{U_o}{U_i}\Big|_{r_L} = \frac{2(1 + D) - 4U_{d-L}/U_i}{1 - D}. \tag{15}$$

Considering the different values of U_{d-L}/U_i and duty cycle D, equation (15) is shown in Figure 6(a), which indicates the effect of the inductor's ESR on the voltage gain. It can be observed that the voltage gain will decrease for higher values of U_{d-L}. This fact indicates that the ESR (r_L) of the inductor should be as small as possible.

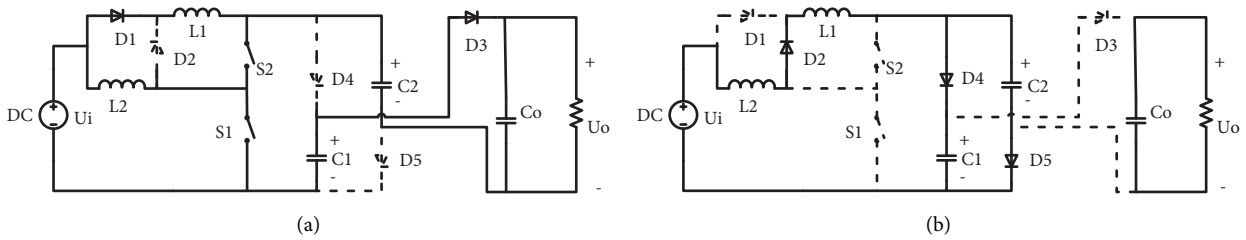


Figure 4: Operating principles of the DS-HS converter in CCM. (a) When S_1 is T_{on}. (b) When S_1 is T_{off}.

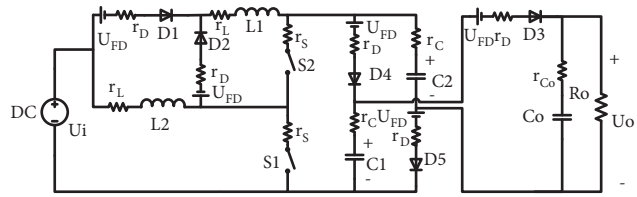


Figure 5: Nonideal equivalent circuit of the DS-HS converter.

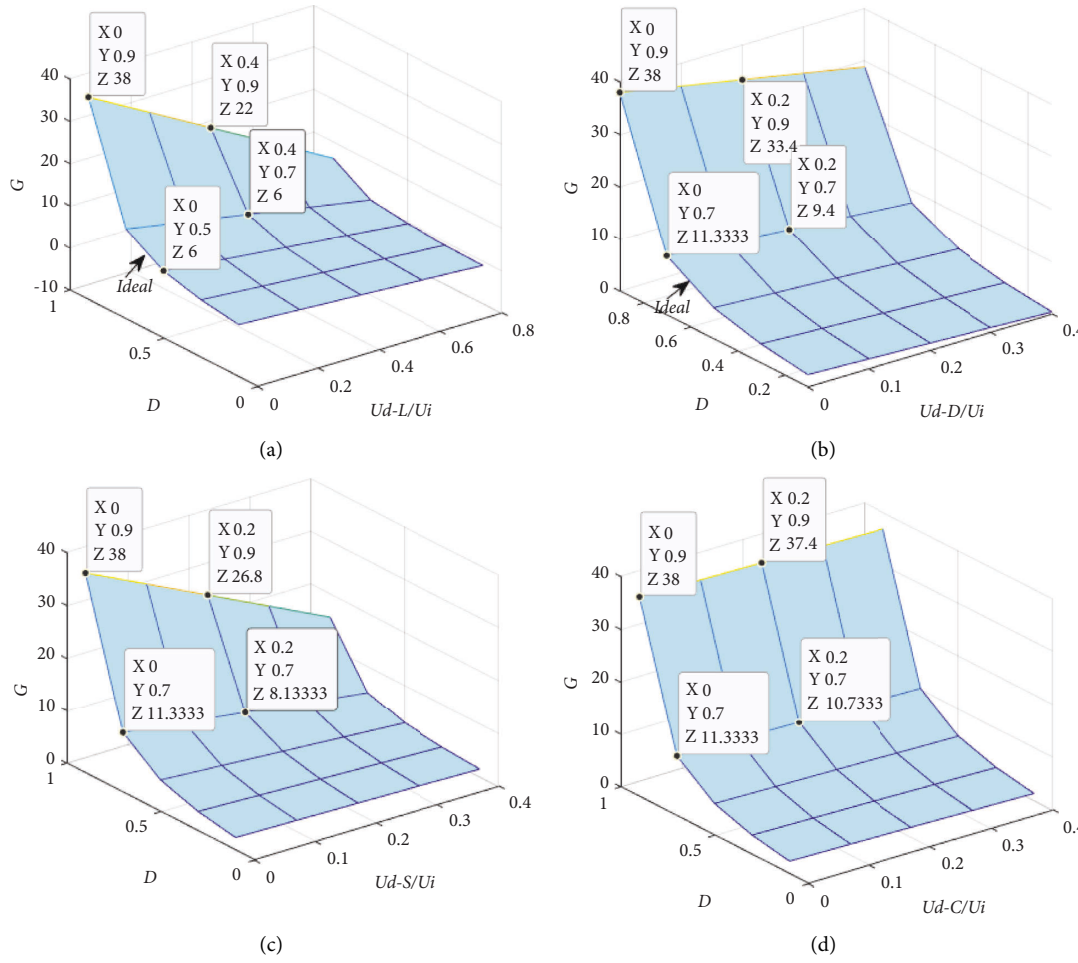


Figure 6: Nonideal effect on the duty cycle and voltage gain. (a) Inductors, (b) diodes, (c) switches, and (d) capacitors.

4.2. Effect of Diodes D_1, D_2, D_3, D_4, and D_5 on Output Voltage. Considering the effect of diodes D_1, D_2, D_3, D_4, and D_5, other parasitic parameters are neglected, i.e., $r_L = 0$, $r_C = 0$, $r_{Co} = 0$, and $r_S = 0$. Assume that the voltage drops due to forward resistance, and the threshold voltage of the diodes are U_{d-D1}, U_{d-D2}, U_{d-D3}, U_{d-D4}, and U_{d-D5}, and the expressions are as follows:

$$\begin{aligned} U_{d-D1} &= U_{FD} + i_{D1} r_D, \\ U_{d-D2} &= U_{FD} + i_{D2} r_D, \\ U_{d-D3} &= U_{FD} + i_{D3} r_D, \\ U_{d-D4} &= U_{FD} + i_{D4} r_D, \\ U_{d-D5} &= U_{FD} + i_{D5} r_D. \end{aligned} \tag{16}$$

Considering the case mentioned above, during T_{on}, the voltages across inductors L_1 and L_2 are expressed as follows:

$$U_{L1} \approx U_i - U_{d-D1}, U_{L2} \approx U_i. \tag{17}$$

During T_{off}, the voltages at L_1 and L_2 are as follows:

$$\begin{aligned} U_{L1} + U_{L2} &\approx U_{C1} + U_{d-D2} + U_{d-D4} - U_i \\ &= U_{C2} + U_{d-D2} + U_{d-D5} - U_i. \end{aligned} \tag{18}$$

According to (17), add voltages across inductors, and the following formula is obtained:

$$U_{L1} + U_{L2} \approx 2U_i - U_{d-D1}. \tag{19}$$

On the basis of voltage-second balances on L_1 and L_2, the following formula is obtained:

$$\begin{aligned} (2U_i - U_{d-D1})D &= (U_{C1} + U_{d-D2} + U_{d-D4} - U_i)(1-D) \\ &= (U_{C2} + U_{d-D2} + U_{d-D5} - U_i)(1-D). \end{aligned} \tag{20}$$

The ratios of the voltages of C_1 and C_2 to the input voltage U_i are obtained as follows:

$$\frac{U_{C1}}{U_i}\Big|_{r_D} = \frac{1 + D - DU_{d-D1}/U_i - (1-D)(U_{d-D2} + U_{d-D4})/U_i}{1-D}, \tag{21}$$

$$\frac{U_{C2}}{U_i}\Big|_{r_D} = \frac{1 + D - DU_{d-D1}/U_i - (1-D)(U_{d-D2} + U_{d-D5})/U_i}{1-D}. \tag{22}$$

Combining the formulas (14), (21), and (22), the relationship between output and input voltages on the DS-HS converter can be deduced as follows:

$$\begin{aligned} \frac{U_o}{U_i}\Big|_{r_D} &= \frac{U_{C1}}{U_i}\Big|_{r_D} + \frac{U_{C2}}{U_i}\Big|_{r_D} - \frac{U_{d-D3}}{U_i} \\ &= \left(2(1+D) - \frac{2DU_{d-D1}}{U_i} - (1-D)\frac{(2U_{d-D2} + U_{d-D3})}{U_i} - (1-D)\frac{(U_{d-D4} + U_{d-D5})}{V_i}\right)\frac{1}{1-D}. \end{aligned} \tag{23}$$

Assuming that the voltage drops of all the diodes are equal, then we get the following formula:

$$U_{d-D} = U_{d-D1} = U_{d-D2} = U_{d-D3} = U_{d-D4} = U_{d-D5}. \tag{24}$$

Thus, (23) can be re-expressed as follows:

$$\frac{U_o}{U_i}\Big|_{r_D} = \frac{2(1+D) - (5-3D)U_{d-D}/U_i}{1-D}. \tag{25}$$

Considering the different values of U_{d-D}/U_i and D, equation (25) is revealed in Figure 6(b), which indicates the effect of the diodes on the voltage gain. It can be observed that for higher values of U_{d-D}/U_i, the voltage gain will decrease. It indicates that the smaller the forward resistance and threshold voltage of the diodes, the better.

4.3. Effect of Switches S_1 and S_2 on Output Voltage. Since only the effect of switches S_1 and S_2 is analyzed here, other parasitic parameters are neglected, i.e., $r_L = 0$, $r_C = 0$, $r_{Co} = 0$, $r_D = 0$, and $U_{FD} = 0$.

During T_{on}, the voltages across inductors L_1 and L_2 are as follows:

$$\begin{aligned} U_{L1} &\approx U_i - i_{S1} r_S - i_{S2} r_S, \\ U_{L2} &\approx U_i - i_{S1} r_S. \end{aligned} \tag{26}$$

During T_{off}, the voltages at L_1 and L_2 are expressed as follows:

$$U_{L1} + U_{L2} \approx U_{C1} - U_i = U_{C2} - U_i. \tag{27}$$

According to (26), add voltages across L_1 and L_2, and the formula is obtained as follows:

$$U_{L1} + U_{L2} \approx 2U_i - 2i_{S1} r_S - i_{S2} r_S. \tag{28}$$

On the basis of voltage-second balances on L_1 and L_2, the following formula is obtained:

$$\begin{aligned} (2U_i - 2i_{S1} r_S - i_{S2} r_S)D &= (U_{C1} - U_i)(1-D) \\ &= (U_{C2} - U_i)(1-D). \end{aligned} \tag{29}$$

The ratios of the voltages of C_1 and C_2 to the input voltage U_i are as follows:

$$\frac{U_{C1}}{U_i}\Big|_{r_S} = \frac{U_{C2}}{U_i}\Big|_{r_S} = \frac{1 + D - D\left(2i_{S1}r_S + i_{S2}r_S\right)/U_i}{1 - D}. \tag{30}$$

Combining the formulas (14) and (30), the voltage gain of the DS-HS converter can be obtained as follows:

$$\begin{aligned}\frac{U_o}{U_i}\Big|_{r_S} &= \frac{U_{C1}}{U_i}\Big|_{r_S} + \frac{U_{C2}}{U_i}\Big|_{r_S} - \frac{\left(i_{S1}r_S + i_{S2}r_S\right)}{U_i} \\ &= \frac{2(1+D) - 2D\left(2i_{S1}r_S + i_{S2}r_S\right)/U_i - (1-D)\left(i_{S1}r_S + i_{S2}r_S\right)/U_i}{1 - D} \\ &= \frac{2(1+D) - (1+3D)i_{S1}r_S/U_i - (1+D)i_{S2}r_S/U_i}{1 - D}.\end{aligned} \tag{31}$$

Assume that the voltage drops on the switches S_1 and S_2 are as follows:

$$\begin{aligned}U_{d-S1} &= i_{S1}r_S, \\ U_{d-S2} &= i_{S2}r_S.\end{aligned} \tag{32}$$

Thus, (31) can be re-expressed as follows:

$$\frac{U_o}{U_i}\Big|_{r_S} = \frac{2(1+D) - (1+3D)U_{d-S1}/U_i - (1+D)U_{d-S2}/U_i}{1 - D}. \tag{33}$$

Assume that $U_{d-S} = U_{d-S1} = U_{d-S2}$. Thus, (33) is re-written as follows:

$$\frac{U_o}{U_i}\Big|_{r_S} = \frac{2(1+D) - 2(1+2D)U_{d-S}/U_i}{1 - D}. \tag{34}$$

By considering the different values of U_{d-S}/U_i and D, (34) is shown in Figure 6(c), and it also shows the relationship between the on-resistance of the switches and the voltage gain. It is observed that the higher the values of U_{d-S}, the lower the voltage gain. This fact indicates that the ON-state resistance of the switches should be as small as possible.

4.4. Effect of the Capacitors C_1, C_2, and Co on Output Voltage. Considering the effect of ESR of capacitors C1, C2, and *Co*, other parasitic parameters are neglected, i.e., $r_L = 0$, $r_D = 0$, $U_{FD} = 0$, and $r_S = 0$.

Considering the case mentioned above, during T_{on}, the voltages across the inductors L_1 and L_2 are expressed as follows:

$$\begin{aligned}U_{L1} &\approx U_i, \\ U_{L2} &\approx U_i.\end{aligned} \tag{35}$$

Simultaneously, C_1 and C_2 are discharged to *Co*, and the output voltage is as follows:

$$U_{o\,\text{on}} = U_{C1} + U_{C2} - i_{C1\,\text{on}}r_C - i_{C2\,\text{on}}r_C = U_{Co} + i_{Co\,\text{on}}r_{Co}. \tag{36}$$

During T_{off}, the voltages at L_1 and L_2 are expressed as follows:

$$U_{L1} + U_{L2} \approx U_{C1} + i_{C1\,\text{off}}r_C - U_i = U_{C2} + i_{C2\,\text{off}}r_C - U_i. \tag{37}$$

The capacitor *Co* is discharged through load Ro during $t_1 - t_2$, and the output voltage is as follows:

$$U_{o\,\text{off}} = U_{Co} - i_{Co\,\text{off}}r_{Co}. \tag{38}$$

According to (35), add voltages across inductors, and the following formula is obtained:

$$U_{L1} + U_{L2} \approx 2U_i. \tag{39}$$

On the basis of voltage-second balances on L_1 and L_2, the following formula is obtained:

$$\begin{aligned}2U_iD &= \left(U_{C1} + i_{C1\,\text{off}}r_C - U_i\right)(1 - D) \\ &= \left(U_{C2} + i_{C2\,\text{off}}r_C - U_i\right)(1 - D).\end{aligned} \tag{40}$$

The ratios of the voltage of C_1 and C_2 to the input voltage V_i are shown as follows:

$$\frac{U_{C1}}{U_i}\Big|_{r_C} = \frac{1 + D - i_{C1\,\text{off}}r_C(1 - D)/U_i}{1 - D}, \tag{41}$$

$$\frac{U_{C2}}{U_i}\Big|_{r_C} = \frac{1 + D - i_{C2\,\text{off}}r_C(1 - D)/U_i}{1 - D}. \tag{42}$$

Since the capacitor voltage cannot be changed suddenly, the voltages across C_1, C_2, and *Co* remain unchanged during

the whole cycle. Therefore, the average value of the output voltage U_o in a whole period is as follows:

$$U_o = DU_{o\text{on}} + (1-D)U_{o\text{off}} = U_{Co}. \tag{43}$$

According to formulas (36), (38), (41), and (42), it can be obtained as follows:

$$\begin{aligned}\frac{U_o}{U_i}\Big|_{r_C, r_{Co}} &= \frac{U_{Co}}{U_i} = \frac{U_{C1} + U_{C2} - i_{C1\,\text{on}} r_C - i_{C2\,\text{on}} r_C - i_{Co\,\text{on}} r_{Co}}{U_i} \\ &= \frac{\left(2(1+D) - i_{C1\,\text{off}} r_C (1-D)/U_i - i_{C2\,\text{off}} r_C (1-D)/U_i - i_{C1\,\text{on}} r_C (1-D)/U_i - i_{C2\,\text{on}} r_C (1-D)/U_i - i_{Co\,\text{on}} r_{Co} (1-D)/U_i\right)}{1-D} \\ &= \frac{\left(2(1+D) - \left(i_{C1\,\text{off}} + i_{C1\,\text{on}}\right) r_C (1-D)/U_i - \left(i_{C2\,\text{off}} + i_{C2\,\text{on}}\right) r_C (1-D)/U_i - i_{Co\,\text{on}} r_{Co} (1-D)/U_i\right)}{1-D}.\end{aligned} \tag{44}$$

The currents through the capacitors C_1 and C_2 are as follows:

$$\begin{aligned} i_{C\,\text{on}} &= i_{C1\,\text{on}} = i_{C2\,\text{on}}, \\ i_{C\,\text{off}} &= i_{C1\,\text{off}} = i_{C2\,\text{off}}. \end{aligned} \tag{45}$$

Hence, the voltage gain is as follows:

$$\frac{U_o}{U_i}\Big|_{r_C, r_{Co}} = \frac{2(1+D) - i_{Co\,\text{on}} r_{Co} (1-D)/U_i - 2\left(i_{C\,\text{off}} + i_{C\,\text{on}}\right) r_C (1-D)/U_i}{1-D}. \tag{46}$$

Let us suppose the voltage drops due to ESR of C_1, C_2, and Co are U_{d-C} and U_{d-Co}, then we get the following formula:

$$\begin{aligned} U_{d-C} &= \left(i_{C\,\text{off}} + i_{C\,\text{on}}\right) r_C, \\ U_{d-Co} &= i_{Co\,\text{on}} r_{Co}. \end{aligned} \tag{47}$$

Thus, (46) can be re-expressed as follows:

$$\frac{U_o}{U_i}\Big|_{r_C, r_{Co}} = \frac{2(1+D) - 2U_{d-C}(1-D)/U_i - U_{d-Co}(1-D)/U_i}{1-D}. \tag{48}$$

Further, let us assume that $U_{d-C} = U_{d-Co}$. Thus, (48) is rewritten as follows:

$$\frac{U_o}{U_i}\Big|_{r_C} = \frac{2(1+D) - 3U_{d-C}(1-D)/U_i}{1-D}. \tag{49}$$

By considering the different values of U_{d-C}/U_i and D, equation (49) is shown in Figure 6(d), and it shows the effect of the ESR of the capacitors on voltage gain. It can be observed that for higher values of U_{d-C}/U_i, the voltage gain will decrease. This fact indicates that the ESR of the capacitor should be as small as possible.

4.5. Combined Effect of Nonidealities on Voltage Gain. By considering the nonideal effect of inductors L_1 and L_2, diodes D_1, D_2, D_3, D_4, and D_5, switches S_1 and S_2, and capacitors C_1, C_2, and Co, respectively, the voltage gain is expressed as follows:

$$\frac{U_o}{U_i} \approx \frac{\left(2(1+D) - 4U_{d-L}/U_i - (5-3D)U_{d-D}/U_i - 2(1+2D)U_{d-S}/U_i - 3U_{d-C}(1-D)/U_i\right)}{1-D}. \tag{50}$$

4.6. Efficiency Analysis. The proportional relationship between the inductor current and the output current is as follows:

$$I_L = I_{L1} = I_{L2} = \frac{2}{1-D} I_o = \frac{2}{1-D} \frac{U_o}{R_o}. \tag{51}$$

Considering that P_{SW-S1} and P_{SW-S2} are the power losses on account of switching of S_1 and S_2, respectively, the total loss P_{SW} during switching is as follows:

$$P_{SW} = \sum_{i=1,2} P_{SW-Si} = \frac{1}{2T_S}\left(I_{S1}U_{S1}\left(t_{r-S1} + t_{f-S1}\right) + I_{S2}U_{S2}\left(t_{r-S2} + t_{f-S2}\right)\right), \tag{52}$$

where the rising and falling time of switches S_1 and S_2 are t_{r-S1}, t_{f-S1} and t_{r-S2}, t_{f-S2}; I_{S1}, U_{S1} and I_{S2}, U_{S2} are the average current and voltage on S_1 and S_2.

The core loss of the inductors is considered, so it can be shown as follows:

$$P_{Fe} = 2KM' f^m B_{ac}^n, \tag{53}$$

where B_{ac}^n is the operating magnetic position swing of the inductor core, M' is the quality of the inductor core, and K, m, and n are the coefficients determined by the core material. The parameters can be found in the datasheet.

The total power of the input and output are received as follows:

$$P_i \begin{cases} = U_i\left[2I_L D + I_L(1-D)\right] + P_{SW} + P_{Fe}, \\ = \dfrac{2U_i}{1-D}\dfrac{U_o}{R_o}(1+D) + P_{SW} + P_{Fe}, \end{cases} \qquad P_o = \frac{U_o^2}{R_o}. \tag{54}$$

According to (50)–(54), the efficiency of the DS-HS converter is obtained as follows:

$$\eta \approx \frac{\left(2(1+D) - 4U_{d-L}/U_i - (5-3D)U_{d-D}/U_i - 2(1+2D)U_{d-S}/U_i - 3U_{d-C}(1-D)/U_i\right)}{2(1+D) + P_{SW}\left(R_o(1-D)/U_oU_i\right) + P_{Fe}\left(R_o(1-D)/U_oU_i\right)}. \tag{55}$$

5. Comparison of Converters

Many converters have recently been proposed to realize high voltage gain. The DS-HS converter is compared with the classical and recently proposed converters in this part. The detailed comparison is shown in Table 2, including voltage gain, number of components, the position of the switch, the voltage and current stresses of switches and diodes, the average value and effective value of inductor current, and efficiency. It is obvious that the total number of components of the DS-HS converter is the same as the converter in [20]. The efficiency of the converter depends on several factors, including voltage and current ratings and their types.

The comparison of the voltage gain for converters is revealed in Figure 7(a). From Figure 7(a), it can be seen that the DS-HS converter and the converter in [20] have higher voltage gain, compared with the converters in [4, 16, 19]. The average values of inductor currents for the converters are described in Figure 7(b), which reflect the relationship between the voltage gain G and the ratio of average inductor current to output current I_L/I_o. From Figure 7(b), it is evident that I_L/I_o of the DS-HS converter and the converter in [20] is slightly higher than that of the converters in [16, 19] but much lower than the boost converter in [4]. The figures of normalized current stress on switches and diodes are incarnated in Figures 8(a) and 8(b). The comparison chart of total current stress on switches and diodes for converter topologies is shown in Figure 8(c), and the comparison chart of total current stress per component is revealed in Figure 8(d). The comparison between the total current stress of the converters is as follows:

$$\underbrace{\frac{3(G+1)}{2}I_o}_{[19]} < \underbrace{2GI_o}_{\text{Boost}[4]} < \underbrace{3(G+1)I_o}_{[16]} < \underbrace{3(G+2)I_o + \frac{2(G+2)}{G-2}I_o}_{[20]} < \underbrace{3(G+2)I_o + \frac{3(G+2)}{G-2}I_o}_{\text{Proposed}}. \tag{56}$$

The relationship between the total current stress averaged to each element is shown as follows:

$$\underbrace{\frac{(G+1)}{2}I_o}_{[19]} < \underbrace{\frac{3(G+1)I_o}{5}}_{[16]} < \underbrace{GI_o}_{\text{Boost}[4]} \underbrace{\frac{3(G+2)I_o + (2(G+2)/(G-2))I_o}{7}}_{[20]} < \underbrace{\frac{3(G+2)I_o + (3(G+2)/(G-2))I_o}{7}}_{\text{Proposed}}. \tag{57}$$

Table 2: The comparison of converters.

	Boost [4]	The converter in [13]	The converter in [16]	The converter in [17]	Proposed converter
C/I/D/S/T	1/1/1/1/4	1/2/4/1/8	1/2/1/2/6	3/2/6/1/12	3/2/5/2/12
Voltage gain	$1/(1-D)$	$(1+D)/(1-D)$	$(1+D)/(1-D)$	$2(1+D)/(1-D)$	$2(1+D)/(1-D)$
Switch voltage	U_o	U_o	$(G+1)U_o/2G$	$(U_o/2)$	$U_{S1} = (G+2)U_o/4G$ $U_{S2} = (G-2)U_o/4G$
Diode voltage	U_o	$U_{D1,3} = ((G-1)U_o/2G)$ $U_{D2} = (U_o/G)$ $U_{Do} = U_o$	$(G+1)U_o/G$	$U_{D1,3} = ((G-2)U_o/4G)$ $U_{D2} = (U_o/G)$ $U_{D4-6} = (U_o/2)$	$V_{D1} = (G-2)U_o/4G$ $V_{D2} = (U_o/G)$ $V_{D3-5} = (U_o/2)$
The average value of inductor current	GI_o	$((G+1)/2)I_o$	$((G+1)/2)I_o$	$((G+2)/2)I_o$	$((G+2)/2)I_o$
RMS of inductor current	$\sqrt{(GI_o)^2 + (1/12)(U_iD/Lf_s)^2}$	$\sqrt{(((G+1)/2)I_o)^2 + (1/12)(U_iD/Lf_s)^2}$	$\sqrt{(((G+1)/2)I_o)^2 + (1/12)(U_iD/Lf_s)^2}$	$\sqrt{(((G+2)/2)I_o)^2 + (1/12)(U_iD/Lf_s)^2}$	$\sqrt{(((G+2)/2)I_o)^2 + (1/12)(U_iD/Lf_s)^2}$
Switch current	GI_o	$(G+1)I_o$	$((G+1)/2)I_o$	$((G^2+G-2)/(G-2))I_o$	$I_{S1} = ((G^2+G-2)/(G-2))I_o$ $I_{S2} = ((G^2+2G)/2(G-2))I_o$
Diode current	GI_o	$I_{D1-3,D_o} = ((G+1)/2)I_o$	$((G+1)/2)I_o$	$I_{D1-3} = ((G+2)/2)I_o$ $I_{D4-5} = ((G+2)/4)I_o$ $I_{D6} = ((G+2)/(G-2))I_o$	$I_{D1-2} = ((G+2)/2)I_o$ $I_{D4-5} = ((G+2)/4)I_o$ $I_{D3} = ((G+2)/(G-2))I_o$
Common ground	Yes	Yes	No	No	No
High/low side gate driver	Low	Low	High/low	Low	High/low
Power efficiency	100 W 88%	40 W 90.2%	40W 92.7%	100 W 94.31%	100W 96.15%

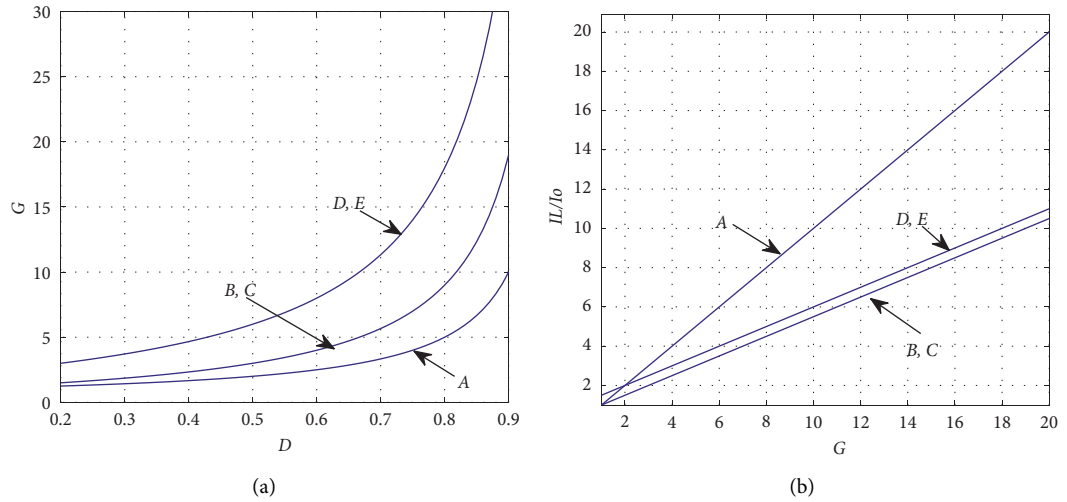


Figure 7: Comparison. (a) Voltage gain G versus duty cycle D. (b) The ratio of inductor current *IL* to output current Io versus duty cycle D. Note: A represents boost converter [4], B represents SIBC [16], C represents converter [19], D represents converter [20], and E represents the proposed DS-HS converter.

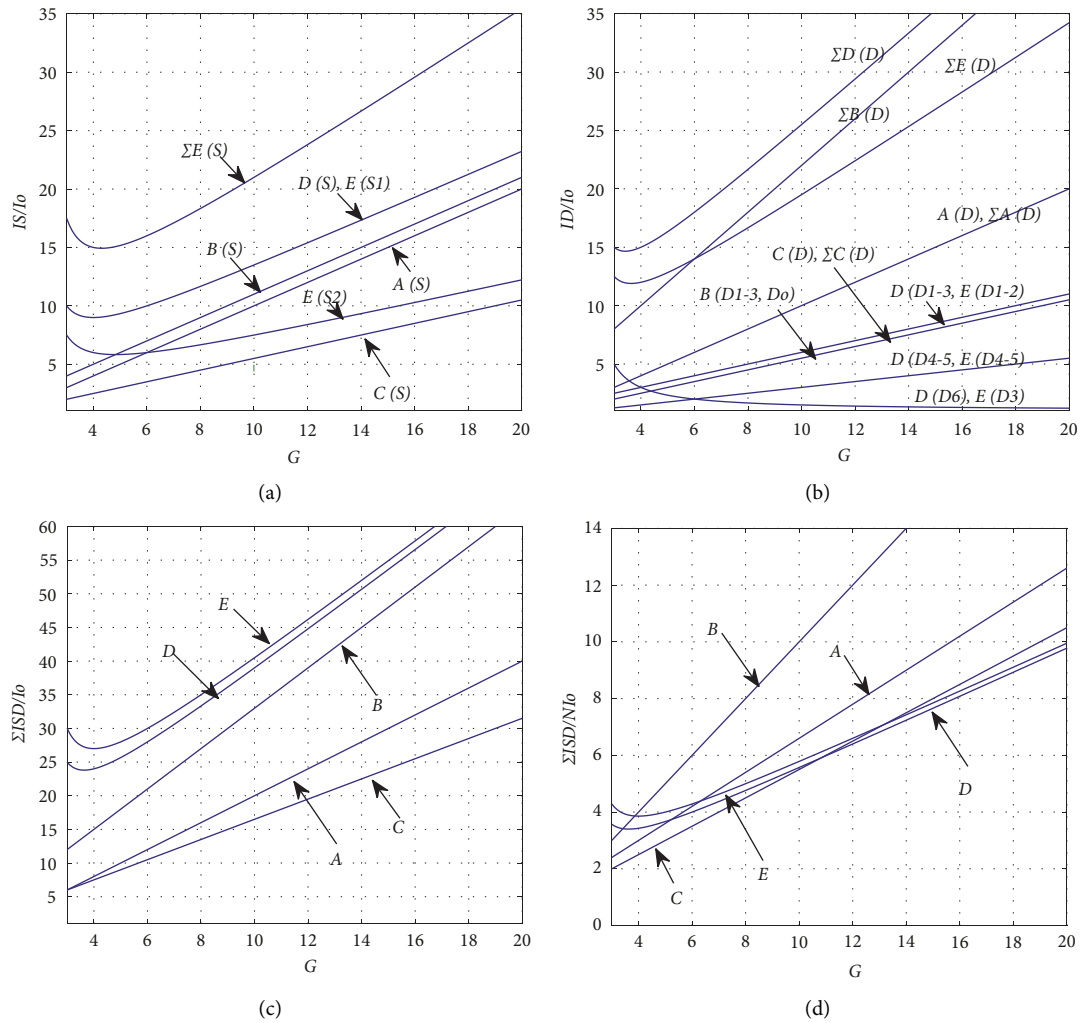


Figure 8: Comparison of current. (a) Switch currents, (b) diode currents, (c) Σ*ISD*/*Io* versus voltage gain *G*, and (d) Σ*ISD*/*NIo* versus voltage gain *G*. Note: *X*(*Z*) means the switch or diode of converter *X*, Σ*X*(*Z*) are total current of switches or diodes for converter *X*, and Σ*ISD* are total current stress of switches and diodes.

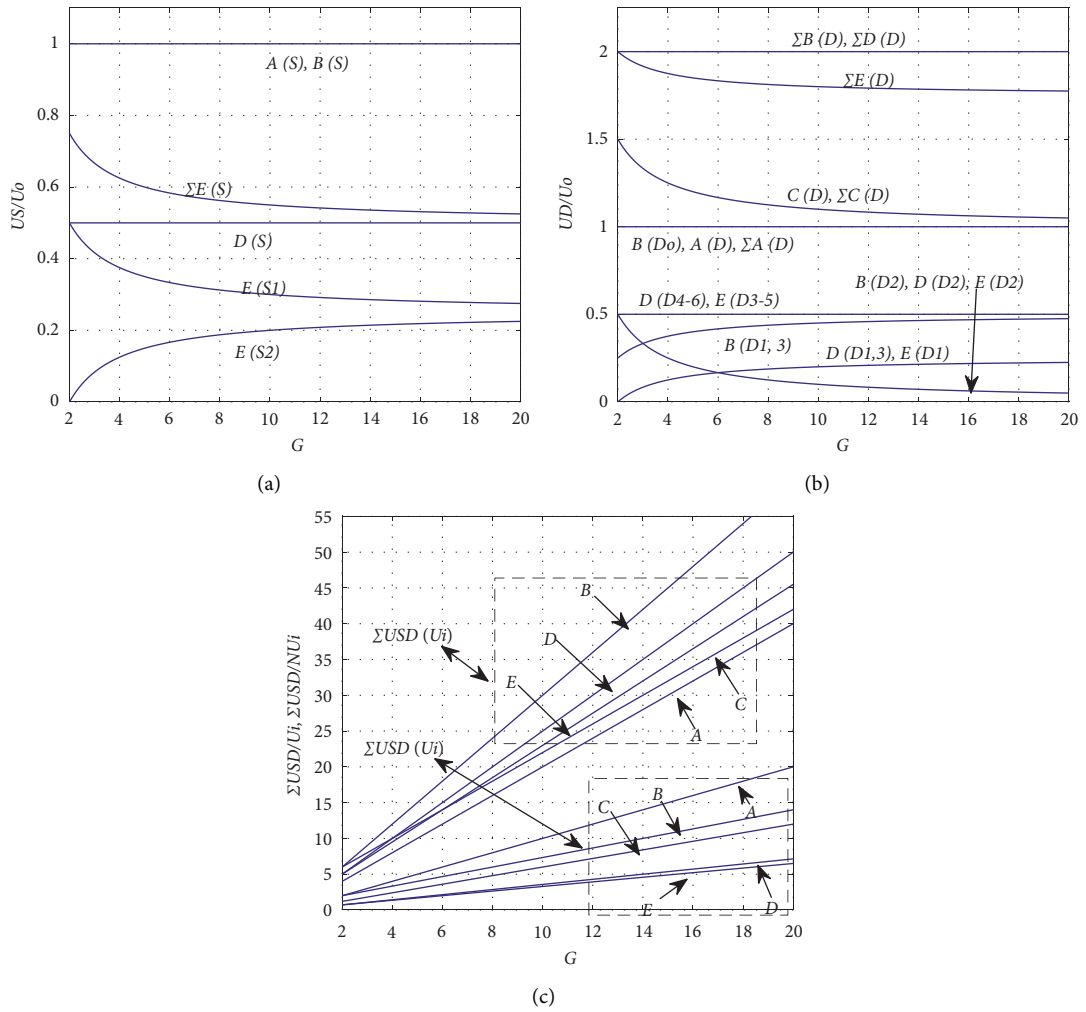


Figure 9: Comparison of voltage. (a) Switch voltages, (b) diode voltages, and (c) Σ*USD*/*Ui* and Σ*USD*/*NUi* versus voltage gain *G*. Note: *X*(*Z*) means the switch or diode of converter *X*, Σ*X*(*Z*) are total voltage of switches or diodes for converter *X*, and Σ*VSD* are total voltage stress of switches and diodes.

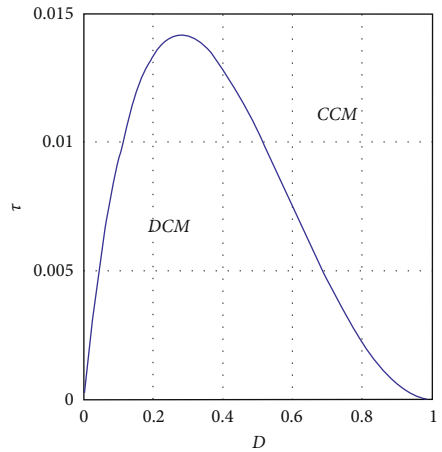


Figure 10: Boundary condition of the HS-LC converter.

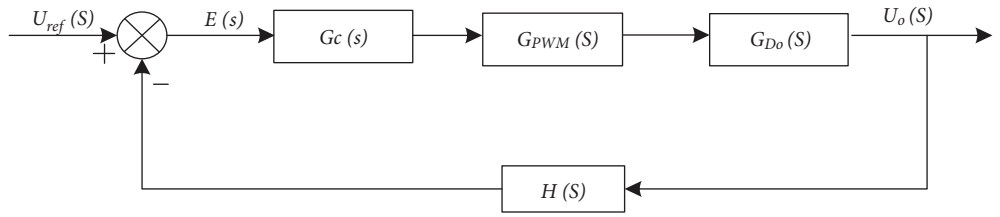


Figure 11: Voltage loop control scheme of the DS-HS converter.

Table 3: The design index and component parameters.

Components	Parameter
Output power P_o	100 W
Output voltage V_o	380 V
Input voltage V_i	25 V
f_s(frequency)	80 kHz
L_1, L_2(inductors)	320 μH
C_1, C_2(capacitors)	6.8 μF
S_1, S_2(MOSFET)	IRFP260 N
D_2(diodes)	V50100P
D_1(diodes)	MBR40200PT
D_3, D_4, and D_5(diodes)	SBR20A300CT
Co(out capacitor)	680 μF/450V

Generally speaking, the cost of components increases parabolically with component ratings. A high rating means high cost and high on-resistance. The relationship of total voltage stresses for converters is as follows:

$$\underbrace{2GU_i}_{\text{Boost}[4]} < \underbrace{2(G+1)U_i}_{[19]} < \underbrace{\frac{9G+2}{4}U_i}_{\text{Proposed}} < \underbrace{\frac{5G}{2}U_i}_{[20]} < \underbrace{3GU_i}_{[16]}. \quad (58)$$

The total voltage stress of each component is received as follows:

$$\underbrace{\frac{9G+2}{28}U_i}_{\text{Proposed}} < \underbrace{\frac{5G}{14}U_i}_{[20]} < \underbrace{\frac{2(G+1)U_i}{3}}_{[19]} < \underbrace{\frac{3GU_i}{5}}_{[16]} < \underbrace{GU_i}_{\text{Boost}[4]}. \quad (59)$$

The figures of normalized voltage stress on switches and diodes are reflected in Figures 9(a) and 9(b), respectively. The comparison chart of total current stress for converters is shown in Figure 9(c), and the comparison chart of total current stress per component is also shown in Figure 9(c). According to (59), on average for each component, the proposed DS-HS converter has lower voltage stress than the converters in [4, 16, 19, 20].

Half of the total output voltage for the proposed DS-HS converter is shared by two switches. Then, low voltage rating switches can be used to design DS-HS converters. In general, as the rating of any device increases, its on-resistance increases. It can be seen that the DS-HS converter requires lower rating components. The efficiency of the classical boost converter [4] and suggested converters in [16, 19, 20] are 88%, 90.2%, 92.7%, and 94.31%, respectively, and that of the DS-HS converter is 96.15%. Therefore, the proposed DS-HS converter has higher efficiency compared with converters in [4, 16, 19, 20].

By comparing with the converter in [20], the DS-HS converter has the same number of components, and the difference in components is just one more switch and one less diode. Therefore, the difference in loss is derived in detail as shown in the following figure.

The total switching losses of the converter in [20] and the proposed DS-HS converter are shown as follows:

$$\begin{aligned} P_{SD}^{[20]} &= \left(E_S + E_{D1} + E_{D2} + E_{D3} + E_{D4} + E_{D5} + E_{D6}\right) f_s, \\ P_{SD}^{DS-HS} &= \left(E_{S1} + E_{S2} + E_{D1} + E_{D2} + E_{D3} + E_{D4} + E_{D5}\right) f_s, \end{aligned} \quad (60)$$

where E represents the energy loss during the switching process, and its subscript represents the components. The difference value between the switching loss of the DS-HS converter and the converter in [20] is shown as follows:

$$\begin{aligned} P_{SD}^{DS-HS} - P_{SD}^{[20]} = &\left(E_{\text{on},S1} + E_{\text{off},S1} + E_{\text{on},S2} + E_{\text{off},S2}\right) f_s \\ &- \left(E_{\text{on},S} + E_{\text{off},S} + E_{\text{on},D3} + E_{\text{off},D3}\right) f_s, \end{aligned} \quad (61)$$

where E_{on} and E_{off} represent the switching energy loss of turn-on and turn-off. Through solving (61), the following formula is obtained:

$$\begin{aligned} &P_{SD}^{DS-HS} - P_{SD}^{D} \\ &= \left(U_{S1} I_{S1} + U_{S2} I_{S2} - U_S I_S\right)\left(t_r + t_f\right) f_s - E_{D3} f_s, \end{aligned} \quad (62)$$

where t_r and t_f represent rise time and fall time. According to the formula (62), the final difference value between the switching losses is as follows:

$$P_{SD}^{DS-HS} - P_{SD}^{D} = -\frac{(G-2)}{4G} DU_o I_L \left(t_r + t_f\right) f_s - E_{D3} f_s < 0, \quad G \geq 2. \tag{63}$$

The solution of (63) is always negative, when the voltage gain G is greater than 2.

Therefore, it can be concluded that the switching loss of the DS-HS converter is less than the converter in [20]. According to the above analysis, the DS-HS converter provides a feasible method to achieve high voltage gain, reduce voltage stress, and improve efficiency.

6. Design Criteria of Component Parameters

The parameter design criteria for inductors and capacitors are given as follows.

When the DS-HS converter operates at the boundary (BCM) between the CCM and DCM modes, the relationship between the average inductor current and the minimum load current I_{oG} is as follows:

$$I_{L1} = I_{L2} = \frac{2DI_{oG}}{1-D}. \tag{64}$$

For a given application, if the maximum allowable value for the inductor current ripple is $\Delta I_{L\max}$, then we get the following formula:

$$\Delta I_{L\max} = K_i I_{L1} = K_i I_{L2}. \tag{65}$$

For the relationship of $\Delta I_{L1} \leq \Delta I_{L1\max}$ and $\Delta I_{L2} \leq \Delta I_{L2\max}$, the minimum inductance of L_1 and L_2 is as follows:

$$L1_{\min} = L2_{\min} = \frac{D(1-D)U_i}{2f_s K_i I_{oG}}, \tag{66}$$

where $f_s = (1/T_s)$, and K_i is the proportional coefficient.

In order to ensure that the DS-HS converter works in CCM, the following inequality needs to be satisfied:

$$I_{L1} \geq \frac{1}{2}\Delta i_{L1}, \quad I_{L2} \geq \frac{1}{2}\Delta i_{L2}, \tag{67}$$

ΔI_{L1} and ΔI_{L2} in the formula are the inductor current ripples, and $\Delta i_{L1} = (U_i/L1)DT_s, \Delta i_{L2} = (U_i/L2)DT_s$.

Substituting formula (64) into (67), the following formula is obtained:

$$\frac{L1 f_s}{R_o} = \frac{L2 f_s}{R_o} \geq \frac{D(1-D)^2}{8(1+D)}. \tag{68}$$

The normalized inductor time constant τ is as follows:

$$\tau = \frac{L1 f_s}{R_o} = \frac{L2 f_s}{R_o}. \tag{69}$$

By combining equations (68) and (69), the boundary functions of the DS-HS converter working in CCM and DCM can be obtained as follows:

$$\tau \geq \frac{D(1-D)^2}{8(1+D)}. \tag{70}$$

The boundary conditions of the HS-LC converter are shown in Figure 10. From Figure 10, it can be seen that when τ is below the solid line, the circuit works in DCM, and when τ is above the solid line, the circuit works in CCM.

Simplifying formula (68), the relationship of Ro can be obtained as follows:

$$R_o \leq \frac{8L1 f_s (1+D)}{D(1-D)^2} = \frac{8L1 f_s (1+D)}{D(1-D)^2}. \tag{71}$$

According to formula (71), it can be known that the value of the load Ro also determines whether the circuit works in CCM or DCM.

The minimum capacitance formula is as follows:

$$C1_{\min} = C2_{\min} = \frac{DU_o}{\left|\Delta U_{C1\max}\right| R_o f_s} = \frac{DU_o}{\left|\Delta U_{C2\max}\right| R_o f_s}, \tag{72}$$

ΔV_{C1} and ΔV_{C2} are the voltage ripples of the capacitors, and $\Delta V_{C1\max}$ and $\Delta V_{C2\max}$ are the maximum allowable values of ΔV_{C1} and ΔV_{C2}, respectively.

The minimum value of the output capacitor is as follows:

$$C_{o\min} = \frac{(1-D)U_o}{\left|\Delta U_{Co\max}\right| R_o f_s}, \tag{73}$$

where $\Delta V_{Co\max}$ is the maximum allowable value of ΔV_{Co}, and ΔV_{Co} is the voltage ripple of the output capacitor.

7. Small Signal Modeling and Control Scheme

Figure 11 shows the voltage loop control scheme of the DS-HS converter. The most important part of closed-loop control is the design of the compensation network, and the

design of the compensation network requires a small signal model as shown in the following figure.

Assuming that the inductance and capacitance are large enough, the small-signal model can be obtained using the state-space averaging method. $U_i(t)$, $U_o(t)$, and $d(t)$ are input variable, output variable, and control variable, respectively. $i_{L1}(t)$, $i_{L2}(t)$, $U_{C1}(t)$, $U_{C2}(t)$, and $U_{Co}(t)$ are state variables. The equivalent series resistance of capacitors C_1 and C_2 is r. When switches S_1 and S_2 are turned on, the state space average model can be obtained as follows:

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dU_{C1}(t)}{dt} \\ \frac{dU_{C2}(t)}{dt} \\ \frac{dU_{Co}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{2rC1} & \frac{1}{2rC1} & -\frac{1}{2rC1} \\ 0 & 0 & \frac{1}{2rC2} & \frac{1}{2rC2} & -\frac{1}{2rC2} \\ 0 & 0 & -\frac{1}{2rCo} & -\frac{1}{2rC_o} & \frac{1}{2rC_o} + \frac{1}{R_oC_o} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ U_{C1}(t) \\ U_{C2}(t) \\ U_{Co}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L1} \\ \frac{1}{L2} \\ 0 \\ 0 \\ 0 \end{bmatrix} U_i(t),$$
$$U_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & U_{C1}(t) & U_{C2}(t) & U_{Co}(t) \end{bmatrix}^T. \tag{74}$$

When S_1 and S_2 are turned off, the state space average model can be written as follows:

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dU_{C1}(t)}{dt} \\ \frac{dU_{C2}(t)}{dt} \\ \frac{dU_{Co}(t)}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r}{4L1} & 0 & -\frac{1}{2L1} & 0 & 0 \\ -\frac{r}{4L2} & 0 & -\frac{1}{2L2} & 0 & 0 \\ -\frac{1}{2C1} & 0 & 0 & 0 & 0 \\ -\frac{1}{2C2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{R_oC_o} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ U_{C1}(t) \\ U_{C2}(t) \\ U_{Co}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{2L1} \\ \frac{1}{2L2} \\ 0 \\ 0 \\ 0 \end{bmatrix} U_i(t),$$
$$U_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & U_{C1}(t) & U_{C2}(t) & U_{Co}(t) \end{bmatrix}^T. \tag{75}$$

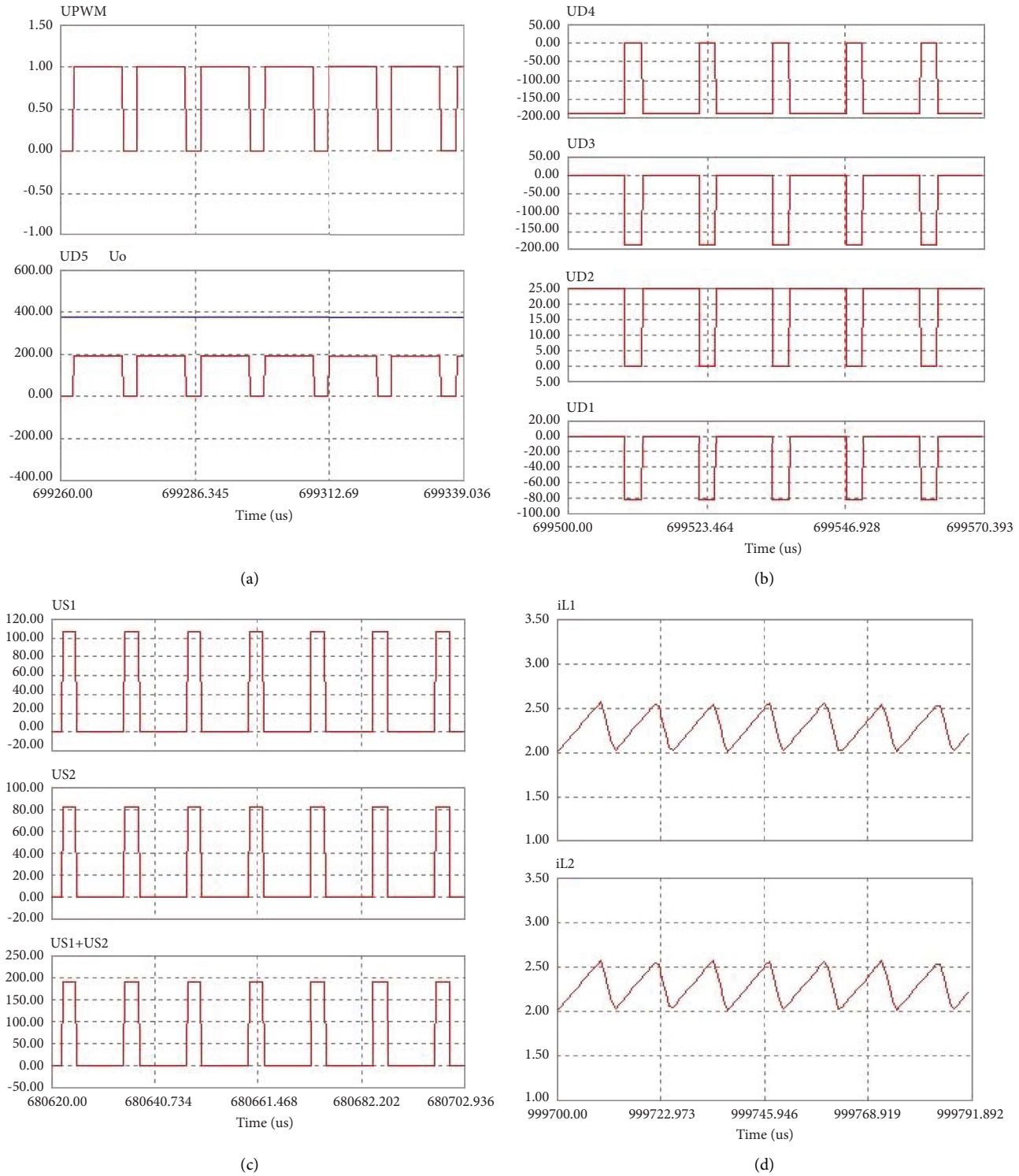


FIGURE 12: Simulation results when $V_i = 25$ V. (a) U_{PWM}, U_o, and U_{D5}, (b) U_{D4}, U_{D3}, $U_{D2,}$ and U_{D1}, (c) U_{S2}, U_{S1}, and $U_{S2} + U_{S1}$, and (d) currents of L1 and L2.

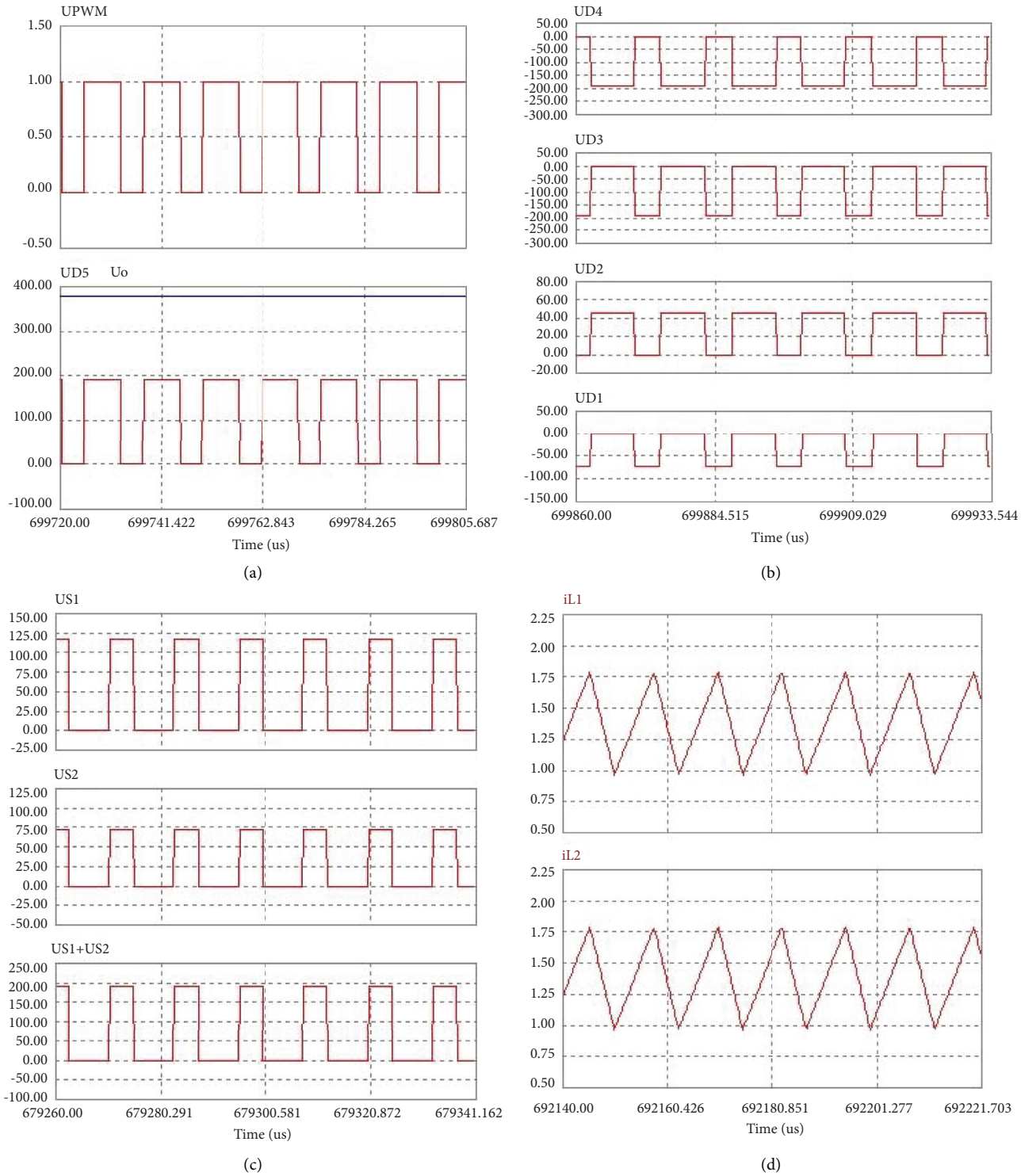
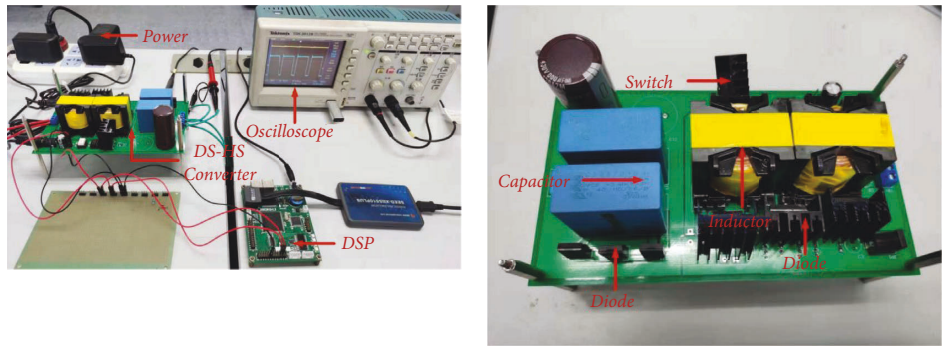


Figure 13: Simulation results when $V_i = 45$ V. (a) U_{PWM}, $U_{o,}$ and U_{D5}, (b) U_{D4}, U_{D3}, $U_{D2,}$ and U_{D1}, (c) U_{S2}, U_{S1}, and $U_{S2} + U_{S1}$, and (d) currents of L_1 and L_2.



(a) (b)

Figure 14: The DS-HS converter. (a) The experimental prototype and (b) the enlarged figure.

Combining (74) and (75), the average model of the DS-HS converter can be obtained as follows:

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dU_{C1}(t)}{dt} \\ \frac{dU_{C2}(t)}{dt} \\ \frac{dU_{Co}(t)}{dt} \end{bmatrix} = \begin{bmatrix} \frac{r(1-d(t))}{4L1} & 0 & -\frac{1-d(t)}{2L1} & 0 & 0 \\ \frac{r(1-d(t))}{4L2} & 0 & -\frac{1-d(t)}{2L2} & 0 & 0 \\ -\frac{1-d(t)}{2C1} & 0 & \frac{d(t)}{2rC1} & \frac{d(t)}{2rC1} & -\frac{d(t)}{2rC1} \\ -\frac{1-d(t)}{2C2} & 0 & \frac{d(t)}{2rC2} & \frac{d(t)}{2rC2} & -\frac{d(t)}{2rC2} \\ 0 & 0 & -\frac{1}{2rCo} & -\frac{1}{2rC_o} & \frac{1}{2rC_o}+\frac{1}{R_oC_o} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ U_{C1}(t) \\ U_{C2}(t) \\ U_{Co}(t) \end{bmatrix} + \begin{bmatrix} \frac{1+d(t)}{2L1} \\ \frac{1+d(t)}{2L2} \\ 0 \\ 0 \\ 0 \end{bmatrix} U_i(t),$$

$$U_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & U_{C1}(t) & U_{C2}(t) & U_{Co}(t) \end{bmatrix}^{\mathrm{T}}. \tag{76}$$

State variables, input variables, output variables, and control variables can be described as follows:

$$\begin{aligned} i_{L1}(t) &= I_{L1} + \hat{i}_{L1}(t), \\ i_{L2}(t) &= I_{L2} + \hat{i}_{L2}(t), \\ U_{C1}(t) &= U_{C1} + \hat{U}_{C1}(t), \\ U_{C2}(t) &= U_{C2} + \hat{U}_{C2}(t), \\ U_{Co}(t) &= U_{Co}, \\ U_o(t) &= U_o + \hat{U}_o(t), \\ U_i(t) &= U_i + \hat{U}_i(t), \\ d(t) &= D + \hat{d}(t), \end{aligned} \tag{77}$$

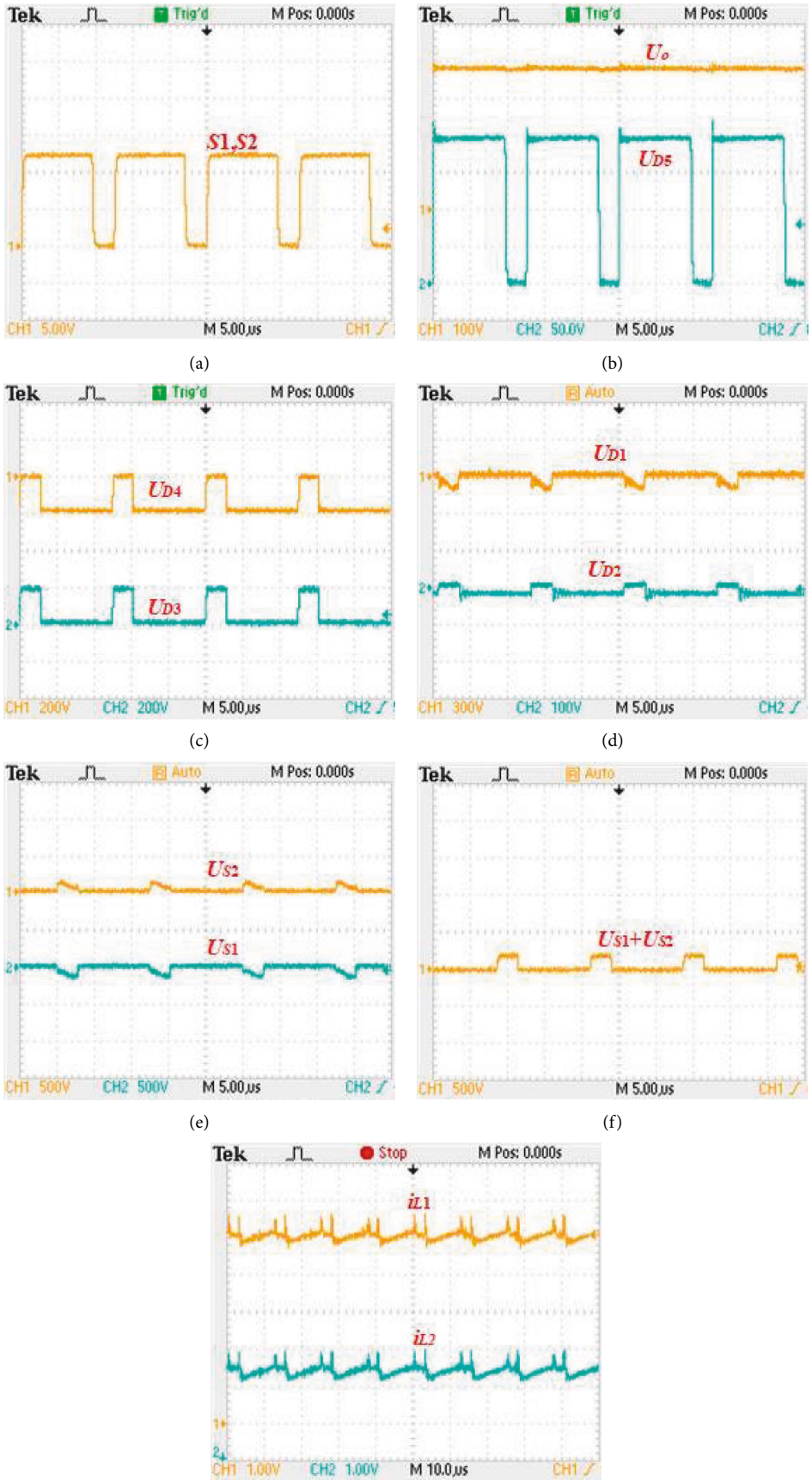


FIGURE 15: Experimental results when $U_i = 25$ V. (a) Drive signal of S_1, S_2, (b) U_o and U_{D5}, (c) U_{D4} and U_{D3}, (d) U_{D1} and U_{D2}, (e) U_{S2} and U_{S1}, (f) $U_{S2} + U_{S1}$, and (g) currents of L_1 and L_2.

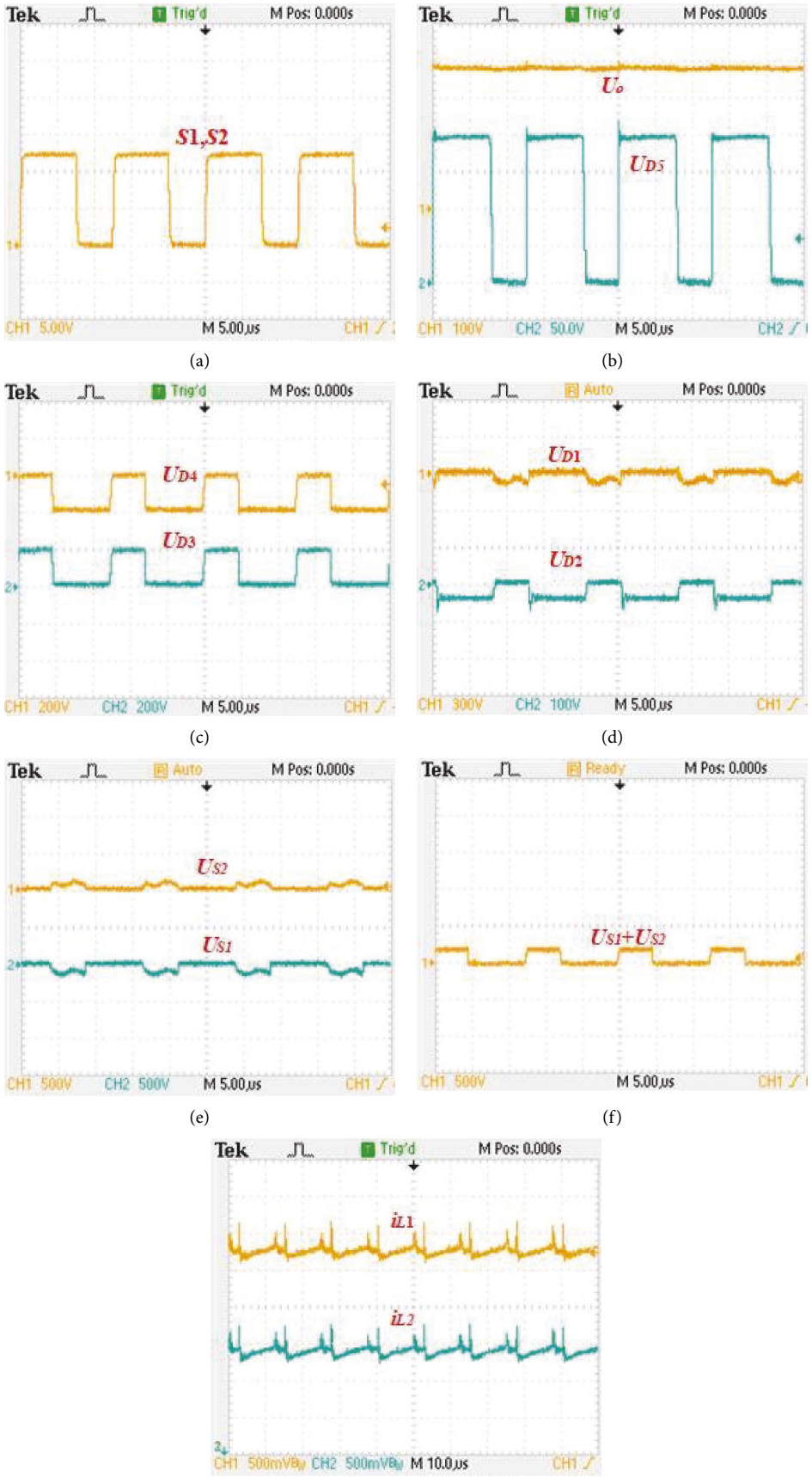


FIGURE 16: Experimental results when $U_i = 45$ V. (a) Drive signal of S1, S2, (b) U_o and U_{D5}, (c) U_{D4} and U_{D3}, (d) U_{D1} and U_{D2}, (e) U_{S2} and U_{S1}, (f) $U_{S2} + U_{S1}$, and (g) currents of L1 and L2.

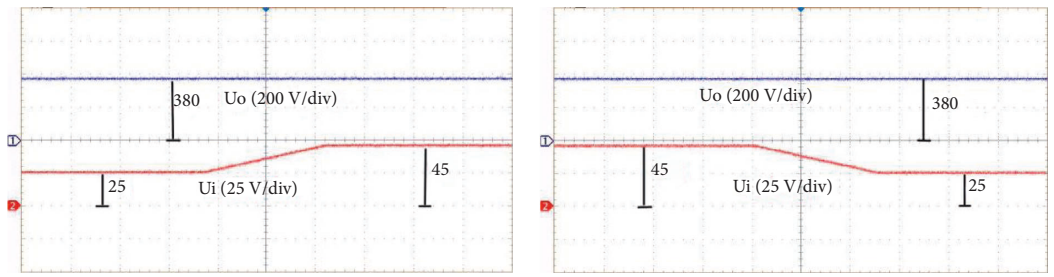


FIGURE 17: The waveforms of U_o, when U_i changes. (a) U_i changes from 25 V to 45 V, (b) U_i changes from 45 V to 25 V.

where I_{L1}, I_{L2}, U_{C1}, U_{C2}, U_{Co}, $U_{i,}$ and D are the steady-state components; $\hat{i}_{L1}(t)$, $\hat{i}_{L2}(t)$, $\hat{U}_{C1}(t)$, $\hat{U}_{C2}(t)$, $\hat{U}_{Co}(t)$, $\hat{U}_i(t)$, $\hat{d}(t)$, and $\hat{U}_o(t)$ are the small-signal disturbance variables.

Combining equations (76) and (77), the small-signal model of the converter can be written as follows:

$$\begin{bmatrix} d\hat{i}_{L1}(t) \\ d\hat{i}_{L2}(t) \\ d\hat{U}_{C1}(t) \\ d\hat{U}_{C2}(t) \\ d\hat{U}_{Co}(t) \end{bmatrix} = \begin{bmatrix} -\frac{r(1-D)}{4L1} & 0 & -\frac{1-D}{2L1} & 0 & 0 \\ -\frac{r(1-D)}{4L2} & 0 & -\frac{1-D}{2L2} & 0 & 0 \\ -\frac{1-D}{2C1} & 0 & \frac{D}{2rC1} & \frac{D}{2rC1} & -\frac{D}{2rC1} \\ -\frac{1-D}{2C2} & 0 & \frac{D}{2rC2} & \frac{D}{2rC2} & -\frac{D}{2rC2} \\ 0 & 0 & -\frac{D}{2rCo} & -\frac{D}{2rC_o} & \frac{D}{2rC_o}+\frac{1}{R_oC_o} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{U}_{C1}(t) \\ \hat{U}_{C2}(t) \\ \hat{U}_{Co}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{2L1} \\ \frac{1}{2L2} \\ 0 \\ 0 \\ 0 \end{bmatrix} U_i\hat{d}(t)$$

$$+ \begin{bmatrix} \frac{D}{L1}+\frac{1-D}{2L1} \\ \frac{D}{L2}+\frac{1-D}{2L2} \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{U}_i(t) + \begin{bmatrix} \frac{r}{4L1} & 0 & \frac{1}{2L1} & 0 & 0 \\ \frac{r}{4L2} & 0 & \frac{1}{2L2} & 0 & 0 \\ \frac{1}{2C1} & 0 & \frac{1}{2rC1} & \frac{1}{2rC1} & -\frac{1}{2rC1} \\ \frac{1}{2C2} & 0 & \frac{1}{2rC2} & \frac{1}{2rC2} & -\frac{1}{2rC2} \\ 0 & 0 & -\frac{1}{2rC_o} & -\frac{1}{2rC_o} & \frac{1}{2rC_o} \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ U_{C1} \\ U_{C2} \\ U_{C_o} \end{bmatrix} \hat{d}(t), \quad (78)$$

$$\hat{U}_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \left[\hat{i}_{L1}(t) \;\; \hat{i}_{L2}(t) \;\; \hat{U}_{C1}(t) \;\; \hat{U}_{C2}(t) \;\; \hat{U}_{Co}(t) \right]^T.$$

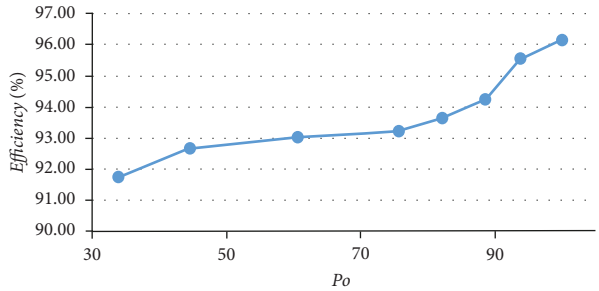


Figure 18: The efficiency of the DS-HS converter, when $U_i = 25$ V.

8. Simulation Results

In order to verify the correctness of the DS-HS converter, a simulation is carried out. The design index and component parameters are shown in Table 3, with an output power of 100 W, an input voltage of 25 V–45 V, and an output voltage of 380 V.

When the input voltage is 25 V and the output voltage is 380 V, the simulation waveforms are shown in Figure 12. The drive signal of the switches S_1 and S_2, output voltage, and the voltage stress of the diode D_5 are shown in Figure 12(a). The voltage stresses of the diodes D_1–D_4 are shown in Figure 12(b). From Figures 12(a) and 12(b), it is obvious that the output voltage is 380 V, and the voltage stresses of the diodes D_3, D_4, and D_5 are half of the output voltage, 190 V. The voltage stress of D_1 is about 82.5 V, and the voltage stress of D_2 is equal to the input voltage, which is about 25 V. The voltage stresses of S_1 and S_2 and the sum of the voltage stresses of S_1 and S_2 are shown in Figure 12(c). The current stress of the inductor current is shown in Figure 12(d), and the average currents of L_1 and L_2 are 2.26 A.

When the input voltage is 45 V and the output voltage is 380 V, the simulation waveforms are shown in Figure 13. The drive signal of the switches S_1 and S_2, output voltage, and the voltage stress of the diode D_5 are shown in Figure 13(a). The voltage stresses of the diodes D_1–D_4 are shown in Figure 13(b), then the voltage stresses of S_1 and S_2 and the sum of the voltage stresses of S_1 and S_2 are shown in Figure 13(c). The current stress of the inductor current is shown in Figure 13(d), and the average currents of L_1 and L_2 are 1.37 A.

9. Experimental Results

For the sake of verifying the correctness of the above analysis for the DS-HS converter, the experimental prototype of the DS-HS converter is built, shown in Figure 14(a), composed of a power supply, DSP, oscilloscope, and DS-HS converter. The enlarged figure of the DS-HS converter is shown in Figure 14(b), which consists of inductors, capacitors, switches and diodes, and so on.

When the input voltage of the DS-HS converter is 25 V and the output voltage is 380 V, the experimental results are shown in Figure 15. The drive signal of the switches S_1 and S_2 for the DS-HS converter is shown in Figure 15(a). The output voltage and the voltage stress of diode D_5 are shown in Figure 15(b), and the voltage stresses of the diodes D_3 and D_4 are shown in Figure 15(c). From Figures 15(b) and 15(c), it is obvious that the output voltage is 380 V, and the voltage stresses of the diodes D_3, D_4, and D_5 are half of the output voltage, 190 V. The voltage stresses of the diodes D_1 and D_2 are revealed in Figure 15(d). The voltage stress of D_1 is about 82.5 V, and the voltage stress of D_2 is equal to the input voltage, which is about 25 V. The voltage stresses of S_1 and S_2 are shown in Figure 15(e), and the sum of the voltage stresses of S_1 and S_2 is shown in Figure 15(f), which is half of the output voltage, 190 V. The current stress of the inductor current is shown in Figure 15(g), and the average currents of L_1 and L_2 are 2.3 A and 2.3 A.

When the input voltage of the DS-HS converter is 45 V and the output voltage is 380 V, the experimental results are shown in Figure 16. The driving signal of switches S_1 and S_2 is shown in Figure 16(a), and the output voltage and the voltage of D_5 are shown in Figure 16(b). The voltage stresses of D_3, D_4, D_1, and D_2 are shown in Figures 16(c) and 16(d). The voltage stresses of S_1 and S_2 are shown in Figure 16(e), and the sum of the voltage stresses of S_1 and S_2 is shown in Figure 16(f), which is half of the output voltage, 190 V. The current of inductors L_1 and L_2 is shown in Figure 16(g), and the average currents of L_1 and L_2 are about 1.33 A and 1.33 A.

As shown in Figure 17(a), when the input voltage of the DS-HS converter changes from 25 V to 45 V, the output voltage remains around 380 V, and the DS-HS converter can achieve a gain range from 8.4 to 15.2. As shown in Figure 17(b), when the input voltage of the HS-LC converter drops from 45 V to 25 V, the output voltage remains around 380 V, and the DS-HS converter can achieve a gain range from 15.2 to 8.4.

The efficiency of the DS-HS converter is shown in Figure 18, when $U_i = 25$ V. It can be seen from Figure 18 that the efficiency of the DS-HS converter increases as the power increases, and the efficiency can reach up to 96.15%. In addition, the DS-HS converter also has some limitations. The input and output do not share the same ground, which will cause an electromagnetic interference problem. Because the DS-HS converter does not use soft switching, voltage and current spikes will be generated which results in power loss when the switch is switched.

10. Conclusion

The improved switching-inductor unit and new step-up DC-DC converters with reduced switch voltage stress are proposed. Through filtering of characteristics, the DS-HS converter is selected from the proposed converters. The voltage gain of the DS-HS converter in CCM, the nonideal effects of components, and the efficiency analysis are analyzed. The design criteria for components and small signal modeling and control are given. By the comparison of the existing converters, it can be shown that the DS-HS converter has lower voltage stress, higher voltage gain, and higher efficiency. The actual circuit of the DS-HS converter is built to verify the correctness of the theory. The simulation and experimental results of the DS-HS converter are presented, and the efficiency can reach 96.15%.

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

This work was financially supported by the National Natural Science Foundation of China (61873180).

References

[1] M. Al-Greer, M. Armstrong, M. Ahmeid, and D. Giaouris, "Advances on system identification techniques for DC-DC switch mode power converter applications," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6973–6990, 2019.

[2] A. Leon-Masich, H. Valderrama-Blavi, J. Bosque-Moncusí, and L. MartínezSalamero, "A high-voltage SiC-based boost PFC for LED applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1633–1642, 2016.

[3] M. S. Bhaskar, R. Alammari, M. Meraj, S. Padmanaban, and A. Iqbal, "A new triple-switch-triple-mode high step-up converter with wide range of duty cycle for DC microgrid applications," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 7425–7441, 2019.

[4] S. K. Kao, J. H. Wu, and H. C. Cheng, "All-digital controlled boost DC-DC converter with all-digital DLL-based calibration," *Microelectronics Journal*, vol. 46, no. 10, pp. 970–980, 2015.

[5] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC-DC converters: a comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9143–9178, 2017.

[6] H. Yeşilyurt and H. Bodur, "New active snubber cell for high power isolated PWM DC-DC converters," *IET Circuits, Devices and Systems*, vol. 13, no. 6, pp. 822–829, 2019.

[7] J. Kwon and B. Kwon, "High step-up active-clamp converter with InputCurrent doubler and output-voltage doubler for fuel cell power systems," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 108–115, 2009.

[8] K. B. Park, G. W. Moon, and M. J. Youn, "Nonisolated high step-up boost converter integrated with sepic converter," *IEEE Transactions on Power Electronics*, vol. 25, no. 9, pp. 2266–2275, 2010.

[9] S. Dwari and L. Parsa, "An efficient high-step-up interleaved DC-DC converter with a common active clamp," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 66–78, 2011.

[10] H. C. Liu and F. Li, "Novel high step-up DC-DC converter with an active coupled-inductor network for a sustainable energy system," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6476–6482, 2015.

[11] Y. P. Siwakoti and F. Blaabjerg, "Single switch nonisolated ultra-step-up DC-DC converter with an integrated coupled inductor for high boost applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8544–8558, 2017.

[12] F. L. Tofoli, D. d. C. Pereira, W. Josias de Paula, and D. d. S. Oliveira Júnior, "Survey on non-isolated highvoltage step-up dc-dc topologies based on the boost converter," *IET Power Electronics*, vol. 8, no. 10, pp. 2044–2057, 2015.

[13] A. Mustafa and S. Mekhilef, "Dual phase LLC resonant converter with variable frequency zero circulating current phase-shift modulation for wide input voltage range applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 2793–2807, 2021.

[14] S. M. S. I. Shakib and S. Mekhilef, "A frequency adaptive phase shift modulation control based LLC series resonant converter for wide input voltage applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8360–8370, 2017.

[15] S. M. S-I-S, M. Saad, and N. Mutsuo, "Dual bridge LLC resonant converter with frequency adaptive phase-shift modulation control for wide voltage gain range," in *Proceedings of the 2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, USA, October 2017.

[16] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/SwitchedInductor structures for getting transformerless hybrid DC-DC PWM converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 2, pp. 687–696, 2008.

[17] Y. Jiao, F. L. Luo, and B. K. Bose, "Voltage-lift split-inductor-type boost converters," *IET Power Electronics*, vol. 4, no. 4, pp. 353–362, 2011.

[18] O. Abutbul, A. Gherlitz, Y. Berkovich, and A. Ioinovici, "Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 50, no. 8, pp. 1098–1102, 2003.

[19] L. S. Yang, T. J. Liang, and J. F. Chen, "Transformerless DC-DC converters with high step-up voltage gain," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 8, pp. 3144–3152, 2009.

[20] L. L. Liu, D. H. Li, and L. L. Yao, "Non-isolated high step-up DC-DC conversion circuits for photovoltaic system," *International Transactions on Electrical Energy Systems*, vol. 30, no. 2, pp. 1–18, 2019.

[21] Y. Tang, T. Wang, and D. Fu, "Multicell switched-inductor/switched-capacitor combined active-network converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2063–2072, 2015.

[22] V. A. K. Prabhala, P. Fajri, V. S. P. Gouribhatla, B. P. Baddipadiga, and M. Ferdowsi, "A DC-DC converter with high voltage gain and two input boost stages," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4206–4215, 2016.

[23] E. Babaei, H. Mashinchi Maheri, M. Sabahi, and S. H. Hosseini, "Extendable nonisolated high gain DC-DC converter based on active-passive inductor cells," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 12, pp. 9478–9487, 2018.

[24] F. Mohammadzadeh Shahir, E. Babaei, and M. Farsadi, "Analysis and design of voltage-lift technique-based non-isolated boost dc-dc converter," *IET Power Electronics*, vol. 11, no. 6, pp. 1083–1091, 2018.

[25] R. Gules, W. M. dos Santos, F. A. dos Reis, E. F. R. Romaneli, and A. A. Badin, "A modified SEPIC converter with high static gain for renewable applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 5860–5871, 2014.

[26] K. R. Li, Y. F. Hu, and A. Ioinovici, "Generation of the large DC gain step-up nonisolated converters in conjunction with renewable energy sources starting from a proposed geometric structure," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5323–5340, 2017.

[27] G. Wu, X. B. Ruan, and Z. H. Ye, "Nonisolated high step-up DC-DC converters adopting switched-capacitor cell," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 383–393, 2015.