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Research Article

A Novel Nearest Level Modulation Method with Increased Output Voltage Quality for Modular Multilevel Converter Topology

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The modular multilevel converter (MMC) topology is gaining more interest because of its modular design, high efficiency, and scalable voltage levels in medium- and high-power industrial applications, where the nearest level modulation (NLM) method is frequently preferred. In this paper, a novel NLM method is proposed with increased output voltage quality for MMC topology. In conventional NLM (C-NLM), output voltage is obtained as $N + 1$ levels, where N is the number of submodules (SMs) per arm. The output voltage is increased to $2N + 1$ levels by the proposed NLM method without using any additional SMs. The proposed NLM method is based on the offset term injection, which is optimally determined in terms of the best output performance of MMC. Also, trapezoidal reference signal is used instead of sinusoidal reference, which provides better output voltage quality and controls the modulation process. The proposed NLM method presents simple implementation as in the C-NLM, and it is implemented to the upper and lower arms of the MMC; then, arm voltages are successfully controlled. Furthermore, output voltage returns the value of zero in the C-NLM process for low-modulation-ratio applications in relatively small amount of SM usage of MMC design. However, the proposed NLM method gives promising results instead of zero voltage. In order to validate the superior performance of the proposed NLM method, a comparative study is presented with C-NLM and third-harmonic injected NLM method in terms of total harmonic distortion (THD) and magnitude of the output voltage and current. THD of output waveforms of MMC is significantly reduced, and DC voltage utilization is remarkably increased, thanks to the proposed NLM method. In addition, capacitor voltage balancing for the proposed NLM method is accomplished to keep the capacitor voltage of each SM of MMC constant. Simulation results are presented to verify the effectiveness of the proposed NLM method under various case studies. Finally, experimental validation is carried out using a field programmable gate array (FPGA)-based hardware implementation on the laboratory prototype to show the applicability of the proposed NLM method.

1. Introduction

1.1. Overview. Voltage source converters (VSCs) have been increasingly adopted in medium-/high-power industrial applications as a key power electronic interface for decades. In comparison with the two-level and three-level VSCs, the multilevel converters (MCs) have the advantages such as high output voltage and current quality, reduced output filter size, and high availability and efficiency. MCs are also operated in higher voltage/power levels [1–5]. As a new type of MCs, the modular multilevel converter (MMC) was first designed by Lesnicar and Marquardt in 2003 [6]. Since the invention of the MMC, it has been used as an attractive power converter topology due to its distinguished benefits in terms of availability, high efficiency, and scalability in many industrial applications [7–9]. The main application areas of MMC include high-voltage direct current (HVDC) systems [10], battery energy storage systems with electrical vehicles [11–13], high-power motor drives [14], static synchronous compensator [15], renewable energy system integrations incorporating wind energy conversion system [16] and solar photovoltaic system [17], power electronic transformer [18], and electrical ship and railway traction implementation [19, 20]. Recently, scholars have attempted research by

focusing the mathematical modeling [21], circuit topology [22], modulation techniques [23], control objectives [24], capacitor voltage balancing [25], precharging for start-up [26] issues, arm current control [27], and circulating current suppression [28] for MMC-based applications.

1.2. Literature Review. Over the years, various modulation methods have been introduced to control the MMCs such as phase-shifted pulse width modulation (PWM) [29], level-shifted PWM [2], space vector modulation [30], selective harmonic elimination [31], and nearest level modulation (NLM) [32]. These methods are investigated by the researchers in a comparative way in the literature [33, 34]. NLM, which is known as carrier-less method, receives wider acceptance over the carrier-based methods, thanks to the flexible and easy implementation in MMC-based power electronic applications. However, the conventional NLM (C-NLM) is mostly adopted by MMC applications with a relatively large number of SMs for the reason of providing satisfactory output quality [35, 36]; on the contrary, it gives poorer output waveforms for MMC with a low number of submodules (SMs). To improve the output voltage quality using the NLM method, several publications have been presented in the existing literature. Most of them have been tested for MMC with a large number of SMs. In [37], output voltage quality can be boosted by combining the NLM and carrier-based PWM method, which causes increase in the switching losses compared with the C-NLM method. The main objective of [38] is to introduce a new NLM method for improving output performance of MMC with increase in the level number. Feasibility of the proposed method is confirmed by simulation results by comparing it with C-NLM for MMC with a large number of SMs. Another NLM method is suggested to increase the voltage level using sinusoidal signal reference and modified rounding function in [39]. The developed method is verified by both simulation and experiment using 10 SMs per arm for high modulation ratio. Research presented in [40] addresses the third-harmonic injection-based total harmonic distortion (THD) reduction scheme by comparing it with C-NLM. Simulation study and hardware in the loop-based experimental system are used to confirm the effectiveness of the proposed scheme using 30 SMs per arm for high modulation ratio. In the meantime, the authors of [41] develop an improved NLM method by considering a system of first-order two-variable equations for circulating current suppression with a low number of SMs. The proposed method is tested by the simulation and experimental prototype in a single-phase MMC system. Moreover, an enhanced NLM method is presented by adding a small offset in [42], which is based on alternating at the double fundamental frequency to the reference signals and shown using 8 SMs per arm for high modulation ratio in simulation and experimental hardware. Although methods for harmonic reduction are studied in [43, 44], they need more computations for the modulation of MMCs.

Aforementioned NLM methods can boost the level number of the output voltage and keep the switching frequency unaffected. On the other hand, they lead to some difficulties such as increasing the capacitor voltage ripple of each SM, arm inductor voltage peak, and computation complexity. Also, they do not consider the low-modulation-ratio applications for MMC with a low number of SMs.

1.3. Key Contributions. Considering the issues mentioned in the Literature Review section, this paper develops a novel NLM method with increased output voltage quality for MMC topology. The proposed NLM method is based on the offset term injection, which is optimally determined in terms of the best output performance of MMC. Trapezoidal reference signal is implemented instead of sinusoidal reference, which ensures better output voltage quality and controls the modulation process. The main contributions of the proposed NLM method are listed as follows:

(1) The output voltage waveform is boosted to $2N + 1$ levels without using any additional SMs.

(2) The proposed NLM method presents simple implementation as in the C-NLM, and it is implemented to the upper and lower arms of the MMC topology; then, arm voltages are successfully controlled.

(3) Compared with the C-NLM and third-harmonic injected NLM method, THD of MMC output parameters is significantly mitigated and DC voltage utilization is considerably increased, thanks to the proposed NLM method.

(4) The proposed NLM method gives convincing results instead of zero voltage in contrast to C-NLM process in low-modulation-ratio applications for MMC with a low number of SMs.

(5) Capacitor voltage balancing for the proposed NLM method is succeeded to keep the capacitor voltage of each SM of MMC constant.

The remaining part of the paper proceeds as follows: Section 2 describes the MMC circuit topology. C-NLM and the proposed NLM method are provided in detail in Sections 3 and 4, respectively. Section 5 presents the findings of the research to show the acceptability of the proposed NLM method under various cases in the simulation environment. In Section 6, experimental results are provided using a field programmable gate array (FPGA)-based hardware implementation on the laboratory prototype to demonstrate the practicality of the proposed NLM method. Finally, the conclusions of the research are given in Section 7.

2. Modeling and Operation of the MMC Topology

A three-phase circuit structure of the MMC is depicted in Figure 1. The MMC circuit has a DC link, which can be fed from a DC voltage source or a renewable energy source. In the MMC topology, there are three phases (legs) and two arms per phase called as the upper and lower arm. N series-connected identical SMs and an arm inductor are included in each arm as shown in Figure 1. The DC capacitor and two switching components with antiparallel diodes are placed in

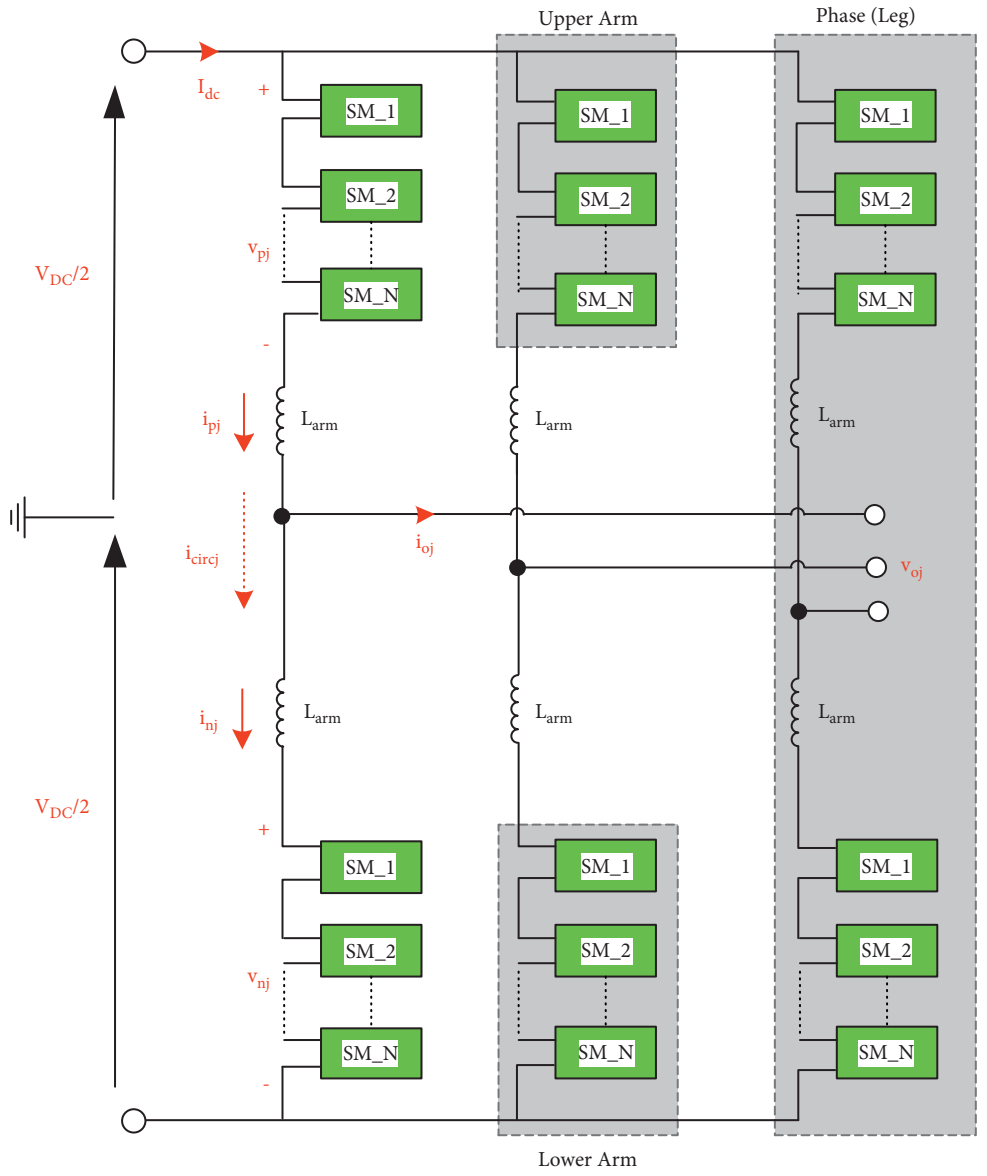


Figure 1: Three-phase circuit configuration of the MMC topology.

each SM, which is defined as half-bridge SM (HBSM) and represented in Figure 2. HBSM is frequently used in MMC-based applications owing to the easy control capability [45, 46]. In HBSM, two outputs are available as V_C and 0. Table 1 describes the switching logics of HBSM, where i_{ij} denotes the arm current. Power switching devices S_1 and S_2 operate in the opposite manner. According to this operation, if switch S_1 is conducting, SM becomes ON and gives V_C in the output. Conversely, if switch S_2 is conducting, SM becomes OFF and gives 0 in the output. In this regard, arm voltages are controlled by regulating N_{ON}, where it expresses the number of active (ON) SMs in the upper and lower arm. In the event of all capacitor voltages in each SM being balanced and equal to V_C, the actual arm voltage is computed by the equation as follows:

$$v_{ij} = N_{ON,ij} \times V_C \quad (i = p, n;\ j = a, b, c), \tag{1}$$

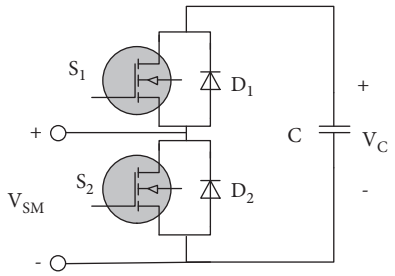


Figure 2: HBSM power cell.

where p and n denote the upper and lower arm in phase j, respectively. Applying Kirchhoff's current law to the MMC circuit, the output AC current can be obtained as

$$i_{oj} = i_{pj} - i_{nj}. \tag{2}$$

Table 1: Switching logics of HBSM.

S_1	S_2	i_{ij}	Capacitor	V_{SM}
1	0	Positive	Charging	V_C
1	0	Negative	Discharging	V_C
0	1	Positive	Unchanged	0
0	1	Negative	Unchanged	0

The half of the summation of the upper and lower arm current corresponds to the circulating current in phase j, which is expressed as

$$i_{circj} = \frac{i_{pj} + i_{nj}}{2}. \tag{3}$$

The circulating current does not affect the DC and AC side of the MMC circuit. However, the voltage ripple of the SM capacitors and arm current can increase if it is too high. When arm energy balancing is efficiently achieved, thanks to the capacitor voltage balancing and suitable sized arm inductor used on the upper and lower arm, no problem arises owing to the circulating current. Applying Kirchhoff's voltage law to the MMC circuit, after the simplifications, the output AC voltage can be defined as

$$V_{oj} = \frac{V_{nj} - V_{pj}}{2} - L_{arm}\frac{\mathrm{d}i_{oj}(t)}{\mathrm{d}t}. \tag{4}$$

The voltage drops on the arm inductors are negligible, which results in the output voltage as follows:

$$V_{oj} = \frac{N_{ON,nj} - N_{ON,pj}}{2} \times V_C. \tag{5}$$

3. Conventional NLM Method

Staircase modulation is the other name of the NLM, which is preferred for MMC applications due to its flexible and simple implementation [47, 48]. Figure 3 shows the basic principle of the C-NLM. Each arm could be controlled separately by using this method. The control scheme of the C-NLM is represented in Figure 4. Another NLM method discussed in the literature is the third-harmonic injected NLM method, which is implemented by injecting the third-harmonic component to the reference waveform [49, 50]. In C-NLM, output performance of MMC is more preferable when the number of SMs in the upper and lower arm is more than enough count. Otherwise, when a few SMs are used in the arms for low modulation ratios, no output voltage is obtained on the AC side of MMC since round function continuously gives the same value during the operation of the NLM process. Therefore, according to equation (5), the output voltage is obtained as nearly zero.

The single-phase circuit structure of MMC is given in Figure 5. Mathematical modeling required for the modulation of phase-a of MMC is presented in the following formulas. Arm voltages can be defined as

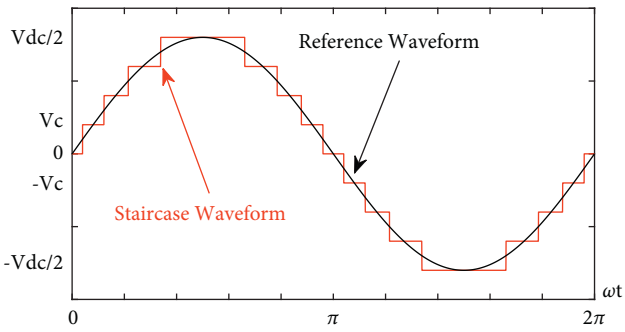


Figure 3: Basic concept of C-NLM.

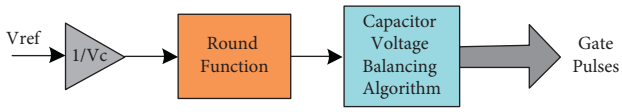


Figure 4: Control structure of C-NLM.

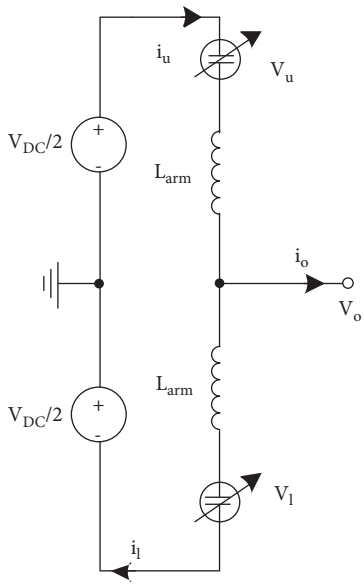


Figure 5: Single-phase equivalent circuit diagram of MMC.

$$V_u = \frac{V_{DC}}{2} - V_o - L_{arm}\frac{\mathrm{d}i_u}{\mathrm{d}t}, \tag{6a}$$

$$V_l = \frac{V_{DC}}{2} + V_o - L_{arm}\frac{\mathrm{d}i_l}{\mathrm{d}t}. \tag{6b}$$

If the arm inductor voltages are symbolized with v_x, the arm equations can be expressed as follows:

$$V_u = \frac{V_{DC}}{2} - V_o - v_x, \tag{7a}$$

$$V_l = \frac{V_{DC}}{2} + V_o - v_x, \tag{7b}$$

where v_x denotes the voltage drop on the arm inductor. The phase voltage for single-phase MMC topology can be formulated by

$$V_o = \mathrm{MI}\frac{V_{DC}}{2}\sin(\omega t + \theta), \tag{8}$$

where MI, ω, and θ are the modulation index, fundamental angular frequency, and phase angle, respectively. Arm voltages are stated for the upper and lower arm using equations (7a), (7b), and (8) as

$$V_u = \frac{V_{DC}}{2} - \mathrm{MI}\frac{V_{DC}}{2}\sin(\omega t + \theta), \tag{9a}$$

$$V_l = \frac{V_{DC}}{2} + \mathrm{MI}\frac{V_{DC}}{2}\sin(\omega t + \theta). \tag{9b}$$

SM capacitor voltage can be expressed using the design principle of MMC as

$$V_{DC} = \mathrm{N}V_c. \tag{10}$$

Replacing (10) into (9a) and (9b) gives

$$V_u = \frac{\mathrm{N}V_c}{2} - \mathrm{MI}\frac{\mathrm{N}V_c}{2}\sin(\omega t + \theta), \tag{11a}$$

$$V_l = \frac{\mathrm{N}V_c}{2} + \mathrm{MI}\frac{\mathrm{N}V_c}{2}\sin(\omega t + \theta), \tag{11b}$$

where V_c denotes the step value of output voltage. After normalization, general forms are deduced for upper and lower arm voltage as

$$V_u^n = \frac{N}{2}[1 - \mathrm{MI}\sin(\omega t + \theta)], \tag{12a}$$

$$V_l^n = \frac{N}{2}[1 + \mathrm{MI}\sin(\omega t + \theta)]. \tag{12b}$$

The voltage level of instantaneous arm voltage of the upper and lower arm is obtained using round function at each sampling cycle as follows:

$$V_{level\_u}^n = \mathrm{round}(V_u^n), \tag{13a}$$

$$V_{level\_l}^n = \mathrm{round}(V_l^n). \tag{13b}$$

Round function can be expressed in a mathematical form by

$$\mathrm{round}(x) = \begin{cases} \mathrm{floor}(x); & x < \mathrm{floor}(x) + 0.5 \\ \mathrm{ceil}(x); & x \geq \mathrm{floor}(x) + 0.5 \end{cases}, \tag{14}$$

where floor (x) denotes the largest integer less than x while ceil (x) represents the smallest integer greater than x.

4. The Proposed NLM Method

In the proposed NLM method, a trapezoidal signal is used instead of sinusoidal signal as a reference waveform to obtain improved output quality and control the modulation process. A trapezoidal waveform can be considered as an intermediate shape between a square and a triangular wave [51]. A typical representation of a trapezoidal signal is given in Figure 6. There are four main parts including rise time (t_r), high time (t_H), fall time (t_f), and low time (t_L) in this waveform. While the signal remains at its maximum level (+MI) during t_H, it remains at its minimum level (−MI) during t_L. Also, the signal increases linearly from the minimum level to the maximum level during t_r, whereas it decreases linearly from the maximum level to minimum level during t_f. Fundamental period (T) of the trapezoidal signal is formed by the summation of these four parts:

$$T = t_r + t_H + t_f + t_L. \tag{15}$$

In symmetrical waveform of the trapezoidal signal, these parts satisfy the following relations:

$$t_H = t_L, \tag{16a}$$

$$t_r = t_f. \tag{16b}$$

While a square wave signal is obtained when $t_r = t_f = 0$ meaning that $t_H = t_L = T/2$, a triangular signal is captured when $t_r = t_f = T/2$ meaning that $t_H = t_L = 0$. A trapezoidal waveform is obtained in all other cases. Eventually, trapezoidal reference signals abbreviated to "tra" for a three-phase MMC topology can be described as

$$E_{o,a} = \mathrm{MI}\frac{V_{DC}}{2}\mathrm{tra}(\omega t + \theta), \tag{17}$$

$$E_{o,b} = \mathrm{MI}\frac{V_{DC}}{2}\mathrm{tra}\left(\omega t + \theta - \frac{2}{3}\pi\right), \tag{18}$$

$$E_{o,c} = \mathrm{MI}\frac{V_{DC}}{2}\mathrm{tra}\left(\omega t + \theta + \frac{2}{3}\pi\right). \tag{19}$$

In addition, in the proposed NLM method, a constant offset term is injected to the reference signal as given in the following:

$$E_o = \mathrm{MI}\frac{V_{DC}}{2}\mathrm{tra}(\omega t + \theta) + k, \tag{20}$$

where k is the corresponding offset value for the reference signal. In order to obtain the optimal value, different values of k-term are tested in terms of output performance of the MMC under the condition that exactly the same model including circuit parameters and capacitor voltage sorting and selection procedure is applied for each k-term. Accordingly, suitable selection of k-term is supposed as nearly $-0.2 \leq k \leq 0.2$. Because, the required SM number received from the NLM process for modulation is held between 0 and N in this range. More precise calculation could be carried out within this range in the modulation process. Also, selection of the suitable SM/SMs is simply done to provide capacitor voltage balancing in a fundamental period in this range. A different capacitor voltage balancing method may be required since the reference values change for the upper and lower arm outside of the defined k-term range. The proposed NLM method operates for both positive and negative k-terms. Normalized output voltage forms of the upper and lower arm are expressed as

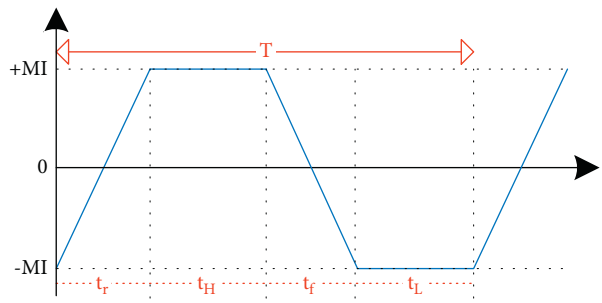


Figure 6: Representation of a trapezoidal signal.

$$E_u^n = \frac{N}{2}\left[1 - \mathrm{MItra}\left(\omega t + \theta\right) + k\right], \tag{21a}$$

$$E_l^n = \frac{N}{2}\left[1 + \mathrm{MItra}\left(\omega t + \theta\right) + k\right]. \tag{21b}$$

The voltage level of instantaneous arm voltage of the upper and lower arm is described at each sampling interval as follows:

$$E_{level\_u}^n = \mathrm{round}\left(E_u^n\right), \tag{22a}$$

$$E_{level\_l}^n = \mathrm{round}\left(E_l^n\right). \tag{22b}$$

Figure 7 depicts the voltage waveforms of the proposed NLM method in a fundamental period for $N = 6$. Upper and lower reference signals are symmetrical to each other. As can be deduced from this principle, output waveform is obtained as $2N + 1$ voltage level.

Both positive and negative k-terms are evaluated for $N = 4$ under various MI values in terms of THD and fundamental voltage magnitude of output as shown in Figure 8 to exhibit the differences of k-terms. A better output performance in terms of THD and DC voltage utilization for output voltage than the C-NLM is obtained in this interval. THD of output voltage is almost symmetrical with respect to the zero value of k-term for positive and negative k-terms as shown in Figure 8(a). In general, negative k-terms provide better performance for different modulation ratios. In addition, Figure 8(b) depicts the DC voltage utilization performance, which is also generally better for negative k-terms. As the k-term moves away from zero, the voltage level increases so that $2N + 1$ voltage level is established around ±0.1. If the k-term is not properly selected, the output voltage quality may not be increased at the desired level. In order to overcome this risk, Figure 8 is provided to determine the k-term under various modulation ratios in terms of THD of output voltage and magnitude of output fundamental voltage. As a result of this analysis, depending on the application area of MMC topology, any k-term could be chosen for the best utilization.

In high-modulation-ratio applications and if the number of SMs in the arms are more than enough (i.e., $N = 10$ or more), the output voltage is generally in the desired form. On the other hand, in low-modulation-ratio applications and when the number of SMs is

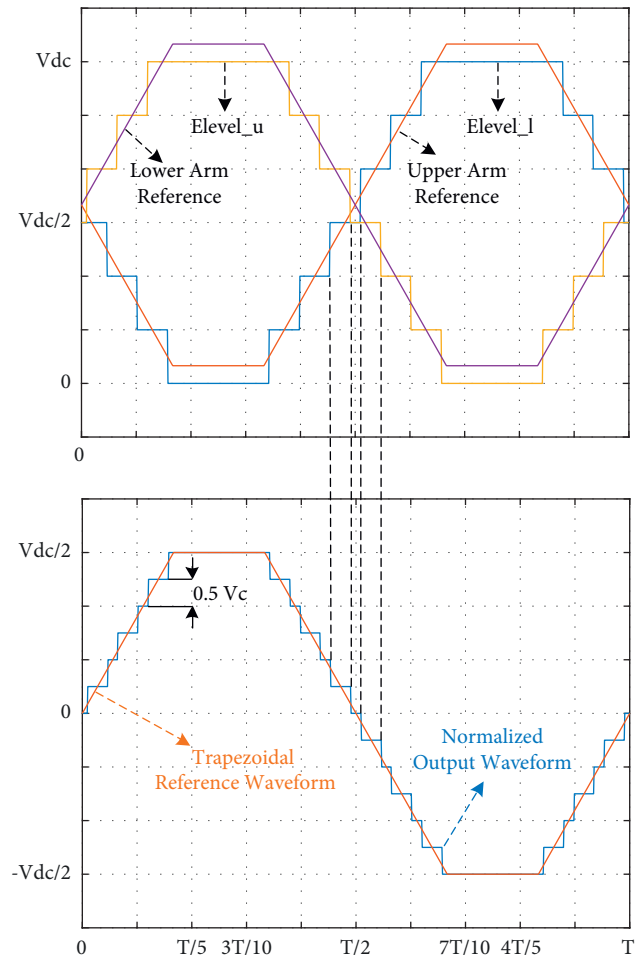


Figure 7: Working principle of the proposed NLM method.

relatively few, C-NLM yields no output voltage owing to the modulation process as mentioned before. As an example, when the number of SMs in each arm is equal to four (i.e., $N = 4$), the result of equations (13a) and (13b) is two and it is continuously same for MI ≤ 0.2 during the operation. This repeated outcome gives no voltage on the output of MMC as can be derived from equation (5). In order to solve this problem, the proposed NLM method enables to obtain an output voltage, thanks to the trapezoidal signal manipulation. In the proposed NLM method, if the output voltage is zero for low modulation indexes, main parts of modulation signal are changed by $t_r = t_f = t_H = t_L = T/4$ from $t_r = t_f = T/3$ and $t_H = t_L = T/6$. Time durations of trapezoidal signal are determined by changing the rise and fall time in low modulation indexes during the operation, which provides nonzero value on the output of MMC. The mentioned time durations are optimally determined using simulation works for the various time parts of the trapezoidal signal. Consequently, when the output voltage is zero during a fundamental period, different modulation processes as stated by the following equations are implemented to obtain the normalized output voltage forms of the upper and lower arm:

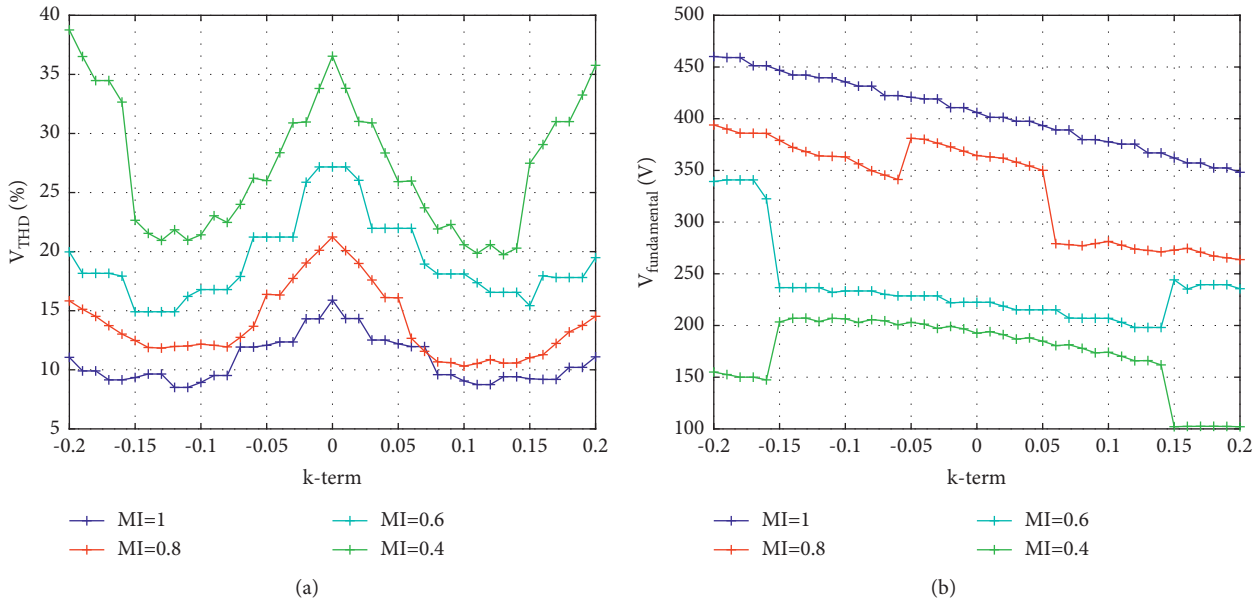


FIGURE 8: Output performance of MMC versus different k-terms under the proposed NLM method: (a) THD of output voltage; (b) magnitude of output fundamental voltage.

$$E_u^{n*} = \frac{N}{2}[1 - \text{MItra}(\omega t + \theta)], \tag{23a}$$

$$E_l^{n*} = \frac{N}{2}[1 + \text{MItra}(\omega t + \theta)]. \tag{23b}$$

Then, the voltage level of instantaneous voltage of arms is expressed as

$$E_{level\_u}^{n*} = \text{round}_{|k|}(E_u^{n*}), \tag{24a}$$

$$E_{level\_l}^{n*} = \text{round}_{|k|}(E_l^{n*}), \tag{24b}$$

where $\text{round}_{|k|}$ is a more precise calculation increased by the absolute value of k-term compared to the conventional rounding function. Resultantly, Figure 9 describes the overall control scheme of the proposed NLM method. The normal process of the proposed NLM method can be operated in all modulation ratios. On the other hand, time durations of trapezoidal reference signal is changed as shown in Figure 9 with more precise calculation when no output voltage is formed during a fundamental period. The general control block diagram representation of the proposed NLM method is presented in Figure 10. Accordingly, first of all, depending on the modulation ratio, trapezoidal signal as a reference waveform is created by determining the main parts of it as given in Figure 9. In order to obtain the nearest voltage level, while directly rounding for equations (21a) and (21b) is used, $\text{round}_{|k|}$ with precise calculation for equations (23a) and (23b) is implemented. Following this step, capacitor voltages of SMs are balanced using the capacitor voltage balancing feedback system as pointed out in the next paragraph.

In order to complete the modulation process, capacitor voltage control is also necessary to balance the capacitor voltages at a nominal value in each SM of the upper and lower arm. For this reason, the capacitor voltage balancing algorithm is applied to the upper and lower arm as shown in Figure 11 and it is based on the principle of measuring and sorting the SM capacitor voltages and selecting the suitable SMs. After measurement of the capacitor voltages and arm currents, depending on the direction of the arm current, capacitor voltages are sorted in the ascending or descending order. Considering the required number of SMs received from the modulation process, convenient capacitors are chosen; then, capacitor voltages are balanced and kept constant.

5. Simulation Study

In order to confirm the effectiveness of the proposed NLM method, a simulation study is carried out in this section. C-NLM, third-harmonic injected NLM method, and the proposed NLM method are compared in terms of the output voltage performance of MMC including number of voltage levels, THD and DC voltage utilization, and low modulation ratio performance under various case studies. THD is calculated until 50th harmonic component in all results. Circuit parameters of the designed single-phase MMC model are given in Table 2.

5.1. Case Study 1: Verification of the Amount of Voltage Level Increment. In this case study, the amount of voltage level increment from $N+1$ to $2N+1$ without using any additional SMs is shown by comparing the proposed NLM method with the C-NLM method. Upper and lower arm voltages are illustrated in Figure 12(a), while the output voltage and current waveform are presented in Figure 12(b) when MI = 1 using the C-NLM method, which is obtained as $N+1$ levels (7 levels). Under the completely same conditions and when

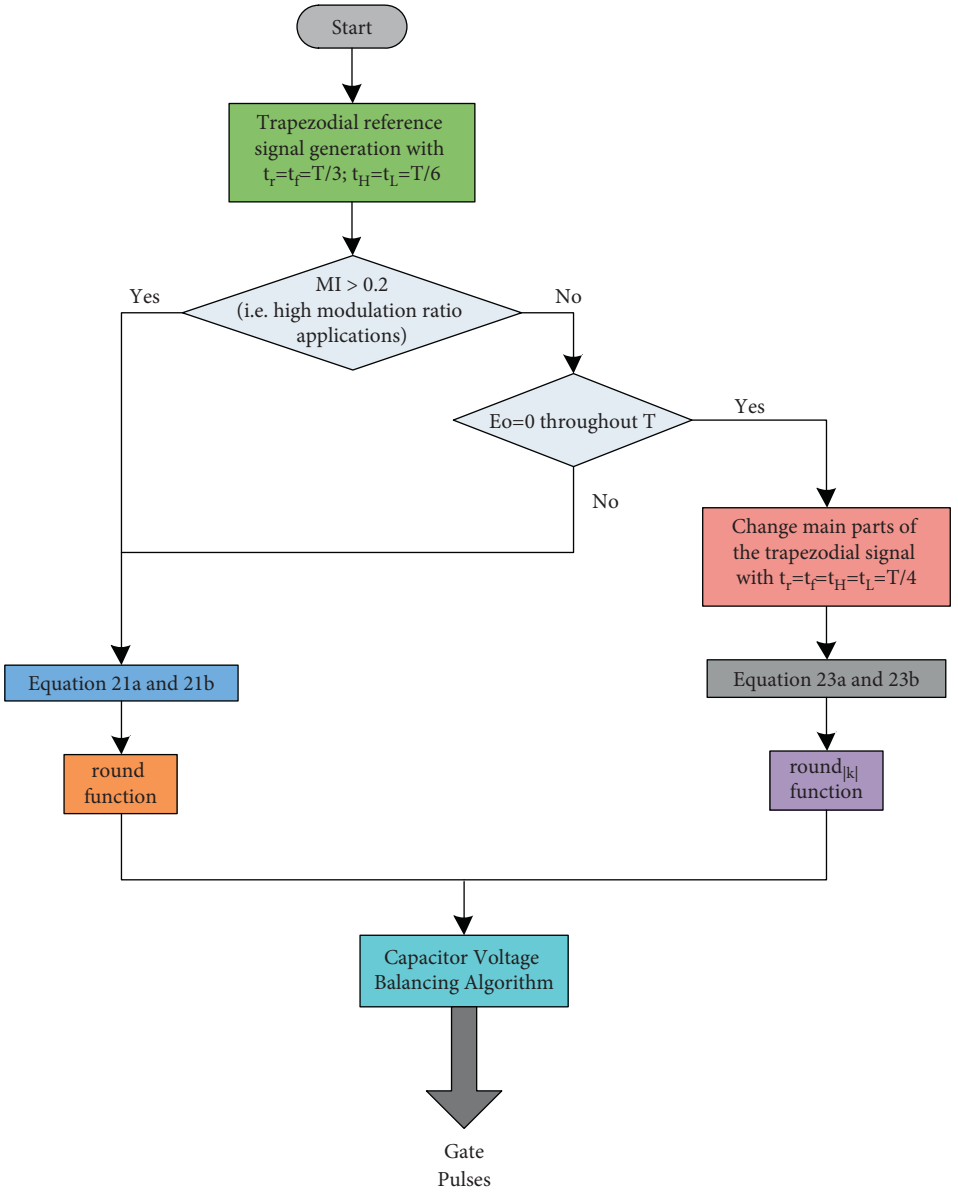


Figure 9: Overall control procedure of the proposed NLM method.

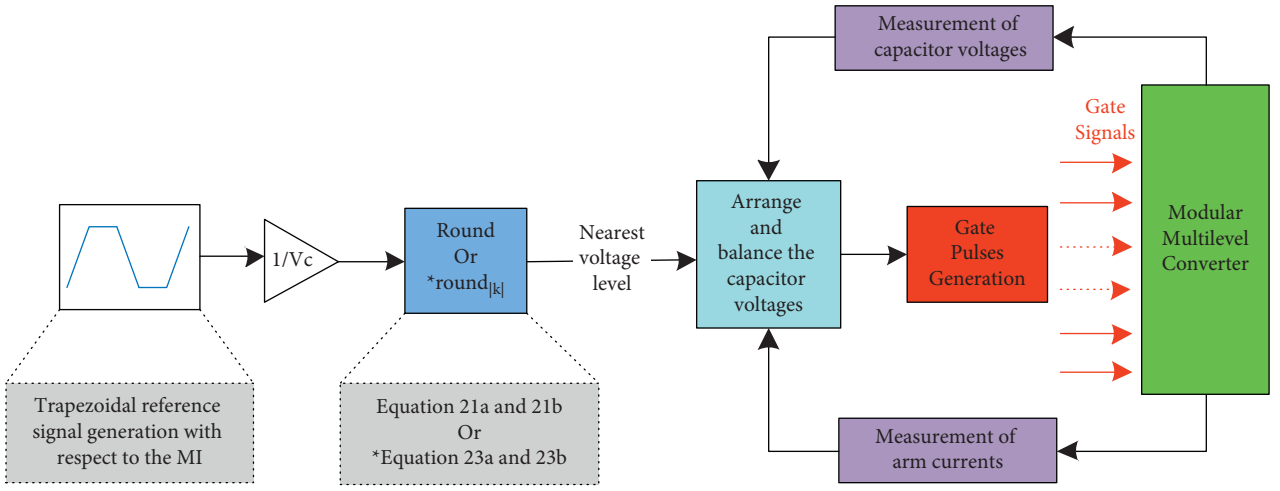


Figure 10: General control block diagram of the proposed NLM method.

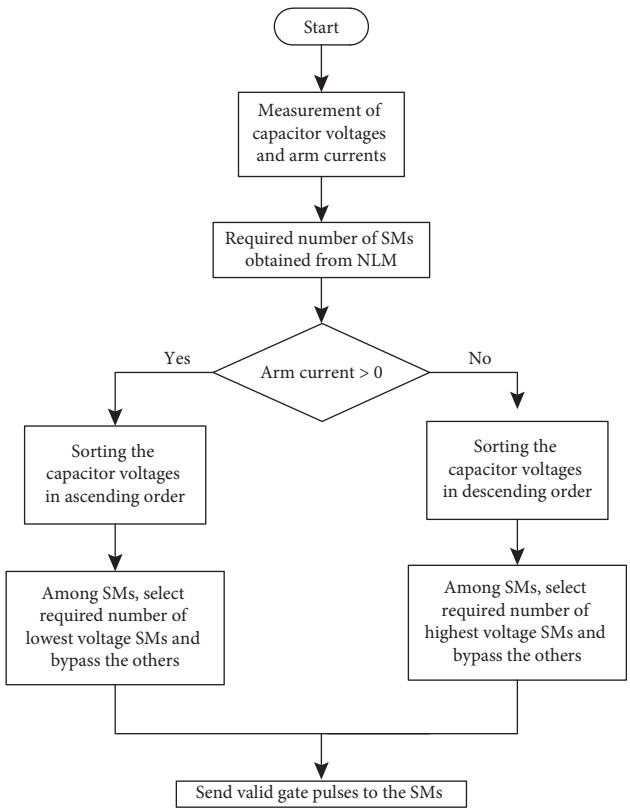


Figure 11: Capacitor voltage balancing algorithm.

Table 2: Main circuit parameters of the simulated MMC model.

Parameter	Value
DC-link voltage	1.29 kV
Output frequency	50 Hz
Number of SMs	6
Arm inductance	20 mH
SM capacitance	1 mF
Sampling frequency	4 kHz
Load resistance	20 Ω
Load inductance	100 mH

k-term = -0.11, the number of the voltage levels is increased to 2N + 1 levels (13 levels) through the proposed NLM method. Figures 13(a) and 13(b) depict the upper and lower arm voltage with the obtained output voltage and current waveform. Moreover, balanced capacitor voltages of the upper and lower arm in the proposed NLM method are given in Figures 14(a) and 14(b), respectively. Average values of them are around 230 V. As a result, this case study shows the satisfactory performance of the proposed NLM method by presenting the voltage level increment without using any extra SMs.

5.2. Case Study 2: Comparison in terms of the THD and DC Voltage Utilization. To show the better performance of the proposed NLM method than C-NLM and third-harmonic injected NLM method, these methods are compared in terms of the THD and DC voltage utilization in this case. In Figure 15, THD performances of these methods are presented for output voltage and current under variation of the modulation index. In this regard, according to Figure 15, both voltage and current THD values are significantly mitigated in all modulation ranges. The THD value of the output voltage is mitigated from 11.35% to 7.78%, thanks to the proposed NLM method for MI = 1. Furthermore, magnitudes of output voltages are compared and exhibited in Figure 16 under different modulation ratios. For almost all modulation index values, DC voltage utilization of the proposed NLM method is better than of the C-NLM and third-harmonic injected NLM method, which causes the increased output voltage and current. The magnitude of the fundamental voltage of the output voltage is boosted from 640.9 V to 713.3 V with the aid of the proposed NLM method for MI = 1. Herewith, according to the comparison results, the acceptability of the proposed NLM method is evident by the reduced voltage and current THD and increased voltage and current magnitude.

5.3. Case Study 3: Verification of Superior Performance under Low Modulation Ratios. A case study is presented to show the feasibility of the proposed NLM method in low-modulation-ratio applications and for MMC with a low number of SMs in this section. When the number of SMs in each arm is equal to four (i.e., $N = 4$), no output voltage is obtained in C-NLM since equations (13a) and (13b) return the value of two and it is continuously same for MI ≤ 0.2 during the operation. It is resulted that no voltage occurs at the output of MMC as can be extracted from equation (5). In order to overcome this problem, the proposed NLM method provides an AC output voltage owing to changing the main parts of trapezoidal signal. In this context, Figure 17 represents the obtained constant rounding values for the upper and lower arm in C-NLM when $N = 4$ and MI = 0.2. $N_{ON,pj}$ and $N_{ON,nj}$ are equal to two during the whole simulation. Therefore, output voltage returns the value of zero as illustrated in Figure 18, which is previously determined in theory. On the other hand, under the completely same conditions and when k-term = 0.11, the calculated rounding values for the upper and lower arm in the proposed NLM method are shown in Figure 19. $N_{ON,pj}$ and $N_{ON,nj}$ are variable during the simulation. The output voltage and current waveform are obtained and presented in Figure 20, thanks to the variation of the rounding values for the upper and lower arm. The same results could be deduced for $N = 4$ and MI = 0.1. Obviously, superiority of the proposed NLM method over C-NLM is proved for low-modulation-ratio applications in this case study.

6. Experimental Study

In order to validate the superior performance of the proposed NLM method, a laboratory prototype of a single-phase MMC circuit consisting of four SMs per arm is designed and established as seen in Figure 21. Aforementioned simulation case studies are experimentally confirmed in this section. Table 3 gives the circuit parameters used for the experiment.

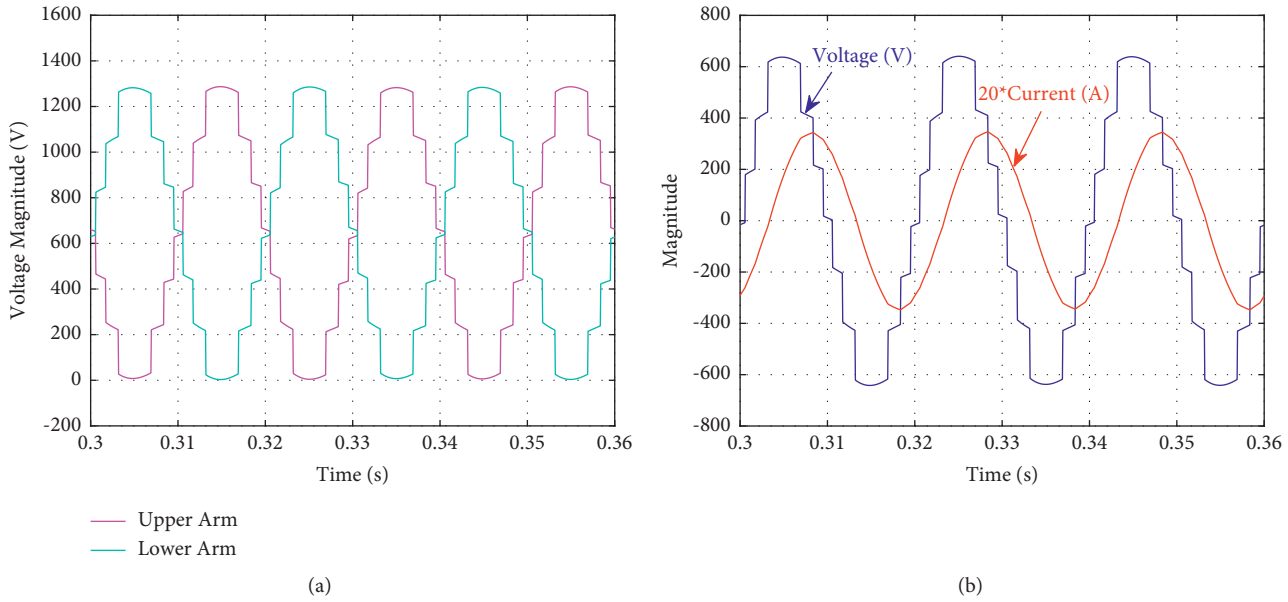


FIGURE 12: Voltage waveforms of the simulated MMC model using the C-NLM method: (a) upper and lower arm voltage; (b) output voltage and current.

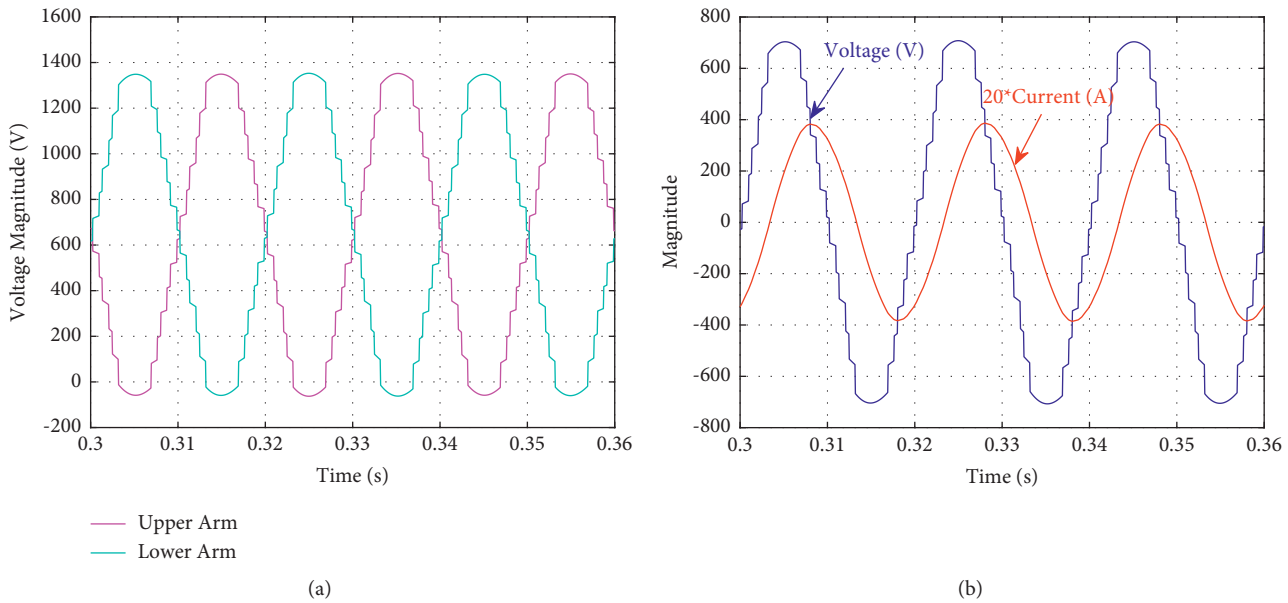


FIGURE 13: Voltage waveforms of the simulated MMC model using the proposed NLM method; (a) upper and lower arm voltage; (b) output voltage and current.

In the experimental setup, the main DC source is utilized at the DC side to supply the MMC topology and the power unit feeds the experiment boards. Atmel ARM Cortex-M3-based microcontroller board [52] and Xilinx SPARTAN-6 FPGA digital circuit development platform at the clock frequency of 100 MHz [53] are used to control the MMC system. ISE design suite software is used to supervise and control the experiment in real time. MMC SMs consist of isolated gate drivers, MOSFET semiconductors, and capacitor cards with current protection. The voltage and current sensors employed in the measurement cards sense the capacitor voltage and arm currents and send them to the microcontroller analog ports. The microcontroller is responsible for receiving the voltage and current sensor data and processing these data for C-NLM and proposed NLM method including capacitor voltage balancing algorithm. Then, it transfers the required information for the switching of semiconductor devices via communication interface with serial line to the FPGA board. Meanwhile, the FPGA platform simultaneously generates the switching pulses for the MMC SMs. It should be noted that the microcontroller completes the required calculations given in Figures 10 and

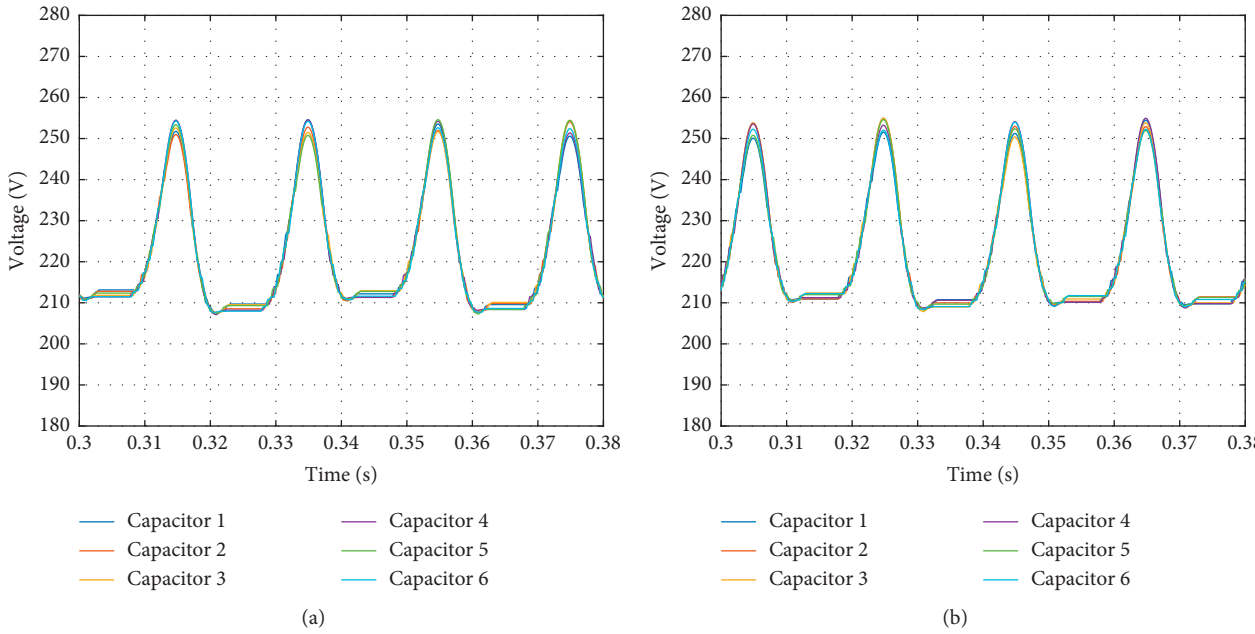


Figure 14: Capacitor voltages: (a) upper arm capacitors; (b) lower arm capacitors.

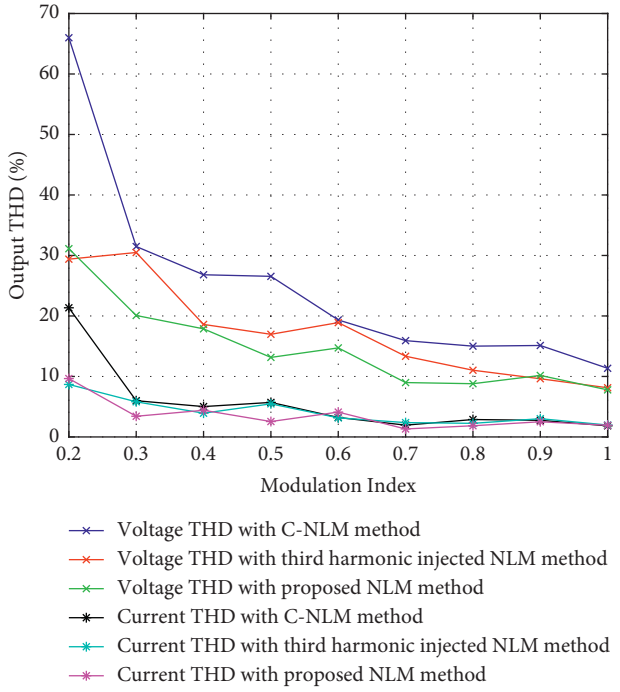


Figure 15: Graphical comparison of the output voltage and current THD values under different modulation ratios.

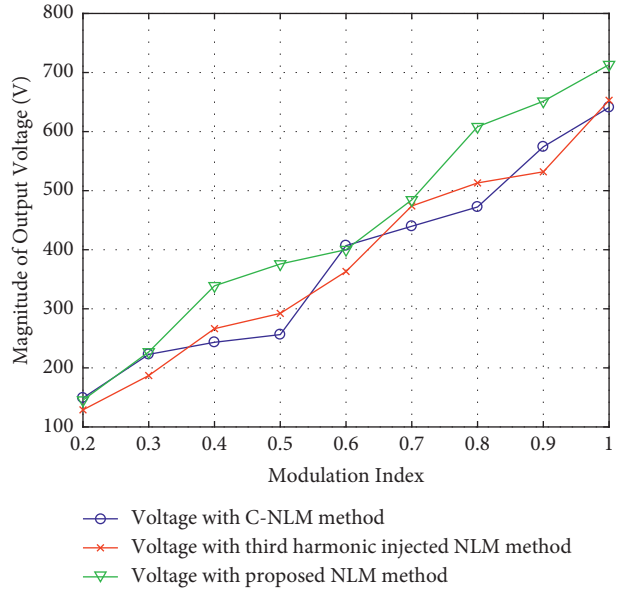


Figure 16: Magnitudes of the output voltage values under different modulation ratios.

11 and sends necessary information to the FPGA in each sampling cycle which is 5 kHz (0.2 ms). The output voltage and current waveform are monitored by a Tektronix TPS2024 digital oscilloscope and stored to a host PC via the computer program of the oscilloscope. The voltage and current are measured by differential probes and current probes, respectively. Resistive and inductive loads whose values are specified in Table 3 are employed at the output of the MMC topology for all cases. In addition, a dead time of 200 ns is used for switching of MOSFETs. The THD of output waveforms is computed until the 50th harmonic component as done in the simulation.

First of all, the amount of voltage level increment is experimentally shown by comparing the proposed NLM method with the C-NLM method. Upper (channel (3)) and lower (channel (4)) arm voltages are illustrated in Figure 22(a), while the output voltage (channel (1)) and current (channel (2)) waveform are presented in Figure 22(b) when MI = 1 using the C-NLM method, which is obtained as $N+1$ levels (5 levels). Under the completely same conditions and when k-term = -0.11, the number of the

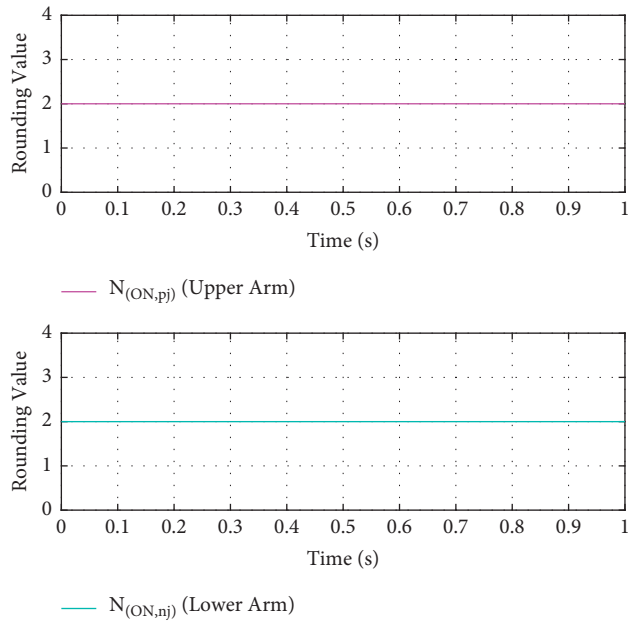


Figure 17: Obtained rounding values for the upper and lower arm in C-NLM when MI = 0.2.

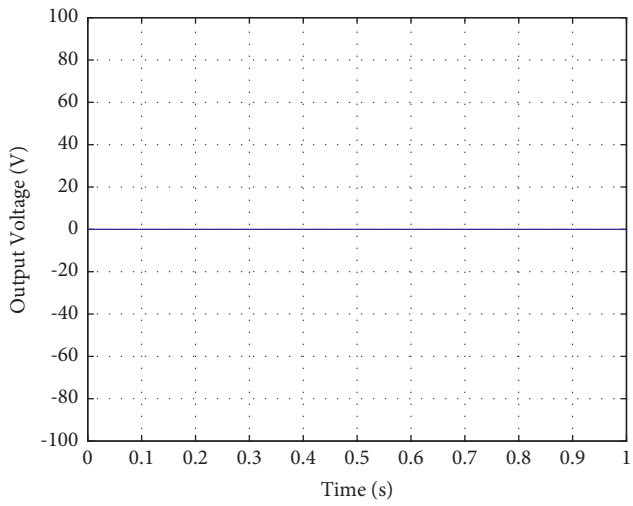


Figure 18: Output voltage in C-NLM when MI = 0.2.

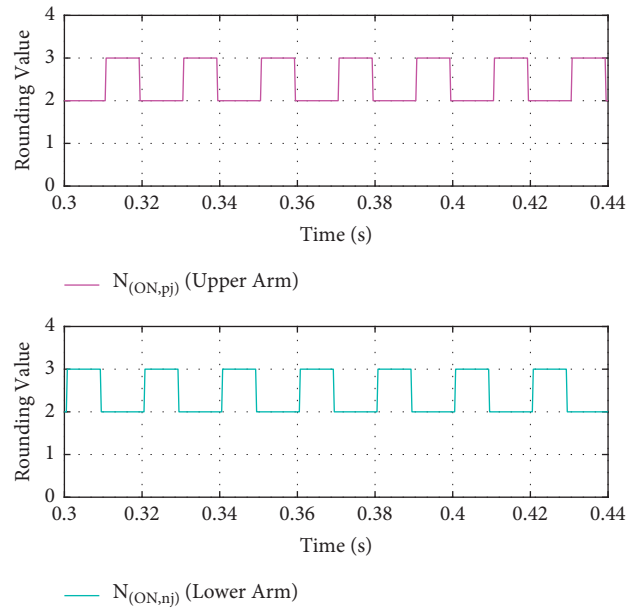


Figure 19: Calculated rounding values for the upper and lower arm in the proposed NLM method when MI = 0.2.

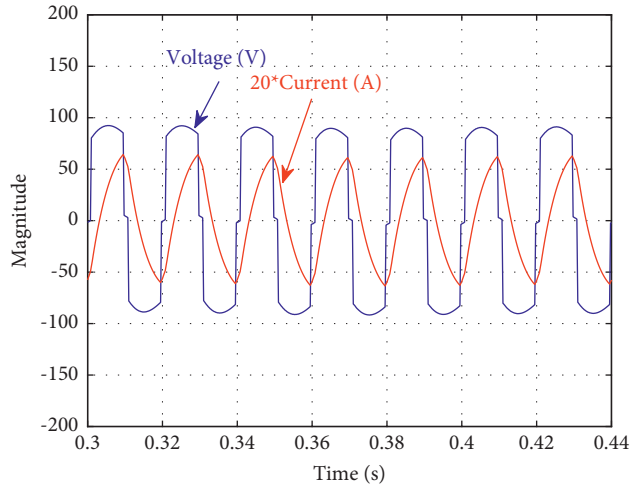


Figure 20: Output voltage and current waveform in the proposed NLM method when MI = 0.2.

voltage levels is increased to 2N + 1 levels (9 levels) using the proposed NLM method. Figures 23(a) and 23(b) indicate the upper (channel (3)) and lower (channel (4)) arm voltage with the obtained output voltage (channel (1)) and current (channel (2)) waveform. Also, balanced capacitor voltages of the upper and lower arm in the proposed NLM method are visualized in Figures 24(a) and 24(b), respectively. In both figures, capacitor voltages are monitored by different and the same horizontal positions. In the screenshot, all four channels from 1 to 4 correspond to the capacitors from 1 to 4, respectively, for the upper and lower arm. Average values of them are around 10.8 V.

Secondly, good performance of the proposed NLM method in terms of the THD and DC voltage utilization is supported here by the experimental results. In Figure 25, THD results are compared for the output voltage and current under different modulation ratios. In this context, according to Figure 25, both voltage and current THD values are significantly reduced in all modulation ranges. The THD value of the output voltage is reduced from 15.65% to 9.05% through the proposed NLM method for MI = 1. Moreover, magnitudes of output voltages are presented in Figure 26 under variable modulation ratios. The magnitude of the fundamental voltage of the output voltage is increased from 15.06 V to 16.77 V, thanks to the proposed NLM method for MI = 1.

Finally, the suitability of the proposed NLM method in low-modulation-ratio applications is presented. With the C-NLM, Figure 27 represents the output voltage, which returns the value of zero. In addition, when k-term = 0.11,

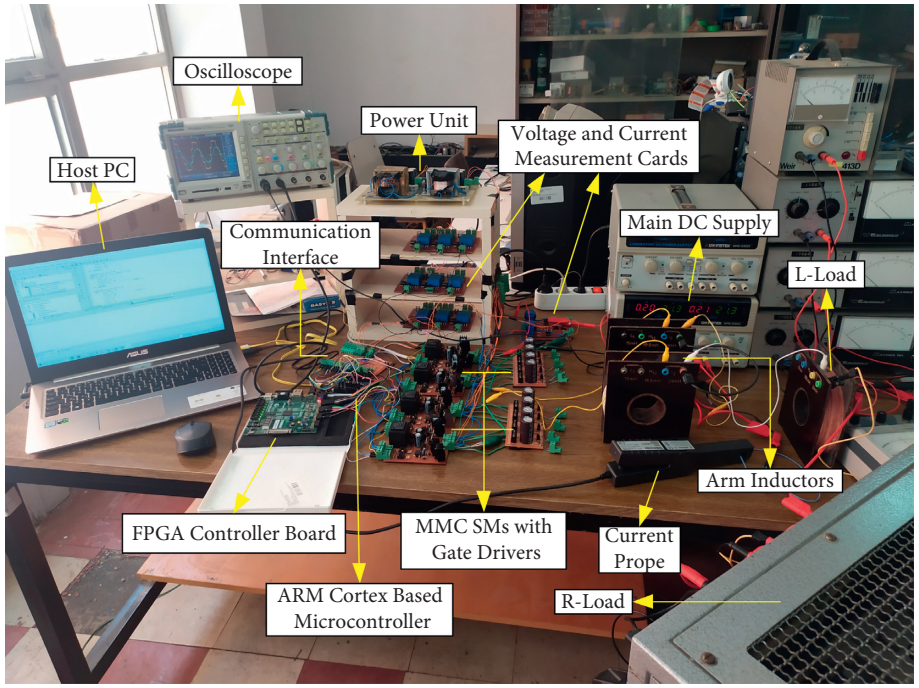
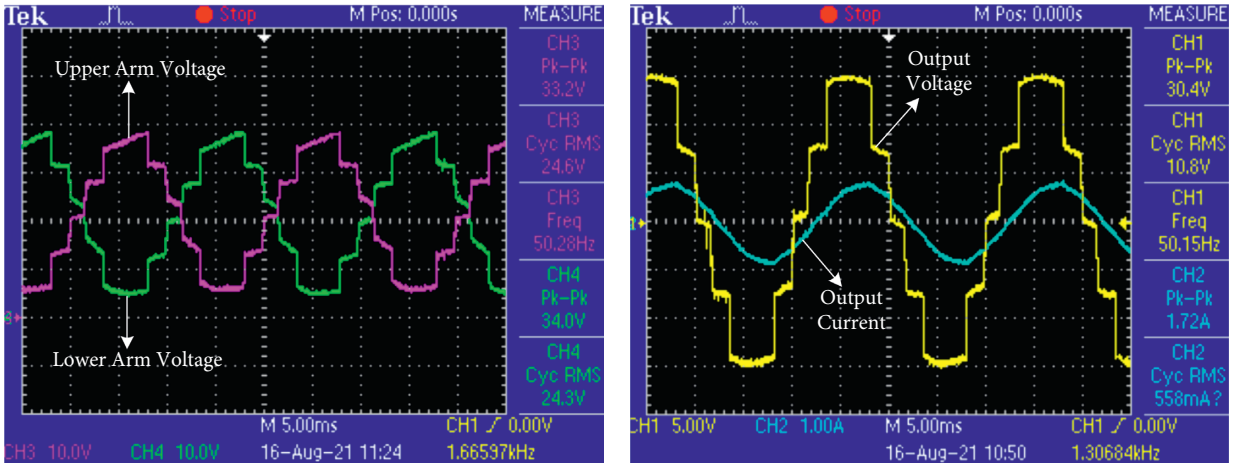


Figure 21: Experimental prototype of the MMC topology.

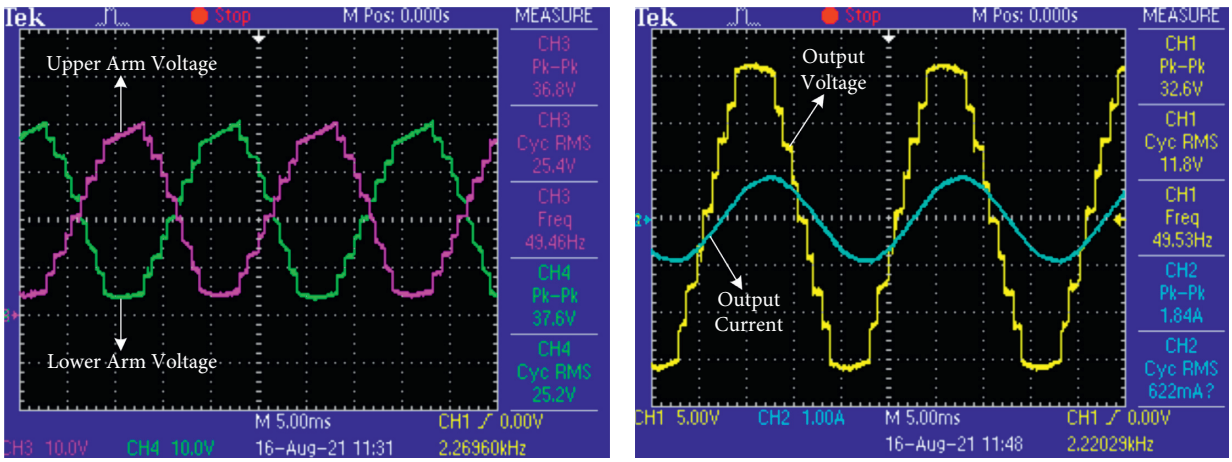
Table 3: Experimental circuit parameters of the MMC system.

Parameter	Value
DC-link voltage	40 V
Output frequency	50 Hz
Number of SMs	4
Arm inductance	29 mH
SM capacitance	4.7 mF
Sampling frequency	5 kHz
Voltage sensor, LEM LV 25-P	Up to 500 V
Current sensor, LEM LA 55-P	Up to 50 A
Load resistance	10 Ω
Load inductance	29 mH



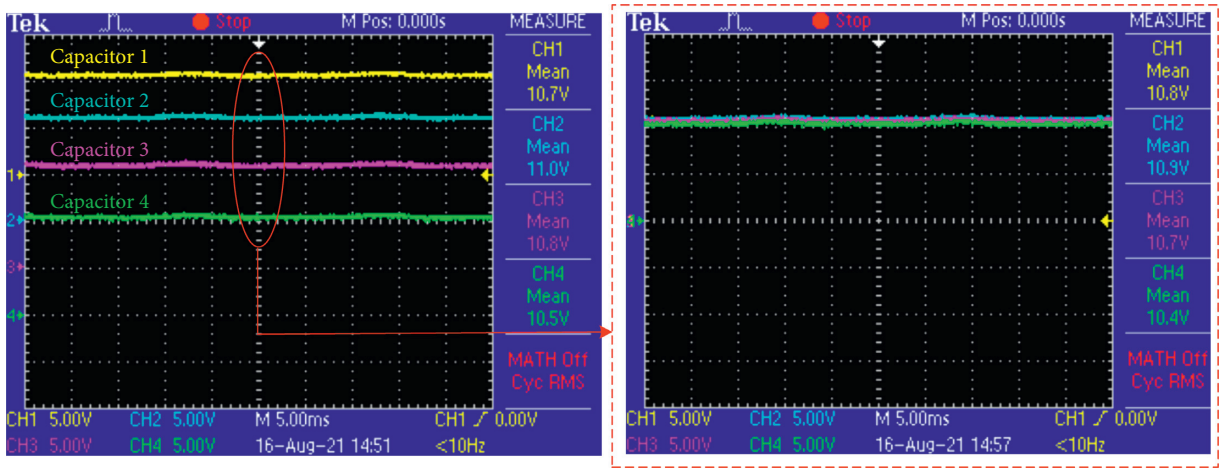
(a) (b)

Figure 22: Experimental waveforms of the MMC topology using the C-NLM method: (a) upper and lower arm voltage; (b) output voltage and current.

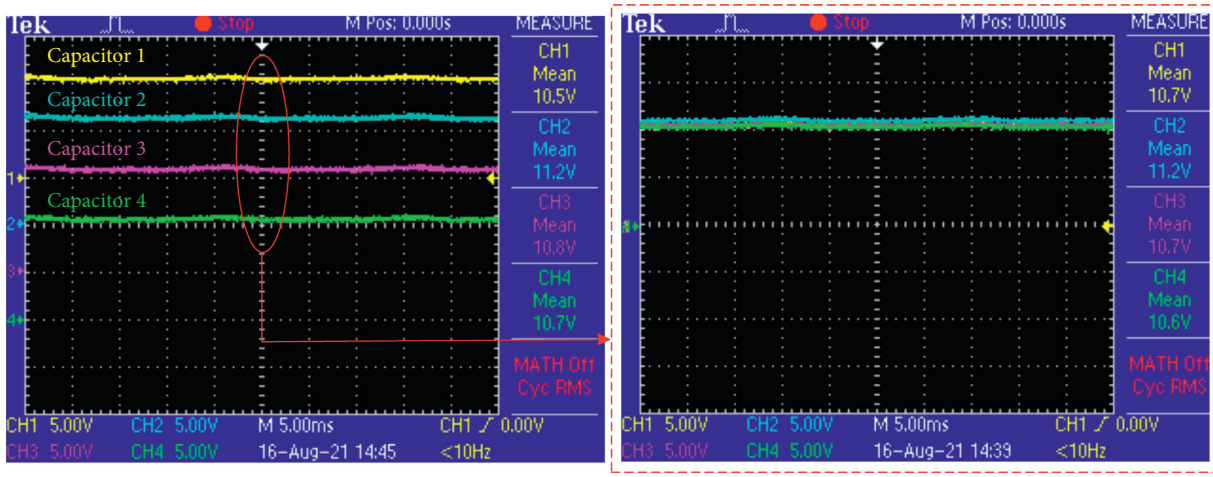


(a) (b)

Figure 23: Experimental waveforms of the MMC topology using the proposed NLM method: (a) upper and lower arm voltage; (b) output voltage and current.



(a)



(b)

Figure 24: Balanced capacitor voltages in the experiment: (a) upper arm capacitors; (b) lower arm capacitors.

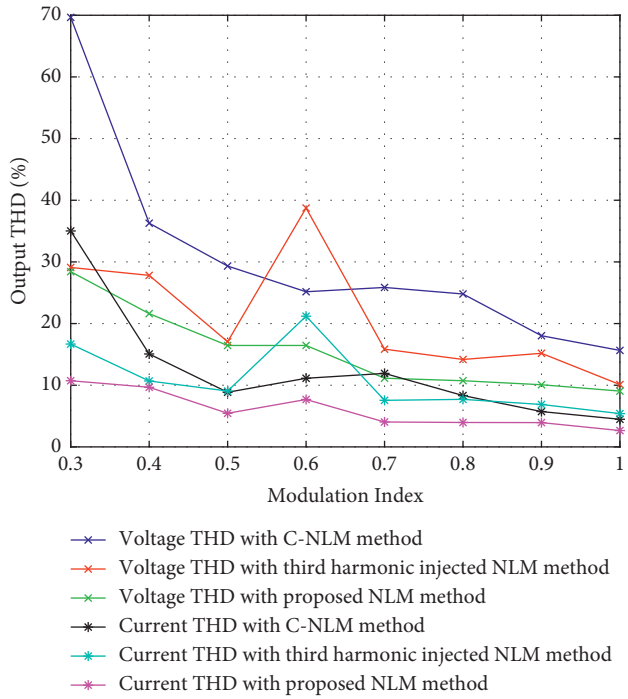


Figure 25: Experimental comparison of the output voltage and current THD values under different modulation ratios.

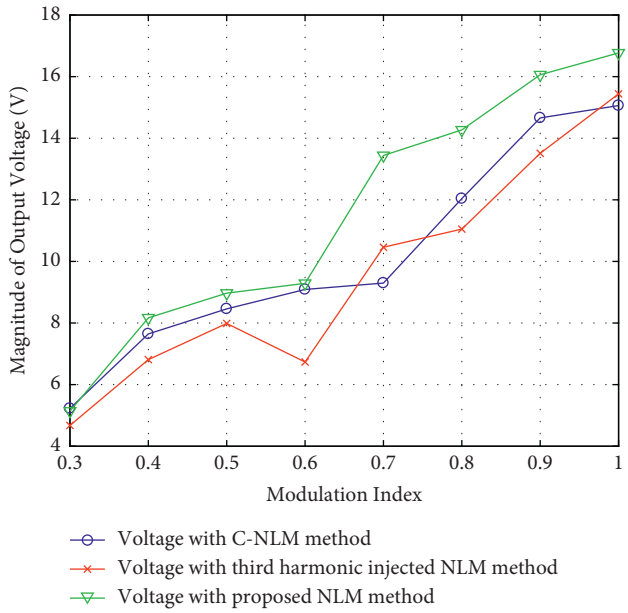


Figure 26: Magnitudes of the output voltage values under different modulation ratios in the experiment.

output voltage (channel (1)) and current (channel (2)) waveform are obtained and shown in Figure 28, thanks to the variation of the rounding values for the upper and lower arm in the proposed NLM method.

Ultimately, all simulation cases are supported and validated by the experimental results and applicability of the proposed NLM method is comprehensively demonstrated in this section.

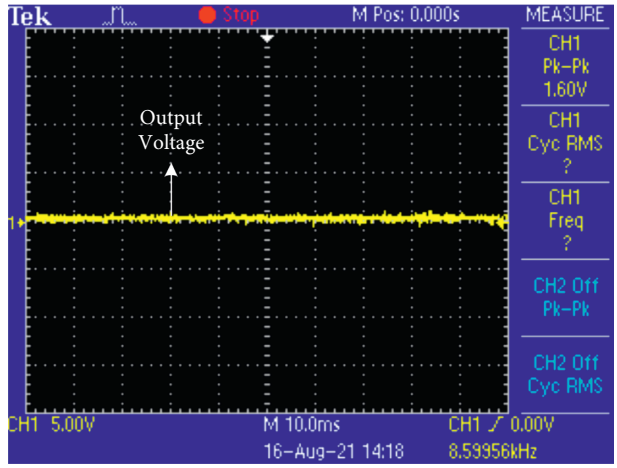


Figure 27: Output voltage in C-NLM when MI = 0.2 in the experiment.

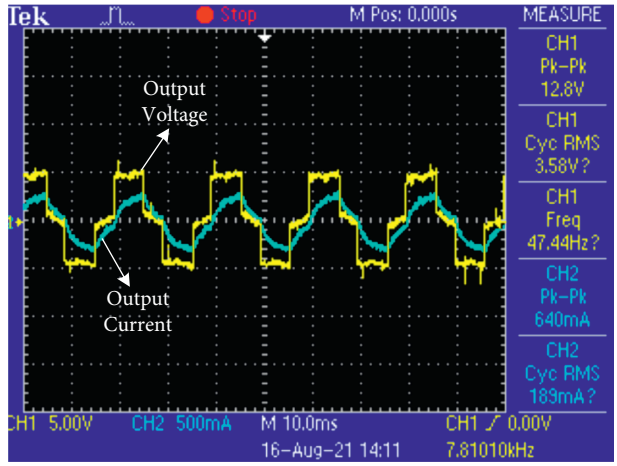


Figure 28: Experimental waveform of the output voltage and current in the proposed NLM method when MI = 0.2.

7. Conclusion

A novel NLM method has been developed with increased output voltage quality for MMC topology in this paper. The output voltage has been boosted to 2N + 1 levels by the proposed NLM method without using any additional SMs. The proposed NLM method has been implemented to the upper and lower arms of the MMC; then, arm voltages have been controlled. In addition, satisfactory results have been obtained for low-modulation-ratio applications in relatively small amount of SM usage of MMC design. In order to present the good performance of the proposed NLM method, a comparison has been made with the C-NLM and third-harmonic injected NLM method in terms of THD and magnitude of the output voltage and current. The THD value of the output voltage has been mitigated from 11.35% to 7.78% and 15.65% to 9.05%, in the simulation and experiment, respectively. The magnitude of the fundamental voltage of the output voltage has been increased from 640.9 V to 713.3 V and 15.06 V to 16.77 V in the simulation and experiment, respectively. In addition, capacitor voltage

balancing for the proposed NLM method has been achieved to keep the capacitor voltage of each SM of MMC constant. To show the appropriateness of the proposed NLM method, simulation case studies have been verified by the experimental results using FPGA-based hardware implementation on the laboratory prototype. As a future work, the proposed NLM method could be implemented for MMC-based industrial applications.

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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