Hindawi
International Transactions on Electrical Energy Systems
Volume 2023, Article ID 9863826, 1 page
https://doi.org/10.1155/2023/9863826

Retraction

Retracted: Application of Laser Scanning Technology in Digital Method

International Transactions on Electrical Energy Systems

Received 19 September 2023; Accepted 19 September 2023; Published 20 September 2023

This article has been retracted by Hindawi following an investigation undertaken by the publisher [1]. This investigation has uncovered evidence of one or more of the following indicators of systematic manipulation of the publication process:

(1) Discrepancies in scope
(2) Discrepancies in the description of the research reported
(3) Discrepancies between the availability of data and the research described
(4) Inappropriate citations
(5) Incoherent, meaningless and/or irrelevant content included in the article
(6) Peer-review manipulation

The presence of these indicators undermines our confidence in the integrity of the article's content and we cannot, therefore, vouch for its reliability. Please note that this notice is intended solely to alert readers that the content of this article is unreliable. We have not investigated whether authors were aware of or involved in the systematic manipulation of the publication process.

Wiley and Hindawi regrets that the usual quality checks did not identify these issues before publication and have since put additional measures in place to safeguard research integrity.

We wish to credit our own Research Integrity and Research Publishing teams and anonymous and named external researchers and research integrity experts for contributing to this investigation.

The corresponding author, as the representative of all authors, has been given the opportunity to register their agreement or disagreement to this retraction. We have kept a record of any response received.

References

[1] F. Liu, "Application of Laser Scanning Technology in Digital Method," *International Transactions on Electrical Energy Systems*, vol. 2022, Article ID 2629688, 11 pages, 2022.

Hindawi
International Transactions on Electrical Energy Systems
Volume 2022, Article ID 2629688, 11 pages
https://doi.org/10.1155/2022/2629688

Research Article

Application of Laser Scanning Technology in Digital Method

Fangfang Liu

Zhoukou Vocational and Technical College, Henan, Zhoukou 466000, China

Correspondence should be addressed to Fangfang Liu; 1520110207@st.usst.edu.cn

Received 14 July 2022; Revised 31 July 2022; Accepted 8 August 2022; Published 16 September 2022

Academic Editor: Nagamalai Vasimalai

In order to improve the efficiency and accuracy of retrieval and mining of highway operation management information, a digital method research and application method based on laser scanning technology is proposed. Combined with the data storage and backup requirements of highway toll collection system, such as large amount of information, high reliability, easy management, and easy management, a complete design scheme of optical storage backup chip based on programmable logic array FPAG technology is proposed. The function, design, and simulation implementation of the write strategy subsystem and the laser power automatic control subsystem of the optical storage backup chip system are emphatically introduced. Through a lot of simulation tests, the scheme is reasonable and feasible, and its performance is stable and reliable.

1. Introduction

With the continuous improvement and operation of expressways, how to manage and use them well and give full play to their role as modern transportation infrastructure has become the most urgent issue. The collection of highway tolls is one of the essential tasks of highway operation and management. The construction and operation of the highway toll system directly affect the quality and economic efficiency of road operation and management in Chuan [1, 2].

The construction of toll roads in China began in Taiwan Province in the 1970s. The North-South Taiwan Expressway, opened to traffic in October 1978, was 373 km long and used toll reimbursement, becoming the first tolled expressway. On the mainland, since October 1988 Shanghai-Jia Expressway toll, there have been Guangfo Expressway, Shen Da Expressway, West Lin Expressway, Beijing-Tianjin-Tang Expressway, and other successive opening and implementation tolls. In addition to a few provinces such as Tibet, most areas have a varying number of toll expressways. Guangdong, Liaoning, Hubei, Shandong, and other regions have more toll roads. Because of the highway construction task and the shortage of funds, contradiction is more prominent, so constructing a toll collection system on the highway, charging vehicle tolls will become the central theme of China's highway development in the future.

The highway toll system is an information data system, and the information of the highway includes three parts: highway personnel information [3, 4], highway activity information, and highway data information. Freeway personnel information includes toll collectors, toll management personnel, maintenance personnel, drivers and passengers, and service organization personnel. Freeway activity information includes information about the tolling process, operations related to the tolling process, and data information processing supporting business activities, such as toll monitoring and toll plaza control. Highway data information includes data generated during the tolling process, such as toll data, traffic volume data, and video information, and data issued by the toll center, including toll rates and base clocks.

Although the data is stored in hard disk memory within the specified time, the hard disk memory cannot be recovered for the data damage caused by many reasons. Therefore, while storing data in real-time, data backup storage should also be performed regularly to ensure that when data is damaged, data can be recovered quickly and correctly and that backup data is easy to keep, reliable, and economical. For the traffic information storage volume,

high information accuracy requirements, storage reliability, financial requirements, and other characteristics, we study what kind of storage backup technology to become one of the keys to the design of highway toll system.

2. Optical Storage Backup Related Technologies

2.1. Data Conversion Process of DVD. First, the data coming from the host is called master data or user data, and the master data consists of 2048 raw data bytes. At the beginning of the master data, 4 bytes of identification code ID are added to identify the sector format, track mode, reflection rate, area where the sector is located, data type, number of layers, number of sectors, etc., 2 bytes are used for ID error detection IED, and 6 bytes of RSV code, and 4 bytes of error detection code EDC are added at the end. The 2064 bytes of data are arranged in a structure of 12 rows and 172 columns, which is called a data frame or data sector.

The 2048 bytes of master data in the data frame are scrambled and encoded to obtain the scrambled data frame. Sixteen consecutive scrambled data frames are combined together to form a data block of 192 (rows) x 172 (columns), and then, the data block is encoded with Reid Solomon error correction; that is, a 16-byte external parity Reid Solomon check code, referred to as P0, is calculated for each column of the 172 columns of the data block, and 16 new P0 rows are formed at the bottom of the ECC block. A complete ECC block can be guaranteed to correct at least 5 bytes of error on each row and 5 bytes of error on each column [5].

The ECC block is crossed in rows, and one P0 row is inserted in order every 12 rows of data, and each of the 16 P0 rows is inserted into the data rows to form a new data structure-record frame. That is, each record frame has 13 rows (including 12 rows of data and 1 row of P0) and 182 columns, and one ECC block will generate 16 record frames. This way of interpolating P0 rows to each sector facilitates the further play of error correction features.

In the process of data encoding and modulation of DVD disc data storage backup system, two techniques are applied to determine the basic form of DVD disc storage backup data, which are 8–14 enhanced modulation EFM + technique and NRZI transform technique.

2.2. EMF + Modulation. EFM+ is the abbreviation for 8–14 enhanced modulation. Optical disk storage system: the purpose of using EMF + modulation is to make the data to be stored into a physical expression suitable for storage on the media; that is, a byte of 8-bit data into 14bti channel code, the transformation from 214 types of code type selected 28 types of code type, and the selected code type should meet: in the channel code between the adjacent two, 1 must have at least 2 more than 10 below the 0. At the same time, in order to extract the synchronization signal in the readout signal, the synchronization signal in EFM + adopts 14T-14 T code type. Thus, EFM + follows the 3T~11 T, 14T rule; that is, there are 10 possible choices of 3T~11 T and 14T for the width of the notch/platform.

The reason why EFM + modulation is used is that when multiple "1s" and "0s" appear in succession when writing data, the laser beam emission will be turned on and off so frequently that the length of the pits becomes very short, which will make the manufacturing process of the optical discs complicated or even difficult. This will make the optical disc manufacturing process complicated or even difficult to achieve. When reading data, because the resolution of the channel code pit/platform is limited by the wavelength of the reading laser and the NA of the focusing lens, if the length of the pit/platform is too short, their edge detection will be difficult; a very short pit will produce unstable data for signal identification; frequent "1" will cause the servo circuit to work unstably, and frequent "0" will cause the laser beam to turn on and off. Frequent "0" will cause the voltage controlled oscillator of the decoding circuit to work unstably because there is no "1" for a longer period of time, and at the same time, long distance pits or planes will also affect the tracking ability of the reading device.

2.3. NRZI Transformation. NRZI transformation is also used before data is stored and backed up to the disc, so that the data to be stored and backed up only jumps when data "1" appears, while the previous state is maintained when data "0" is present. In this way, the data to be stored for backup corresponds to the pit and platform of the VDD, and the transformation from pit to platform or from platform to pit on the DVD disc represents binary data "1," while no transformation represents binary data "0." Figure 1 shows the NRZI conversion timing diagram.

2.4. Overall Solution for Optical Storage Backup Chip Design. The optical disk storage and backup chip is the main component of the optical disk storage and backup system, and its structure is shown in Figure 2.

The functions of each subsystem are described as follows:

(1) The function of the optimal power control subsystem is to determine the optimal power value for reading and burning discs at all levels by conducting a test burn in the disc test burn area.

(2) The automatic laser power control subsystem monitors the power level by closed-loop control to stabilize the power level at its optimal value when reading or burning discs.

(3) The function of the write strategy subsystem is to generate switching control signals for each power level according to the type of disc and the burning speed.

(4) The function of the encoding and modulation subsystem is to convert the user data in the host into the NRZI data to be recorded after a series of encoding and modulation. Coding and modulation are mainly used for error correction and data recovery.

(5) The function of the phase-locked loop subsystem is to provide a stable and unified clock mnemonic for the reading and burning of the disc.

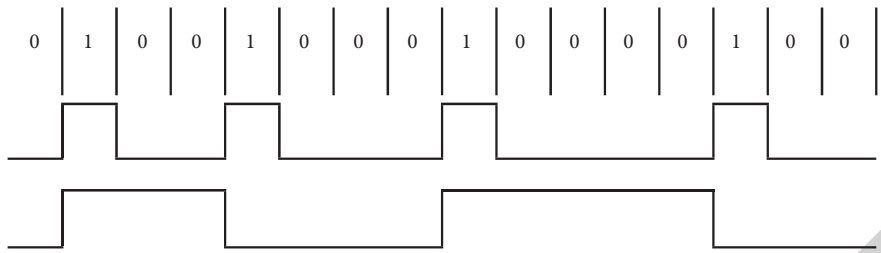

Figure 1: NRZI conversion timing diagram.

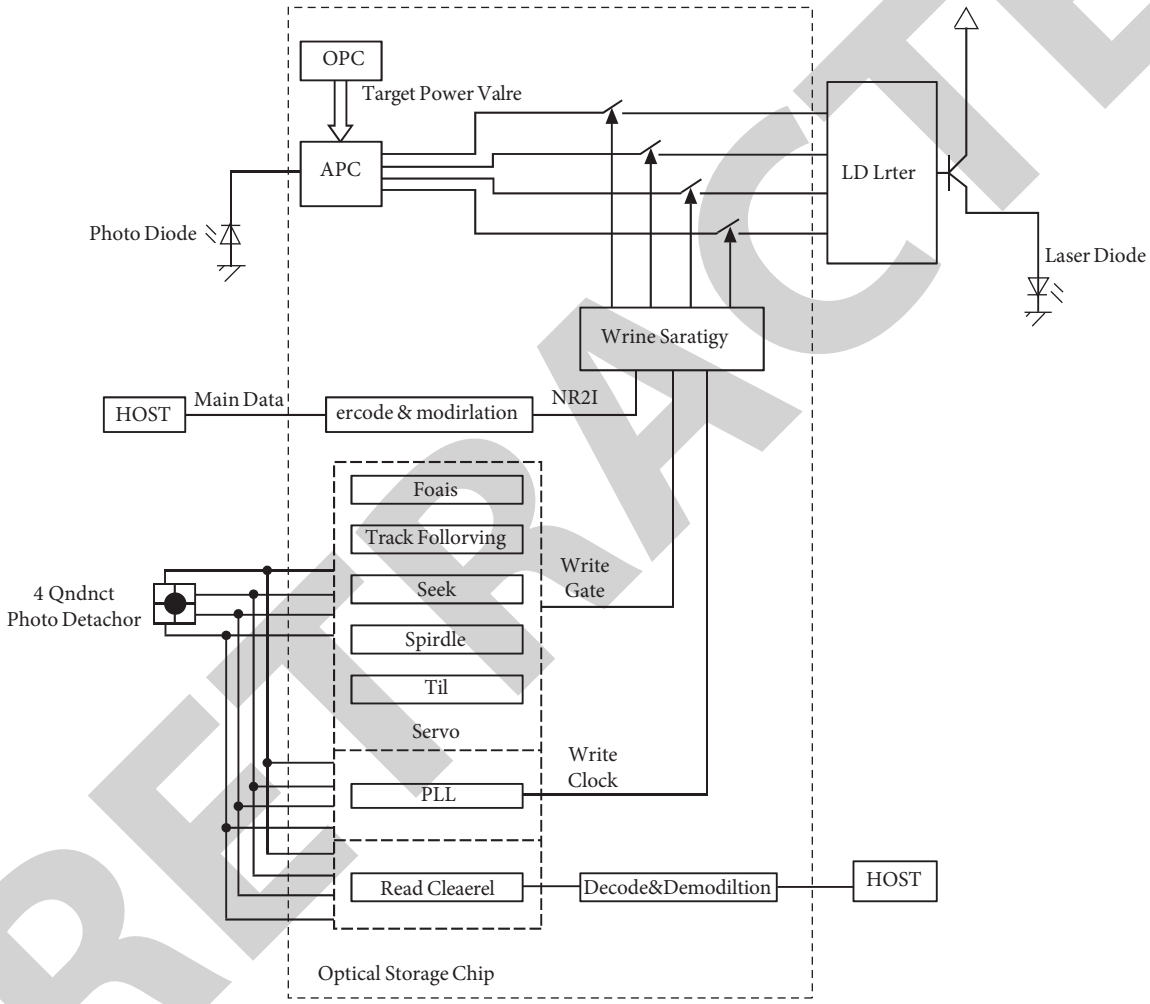

Figure 2: Optical disk data storage backup chip structure diagram.

(6) The function of the servo subsystem is to ensure the correct tracking scan relationship of the read/write laser spot to the track traces. The correct tracking and scanning relationship between the spot and the traces mainly includes space and time aspects. Spot in space and the trace to maintain the correct tracking relationship means: the optical head and disc for high-speed relative motion, on the one hand, must make the disc signal surface always fall in the reading beam about 2um depth of focus range, which is mainly by the tilt servo, height servo, and focus servo to achieve it: on the other hand, to ensure that the reading spot can always be scanned on the trace, which is mainly by the tilt servo, tracking servo, and feed servo to achieve it. This is mainly achieved by the tilt servo, the tracking servo, and the feed servo. The rate of the correct scanning relationship is to ensure that the reading rate is correct, so that the playback signal and the time base of the recorded signal are consistent, which is mainly by the spindle servo and playback signal processing system to achieve it.

(7) Read channel subsystem function is through the Partial Response Maximum Likelihood (PRML) technology, that is, the use of logic rules to analyze a set of data read out by the optical head, inducting a signal closest to the standard data method to convert the data signal RF into NRZI signal.

(8) Decoding and demodulation subsystem is the inverse process of encoding and modulation subsystem, whose function is to recover the original data, audio, or video information burned according to the NRZI signal output from the read channel subsystem. The eight subsystems of the optical storage backup chip work in coordination to complete the read and write operation of the optical disc data together.

3. New Automatic Laser Power Control Design Scheme for Digital Information

The conventional sampling/holding analog circuit uses nonuniform sampling, which has a costly design and a complex structure that cannot accommodate more levels of power. In this paper, a new all-digital automatic laser power control design is used to depart from the conventional sample/hold circuit design introduced earlier, avoiding the generation of high-frequency nonuniformly sampled clock signals and making the structure of automatic laser power control simple and easy to implement.

3.1. New Automatic Laser Power Control Design Principle. Automatic laser control, as a closed-loop control system, is much less frequent for power detection and adjustment than the frequency of laser power signal changes [6]. Therefore, instead of using the average value of the laser power at each level as the feedback of the closed-loop control system by the power sampling value of the sampling/holding circuit, a scheme is proposed with a power adjustment frequency of 20 kHz at each level. This closed-loop control scheme using the average value of the laser power can be implemented entirely by hardware, that is, FPAG implementation, which greatly increases the design flexibility and reduces the design cost (Figure 3).

First of all, since the output-PDNI signal of the laser detection diode DP, which represents the power situation at all levels of the disc storage and recording process, is an analog signal, and the FPGA can only process digital signals, the PDIN signal is first converted into a digital power signal by a digital-to-analog converter chip ADC, and then the converted digital signal enters the FGPA according to a certain. Then, the converted digital signal enters the FGPA according to a certain rule for classification and processing and outputs the feedback control signal for each power. The feedback control signal is used to control the laser emitter, but also it must be converted from digital signals to analog signals, and the design uses PWM plus analog low-pass filter method instead of digital/analog converter chip DAC to complete the conversion of digital signals to analog signals; the converted analog signal directly controls the laser emission of all levels of power to achieve the role of stable power. The Soc, ACP, and P delete parts in the above figure are done in FPGA, the first-order analog low-pass filter is implemented with hardware analog circuit, and the analog/digital conversion is done with the AD/converter chip [7, 8].

3.2. New Automatic Laser Power Control FPAG Design. The new automatic laser power control FGPA design consists of three main parts, namely, Soc, ACP, and PWM. The principle of connecting the three parts is shown in Figure 4.

In the figure, Soc is the core of the whole optical memory backup chip, controlling the reset (RESET) and enable (EN) of each subsystem and providing the clock signal (CLK) for each subsystem, and it can read and write with each subsystem through the three control signals of read (RD), write (WR), and chip select (CS), the 32-bit data input bus (DINO ~ DIN31), the 32-bit output data bus (DOUTO-DOUT31), and 32-bit address bus (ADDRO ~ ADDR31) for read and write operations with each subsystem. For ACP subsystem, Soc mainly completes system reset and enable of ACP subsystem and PWM, provides clock for ACP subsystem and PWM, and sets control and status registers of ACP subsystem.

APC structure is the main structure of APC subsystem. There are two main functions: one is to complete the control of AD/chip, including the setting of AD/chip working mode (by setting the control register of AD/chip), the generation of control signals of AD/chip (clock signal ADCLK, enable signal ADCS, read control signal ADRD, write control signal ADWR, and receiving A/*D* conversion completion signal ADINT and A/*D* conversion result (ADD0~ADD9)); secondly, the result of AD/conversion (ADD0~ADD9) is processed to get the digital drive signal of the laser emitter, that is, laser emitting power signal read laser power, that is, RP0-RP9, write laser power WP0~WPg9 erase laser power BP0~EP9, and bias laser power BP0~BP9.

The purpose of the PWM is to replace the expensive D/A converter with a digital circuit design that changes the DC component of the output by modulating the duty cycle of the square wave, and after a low-pass filter to get the desired level signal, complete the transformation of the digital signal to the analog signal. The design of the analog low-pass filter is shown in Figure 5. Each power level corresponds to a set of PWM with analog low-pass filter [9, 10].

The new all-digital makes the power level increase, and APC design scheme can be closed-loop control of each level of laser emission power; that is, it only needs to increase the APC structure, and the increase in its hardware structure is extremely limited, as well as the structure of the power signal processing and PMW junction, and there is no technical bottleneck.

3.3. New Automatic Laser Power Control Design for a/D Conversion. The analog/digital converter chip in this design is the TLV1571 chip from TI. The TLvl571 is a 10 bit single-channel analog input analog/digital converter with two internal 8-bit control registers COR and CRI to control the ADC operating modes, including software conversion or hardware conversion start selection, internal or external clock selection, and binary or binary-complement output.

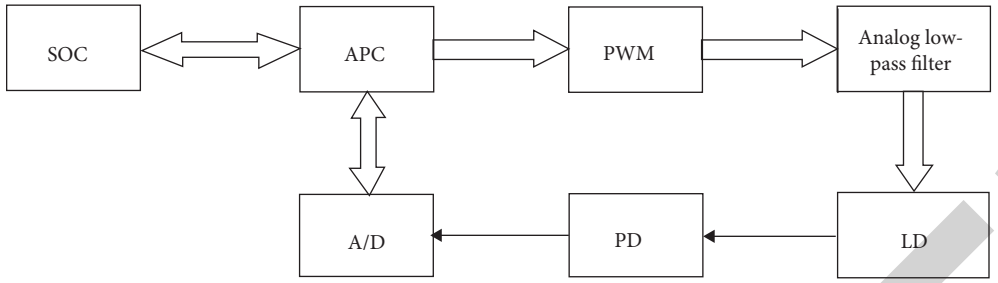

Figure 3: Structural block diagram of the new all-digital ACP design.

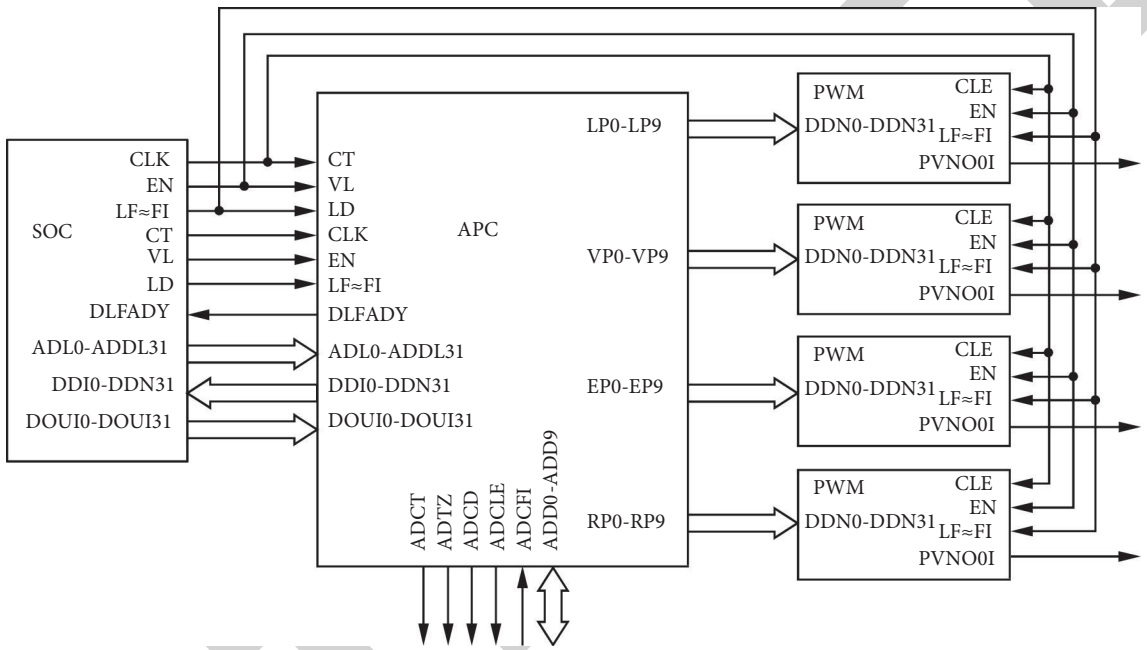

Figure 4: New automatic laser power control FGPA internal structure diagram.

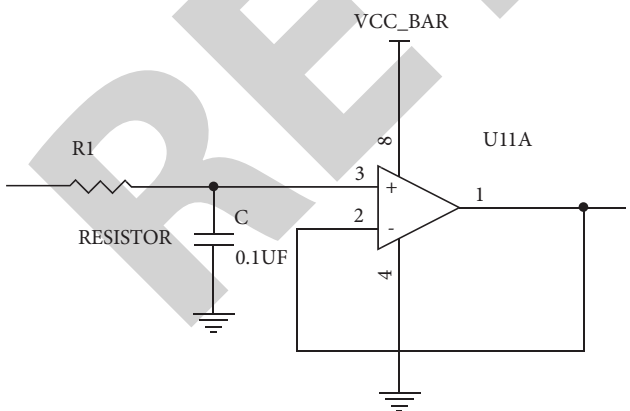

Figure 5: Analog low-pass filter circuit diagram.

The following diagram shows the operating modes of the TLV1571. Figure 6 shows the block diagram of the TLV1571 functional structure.

AIN is the input analog signal port of TLV1571; D0~D9 are 1b0ti tristate bidirectional data bus; when used as input, D0~D9 is used to set two 8-bit control registers, among which D0~D7 is used as the setting value of control registers, and D8 and D9 are used as the address selection of two control registers; when used as output, D0~D9 are the result of A/*D* conversion output. CLK is the input clock signal port of TLV1571, and TLV1571 supports internal clock signal and external clock signal in two ways: the internal clock signal frequency range is gMHz~22 MHz, and the external allowed input clock frequency range is l-20 MHz; RD, WR, and CSTART are the control signal input ports for A/*D* conversion, which control the way and time of AD/conversion.

When the TLV1571 performs A/*D* conversion, its AD/sampling takes 6 clock cycles, AD/conversion takes 10 clock cycles, and output data takes at least one clock cycle, so the maximum A/*D* conversion frequency $f = f(1/17)$. The design controls the conversion working mode by setting the two control registers of the TVL1571 to the external clock signal, and its working timing is shown in Figure 7.

When both CS and WR signals are low, the control register of TLV1571 is written. After setting the control register of TLV1571, the AD/sampling starts at the rising edge of WR, and after the sampling lasts for 6 clock cycles,

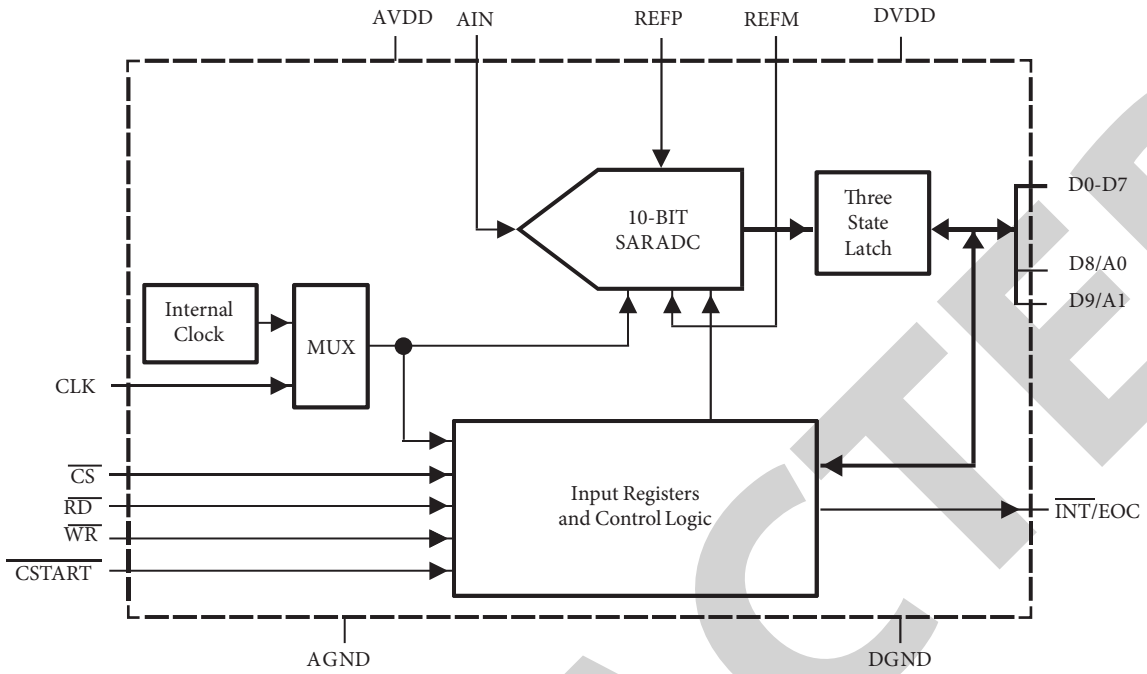

Figure 6: Block diagram of the functional structure of the TLV1571.

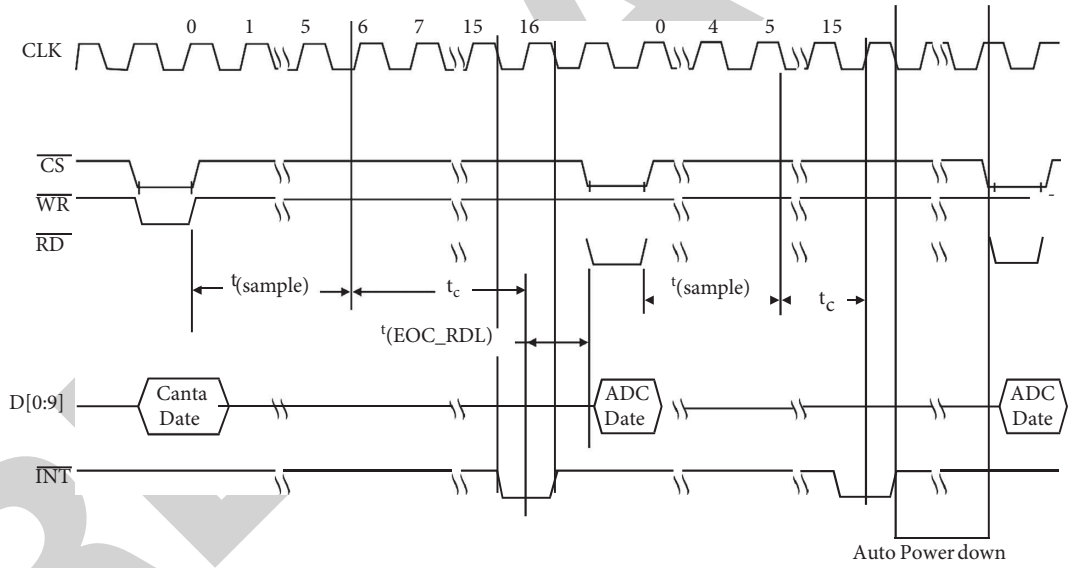

Figure 7: TLV1571 operating timing diagram.

the A/*D* conversion is automatically performed, and the conversion takes 10 clock cycles. After the conversion is completed, INT becomes low to notify the FGPA that the AD/conversion has been completed, and at the same time, the AD converted digital signals are prepared on the D0~D9 data bus, and at the falling edge of the RD signal, the data is read into the FPAG for next processing. The clock signals CKL, CS, WR, and RD of the TLV1571 are generated by the FPGA. D0~D9 are connected to the 10 bidirectional I/O ports of the FPGA for completing the two control registers of the TLV1571 settings and the transfer of AD/conversion results. Figure 8 shows the circuit diagram of TLV1571 and FPGA connection.

3.4. Advantages of the New All-Digital Automatic Laser Power Control Design. The new fully digital automatic laser power control design applies the FGPA design, which has the following advantages over the conventional sample/hold circuit design.

Hold circuit design; it has the following advantages.

(1) The sampling frequency of the ADC is fixed and determined by the selected ADC model, so it is not necessary to use a special structure to generate the sampling clock signal, and the sampling conversion frequency of the ADC can be easily adjusted according to the actual needs.

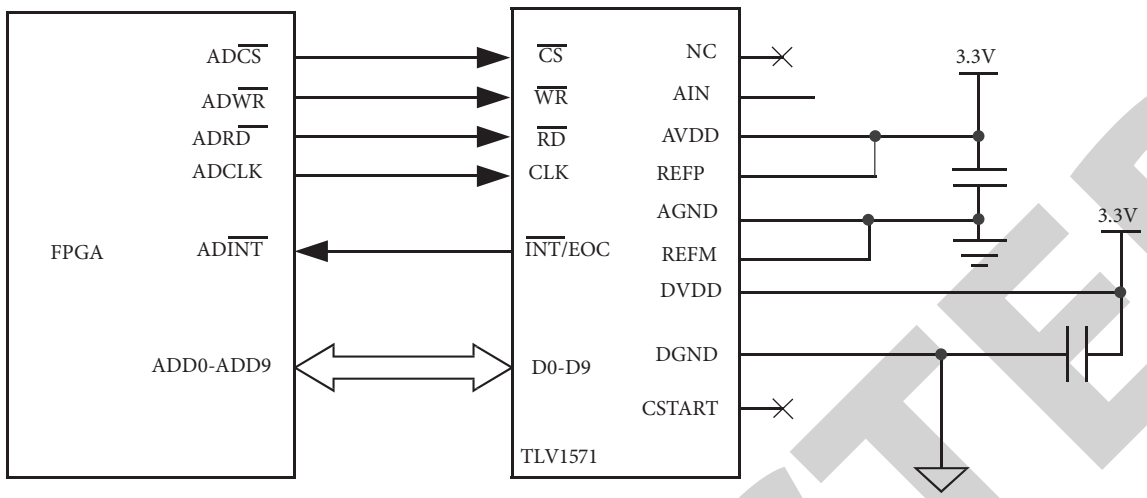

Figure 8: TLV1571 and FPGA connection circuit diagram.

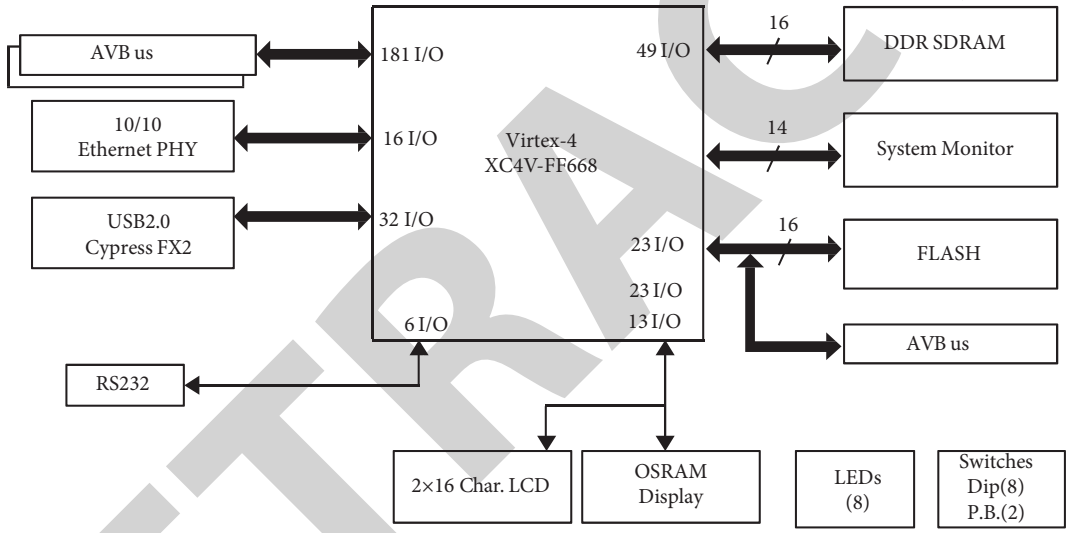

Figure 9: Block diagram of AVNET's XC4vLX25-FF668 FGPA evaluation board.

(2) The sampled signal is classified into its corresponding power level (write power, read power, and erase power) by the power level classification standard, which will not generate misjudgment and misadjustment caused by missampling.

(3) According to the different discs, the power level classification is bound to be different. By setting the value of the corresponding power level register, the power level classification standard can be easily changed, which greatly increases the flexibility of the design.

(4) Through the division of the power level, avoid the sampling difficulty caused by the read/write pulse is too narrow, and use other power level to replace the judgment, for Blu-ray technology, even if the power level increases, and we only need to increase the ACP structure of the power signal processing structure and PWM structure, the increase of its hardware structure is extremely limited, and there is no technical bottleneck.

(5) Use the cumulative average value instead of the actual power to avoid misjudgment caused by sudden noise.

(6) PWM plus analog low-pass filter design instead of D/A chip greatly reduces the design and production costs.

This greatly reduces the design and production cost.

4. Experiment and Analysis Based on FPGA

This design uses the FGPA evaluation board designed by Avnet Design Services, which uses Xilinx's XC4VLX25-FF668 type FGPA chip. Figure 9 shows the block diagram of AVNET's XC4vLX25-FF668 FGPA evaluation board structure.

In addition, there are 32 MB DDRSDRAM and SMB Intel StrataFlash, 10/100 M adaptive Ethernet interface, USB2.0 interface and RS232 serial interface, 128 × 64 OLED graphic display, 3 sets of 140-pin universal I/O connectors

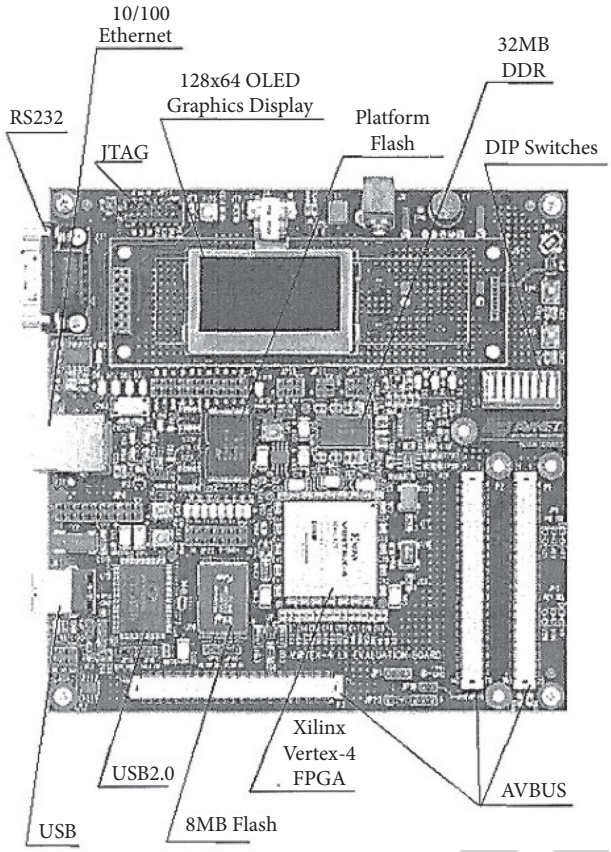

Figure 10: AVNET's XC4VLX25-FF668 type FPGA evaluation board.

(AvBus), and other hardware structures. Figure 10 shows AVNET's XC4VLX25-FF668 FPGA evaluation board.

The XC4vLX25-FF668 FPGA evaluation board has two types of board-level clock inputs, 50 M and 100 M, and its configuration methods include boundary-scan and serial and parallel configuration.

XC4VLX25-FF668 is a Virtex-4 series field programmable gate array FGPA from Xilinx, the first LX high-performance logic application solution, and platform FPGA based on the ASMBL architecture. XC4VLx25-FF668 uses 300 mm (12-inch) wafer technology and 90 nm CM0s copper process manufacturing, reducing dynamic power consumption, while we use trigate oxide layer technology to reduce static power consumption, and compared with the previous generation of FGPA, the net power consumption reduced to 50%, while compared with other competitive products using 90 nm technology, it also has the following significant advantages.

(1) xe4vLx25 a FF66s type FPGA is 96×28 array structure, with 24,192 logic cells (Logic, Cells), 10,752 Slices structure, and its maximum configurable 168 kb RAM.

(2) With 48 XtermeDSP51iecs, it provides the highest performance, the lowest power consumption, and the most functional arithmetic units, and it can implement multiply one accumulation unit or cascade with other similar modules to achieve a larger design architecture; in addition, the DPS module can also be configured to work at 500 MHz counters, barrel shift registers, address subtractors, accumulators, and other structures. This performance and scalability can be used to implement highly integrated and performant DSP functions without taking up general-purpose logic resources.

(3) With 72 built-in block RAMs, each block RAM can store 18 kb, and two adjacent block RAMs can be combined to form a 32 kb memory. The combination of block RAMs can be easily configured into synchronous or asynchronous SRAM, DSARM, synchronous/asynchronous FIOF, ORM, CAM, and other memory forms according to user requirements.

(4) With eight digital clock managers DCM, each DCM can be used to eliminate clock distribution delay, clock multiplication, frequency division, shifting, and other operations; in addition, the DCM also has clock synthesis capabilities; the most critical is as follows: DCM processing of the resulting clock signal has good timing characteristics, and the signal can be directly connected to the global clock network to improve the driving capability and reduce the clock DCM, and global clock multiplexer provides a complete solution for designing high-speed clock networks.

(5) The Phase-Matched Clock Dividers (PMCD) module with four new phase-matched clock dividers provides 32 ps accuracy, simplifying clock synthesis and alignment. The differential clock tree is utilized to ensure minimal distortion and jitter.

(6) With 11 input/output banks (Totle I/O Banks), the most flexible I/O interfaces and XCITE serial/parallel/differential active I/O ports are supported, thus providing the highest performance, enhanced power, and better signal integrity for both single-ended and differential I/O.

(7) With 448 user-available 1/0 pins.

(8) The Generic Routing Matrix (GRM) provides an array of routing switches between each programmable part to connect the components of the XC4vLX25-FF668 to the routing matrix, and all components use the same interconnect mechanism.

The FPGA design process for this design includes several major steps: design input, functional simulation, synthesis, postsynthesis simulation, implementation, post-layout-wiring simulation, and download verification debug.

The design input usually includes schematic input, hardware description language HDL input, waveform input, state machine input, and a combination of several input methods. The design input for this design is VHDL hardware description language; after the design input is completed, the design should be simulated using simulation tools to verify whether the designed circuit meets the design requirements, and if not, go back to the design step and modify the original design until it meets the design

requirements. Functional simulation can identify errors in the design and speed up the design process. After the completion of the functional simulation to synthesize the design, synthesis refers to the process of converting the design input into a logic connection diagram consisting of basic logic units such as with, or, nongates, RAM, flip-flops, etc.; after the completion of the synthesis, the same is needed for postsynthesis simulation to check whether the synthesis results are consistent with the original design, as well as the synthesis in the postsynthesis simulation, and the generated delay file is backlabeled to the model of the postsynthesis simulation to check the working situation after adding the delay of the device, and if the simulation result shows that it does not match with the design requirements, it should go back to the input or synthesis stage for modification until it reaches the design requirements. Since the result of synthesis still has a certain gap with the actual configuration, the implementation step is also performed. Implementation is the process of configuring the basic logic cells generated by synthesis to specific FGPA devices, and it is composed of three substeps: translation, mapping, and layout wiring. After implementation, there is another simulation, that is, post-layout-wiring simulation. The post-layout-wiring simulation includes both device delay and delay caused by layout and wiring, which can basically reflect the actual working condition of the chip correctly. Similarly, if the result of post-layout-wiring simulation cannot meet the design requirements, the link that produces the difference should be found whether it is in the design input stage, synthesis stage, or implementation stage, and go back to the corresponding stage for modification until it meets the design requirements. When all the simulations meet the requirements, it is time to configure and verify the FGPA chip. Only the design that is successfully verified on the FGPA chip is a design that really meets the design requirements. In addition, in the synthesis and implementation process, the performance of the design can usually be improved by adding constraints, including timing constraints, pin constraints, and area constraints.

4.1. Write Policy Subsystem FGPA Design and Verification. In this paper, the top-level structure of the block-type and pulse-type write strategy subsystems are given, and the layout wiring after the design of the block-type and pulse-type write strategies are given as an example for the CD-R preheat method and the DVD-R preheat method, respectively. The real waveforms of the block-type and pulse-type write strategy designs are given in the example of CD-R preheat and DVD-R preheat.

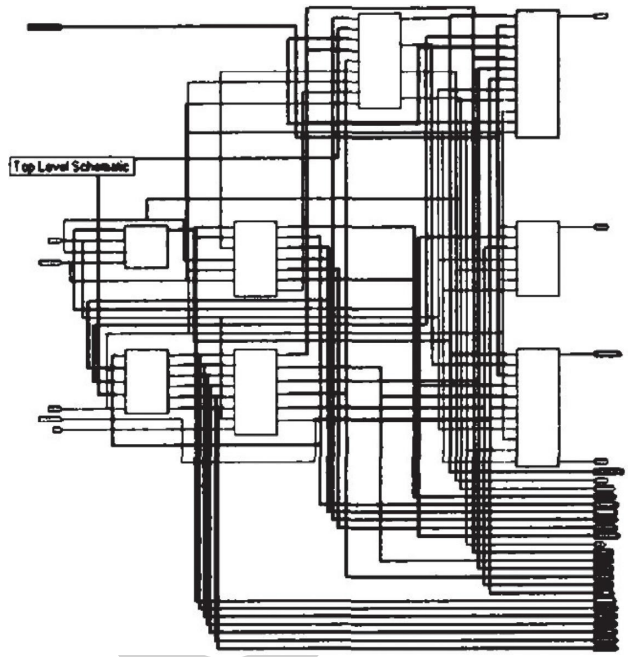

Figure 11: Top-level structure diagram of FPGA-designed block writing strategy.

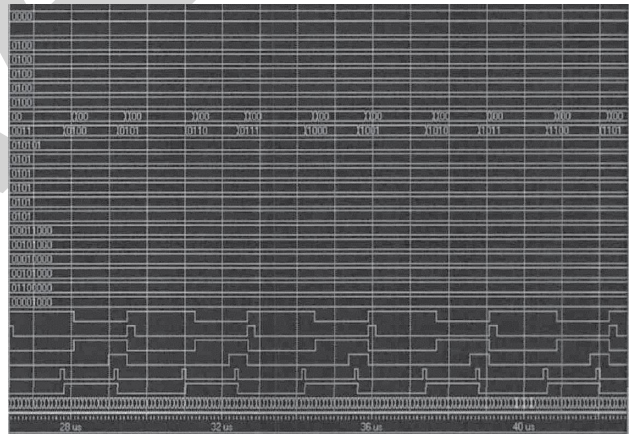

Figure 12: Simulation waveform after wiring the block-type write strategy layout in CD-R preheat mode.

4.1.1. Block Write Strategy FPAG Design and Verification

(1) Top-level structure of block write strategy for FPGA design

The top-level structure of the block write strategy for FPGA design is shown in Figure 11.

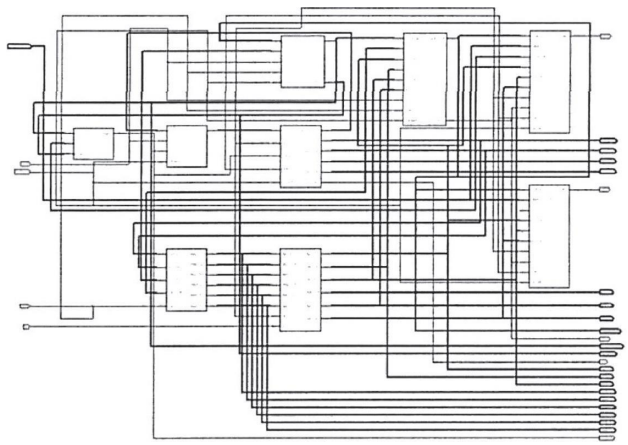

Figure 13: Top-level structure diagram of the FGPA-designed pulse-based writing strategy.

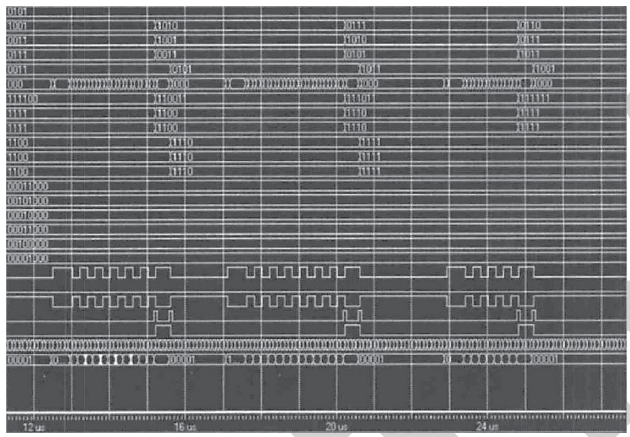

Figure 14: Simulation waveform after layout wiring of DVD-R preheat method with pulse-type write strategy.

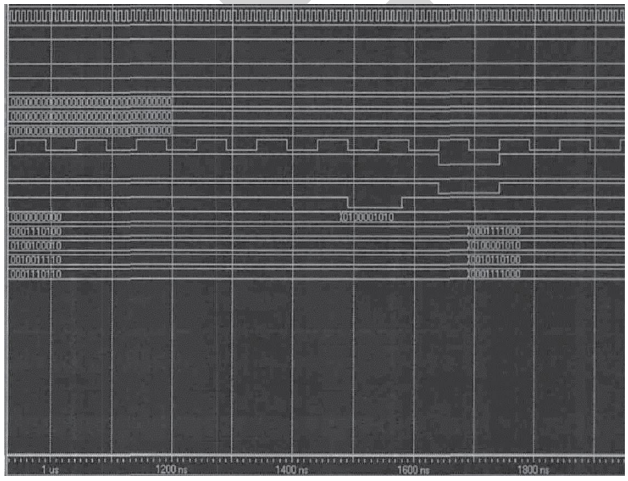

Figure 15: Simulation waveform of automatic laser power control subsystem after layout and wiring.

(2) Simulation waveform after the layout and wiring of block-type write strategy in CD-R preheat mode

Figure 12 shows the simulation waveform after the layout and wiring of the CD-R preheating method with block-type write strategy.

4.1.2. Pulse Mode

(1) Top-level structure of the FGPA-designed pulse-type write strategy

The top-level structure of the pulse-based write policy designed by FPGA is shown in Figure 13.

(2) Simulation waveform after layout wiring of DVD-R preheat method with pulse-type write strategy

Figure 14 shows the simulation waveform after the layout and wiring of DVD-R preheat method with pulse-type write strategy.

4.2. Automatic Laser Power Control Subsystem FGPA Design and Verification. Figure 15 shows the simulation waveform of the automatic laser power control subsystem after layout and wiring.

5. Conclusion

With the rapid development of modern road traffic, the development of advanced information technology, electronic communication technology, automatic control technology, computer technology, sensor technology, and network technology, and their penetration in the field of road traffic, the storage and backup of massive traffic information have become an extremely important link in traffic transportation and management. The optical storage backup technology designed in this paper has the advantages of high recording density, large storage capacity, long service life, easy storage, low storage cost, and strong compatibility. It will replace the existing disk and tape storage backup technology and become the mainstream of traffic information storage backup in the future.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References

[1] H. Xu, X. Zhao, and K. Guan, *Theory and Application of Highway Toll Collection System*, Electronic Industry Press, Beijing, China, 2003.

[2] W. Huang and R. Chen, *Introduction to Intelligent Transportation System (ITS)*, People's Traffic Publishing House, Nanchang, China, 1999.

[3] G. Fu Xi, "The development of optical disk storage technology, products and market," *Journal of Qufu Normal University*, vol. 1, no. 1, pp. 45–51, 1996.
[4] Yi Xu, "Prospects for the development of information storage and display technology," *Recording Media Technology*, vol. 4, no. 7, pp. 20-21, 2004.
[5] W. M. Liu, Z. R. Wang, and X. T. Zheng, *Theory and Methods of Highway Toll Collection System*, People's Traffic Publishing House, Nanchang, China, 2000.
[6] E. Takahashi, Y. Suzuki, and H. Inagaki, "Reliability of phthalocyanine CD-R," *Teeh. Digest of International Symposium on Optical Memory*, vol. 4, pp. 157-158, 1995.
[7] A. Ren, X. Chu, C. Chang, and X. Sun, *Embedded System Design Based on FPAG*, Xi'an University of Electronic Science and Technology, Xi'an, China, 2004.
[8] Z. Huang and S. Li, "Reactivation of learned reward association reduces retroactive interference from new reward learning," *Journal of Experimental Psychology: Learning, Memory, and Cognition*, vol. 48, no. 2, pp. 213–225, 2022.
[9] X. Yang and G. M. Li, "Research progress of modulation technology in optical disc storage," *Laser and Infrared*, vol. 3, pp. 12–14, 2004.
[10] R. Huang and X. Yang, "Analysis and research hotspots of ceramic materials in textile application," *Journal of Ceramic Processing Research*, vol. 23, no. 3, pp. 312–319, 2022.