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*Research Article*

# Design of an Interleaved High Step-Up DC-DC Converter with Multiple Magnetic Devices for Renewable Energy Systems Applications

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An interleaved high step-up converter topology based on the coupled inductor (CI) and built-in transformer (BIT) is proposed in this study to provide high step-up voltage gain and high efficiency with a low number of power electronic components for renewable energy applications. The voltage gain is increased by both of the turns' ratio of CI and BIT, so there is no need to extend duty ratio to obtain high voltage gain. The proposed topology is much more flexible than those with only either CI or BIT. Moreover, the voltage stress across semiconductor devices can be relatively decreased by adjusting the turns' ratio of the CI and BIT. In addition, the input current ripple can be reduced when the interleaved structure is applied at the input of this converter. Furthermore, turned-OFF and turned-ON zero current switching (ZCS) conditions for the diodes and power MOSFETs are achieved, respectively, thanks to the leakage inductances of the magnetic devices. Hence, due to the control of the falling current rate of the diodes by the leakage inductances, reverse recovery problem is alleviated. Moreover, the energy of the leakage inductances is recycled by the clamp capacitors avoiding high spikes across MOSFETs. As a result, according to the abovementioned advantages of the proposed converter, MOSFETs with low ON-state resistance and diodes with low forward voltage drop can be used to decrease the conduction losses. A 600 W laboratory prototype with 27–400 V voltage conversion at switching frequency 50 kHz is built to verify the performance of the proposed converter. Experimental results confirm the theoretical analysis. The efficiency reaches to 94.6% at full load which is close to the calculated of 95.8%.

## 1. Introduction

Renewable energy sources, such as photovoltaic (PV) and fuel cell (FC), have been receiving more attention in recent years as a result of a substantial increase in demand for clean energy, concerns related to electricity generation based on FC, and environmental effects of greenhouse gas (GHG) emissions [1]. The output voltage of FCs and PV panels are relatively less than the required amount. In isolated converters, high voltage gain can be achieved by adjusting the transformer ratio. In [2, 3], isolated LLC resonant converters have been proposed. Introduced configuration in [2, 3] not only reduces the voltage stress across MOSFETs to half of the input voltage in the low voltage side but also makes the converter suitable for high power applications. Moreover, high operation frequency, high energy density, and wide output ranges are advantages of such converters. Meanwhile, nonisolated converters are typically used to increase the output voltage of PV panels and FCs. The conventional boost converter (CBC) with a simple structure and low cost can be used as a fundamental solution [4]. As a result, appropriate voltage levels can be reached for the inverter-fed AC utility when connecting to the electricity grid. However, the CBC should operate in a high duty ratio to achieve high step-up voltage gain, leading to problems such as the increased voltage rate of power MOSFETs and high peak currents.

Consequently, power MOSFETs with higher on-state resistance should be selected, increasing conduction losses, reducing performance operation, and decreasing conversion efficiency [5]. In [6], a quadratic boost converter is used to increase the voltage step-up gain. Although it does not call for a high duty ratio, this structure still suffers from the high voltage stress across power MOSFET. Switched capacitor (SC) and switched inductor (SI) topologies (known as transformer-less converters) are presented in [7–11] to increase voltage gain. However, SI-based structures suffer from problems such as high voltage stress across semiconductor devices. To deal with this problem, voltage multiplier cell (VMC) converters are introduced [12–14]. These converters can achieve high voltage gain while reducing cost, voltage stress, and duty ratio. By increasing the number of VMCs, voltage gain can be boosted. However, the more the number of VMC is, the more the circuit complexity will be. High switching losses and reverse recovery due to operating under hard switching conditions are other issues associated with these converters. Coupled inductors (CI) are other structures to obtain high step-up voltage gain [15–22]. They can provide zero current switching (ZCS) turn-on for MOSFETs thanks to the leakage inductances of the CI, which will decrease switching losses and attenuate the reverse recovery problem. Nevertheless, voltage spike during switching transition due to the leakage inductor is the main disadvantage of CI-based converters. Passive clamp circuits can be implemented to recycle the leakage-inductor energy and avoid efficiency degradation. To decrease voltage stress across semiconductor devices, improve efficiency, and recycle the leakage-inductor energy, CIs can be implemented with VMCs [23–26]. A high step-up converter is developed in [23] with low voltage stress across the main power switch, in which voltage gain is increased by applying one CI and two VMCs. Moreover, a capacitor is being charged during the switch-off period using the energy stored in the CI, increasing the voltage transfer gain. The energy stored in the leakage inductance is recycled using a passive clamp circuit, reducing voltage spike during switching transition. In addition, a built-in transformer (BIT) can be utilized with CI to improve voltage gain further. Due to the zero average current of the primary windings of the BIT, the RMS current is also reduced. Thus, a low volume core can be selected when fabricating the BIT. Nevertheless, the single-phase nature of these converters restricts them to low power levels. To use high voltage gain converters at high power, minimize the input current ripple, and increase reliability, interleaved converters have been introduced. The abovementioned structures (i.e., SC, CI, and VMC) are adopted to interleaved topologies to achieve high step-up voltage gain [27–39]. An interleaved boost converter with a bi-fold Dickson voltage multiplier is presented in [40], in which several diodes and capacitors are employed to increase the overall voltage gain. However, the added number of diodes and capacitors increases losses and reduces efficiency. Another interleaved boost converter using two CIs and a VMC is developed in [41], achieving a very high step-up voltage gain without a high turn ratio. The voltage stress across the semiconductor switches and the passive components is reduced to lower than the output voltage. Interleaved high step-up converter presented in [42] uses BIT and VMC to have more flexible voltage gain. This topology delivers benefits such as high voltage gain, low voltage stress across the power MOSFETs, a low number of components, and low input current ripple. To reduce the size and improve transient response, switching frequency should be increased, leading to increased switching losses. Interleaved boost converter in [43] utilises the clamp capacitors and integrates the secondary winding of the BIT. Nevertheless, the voltage gain is low and can be increased when adding CI structure.

In this study, a new interleaved topology is proposed by locating the secondary windings of the CI between the main MOSFETs and the primary winding of the BIT. In such a topology, the voltage gain is proportional to the multiplication of the turn ratios of CI and BIT. The proposed converter delivers the following advantages:

(1) High voltage gain (as a result of windings of the BIT and CI)

(2) Low voltage stress across MOSFETs and diodes

(3) Low input current ripple

(4) Zero current switching (ZCS) turned-OFF condition for diodes

(5) Zero current switching (ZCS) turned-ON condition for MOSFETs

(6) Alleviated reverse recovery problem of the diodes

(7) High conversion efficiency

(8) Low number of components

The rest of this study is organized as follows. The proposed converter and its operational principle are presented in Section 2. The performance analysis of the proposed converter is studied in Section 3. Performance comparison and numerical design are discussed in Section 4 and 5, respectively. The experimental results are given in Section 6. Finally, conclusions are drawn in Section 7.

## 2. Operational Principle of the Proposed Converter

The abstract model of the proposed converter is illustrated in Figure 1. As can be seen, the built-in transformer (BIT) and coupled inductor (CI) structures are utilized in this converter. This converter can achieve high voltage gain by adjusting the turns' ratio of the BIT and CI. Two main power MOSFETs ($S_1$ and $S_2$), four diodes ($D_1, D_2, D_3, D_4$), and three capacitors ($C_1, C_2, C_3$) are some other components of this converter. $L_{m1}$ and $L_{m2}$ also represent the leakage and magnetizing inductances of the CIs, respectively. BIT consists of primary, secondary, and tertiary windings with $N_1$, $N_2$, and $N_3$ number of turns. $L_{LKb}$ also indicates its leakage inductor. Turns' ratios of the CI and BIT are defined as $n = n_2/n_1$ and $N = N_2/N_1 = N_3/N_1$, respectively. The proposed converter has 10 main operating modes in a single switching period. However, due to the symmetrical feature of the topology, only five operating modes are analyzed in detail in the following. The key waveforms of the proposed converter

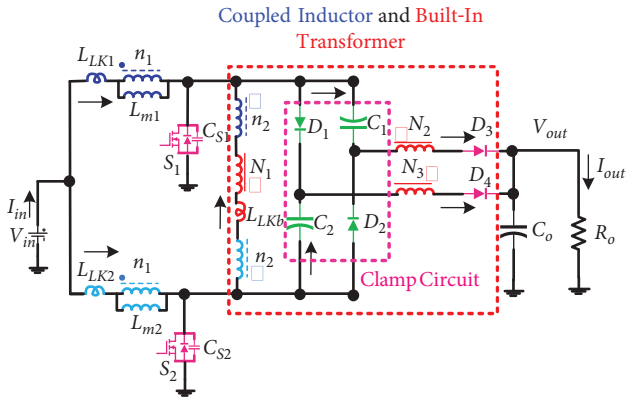


Figure 1: The abstract model of the proposed converter.

and the related equivalent circuits in each mode are depicted in Figure 2 and Figure 3, respectively.

*2.1. Mode 1 $[t_0 - t_1]$.* During this mode, both power MOSFETS $S_1$ and $S_2$ are in ON-state, and all the diodes are reverse-biased. The magnetizing inductances of the CIs are linearly charged by the input voltage, and the output capacitor supplies the output load:

$$I_{Lm1}(t) = i_{LK1}(t) = i_{S1}(t) = \frac{V_{\text{in}}}{L_{m1} + L_{LK1}}(t - t_0) + I_{Lm1}(t_0), \quad (1)$$

$$I_{Lm2}(t) = i_{LK2}(t) = i_{S2}(t) = \frac{V_{\text{in}}}{L_{m2} + L_{LK2}}(t - t_0) + I_{Lm2}(t_0). \quad (2)$$

*2.2. Mode 2 $[t_1 - t_2]$.* At $t_1$, $S_2$ is turned-OFF. During this mode, the parallel capacitor $C_{S2}$ is being linearly charged by the current of $i_{Lm2}$. The voltage across the switch $S_2$ is given by

$$v_{DS2}(t) = \frac{I_{L_{m2}}(t_1)}{C_{S2}}(t - t_1). \quad (3)$$

*2.3. Mode 3 $[t_2 - t_3]$.* At $t_2$, the diodes $D_2$ and $D_4$ are turned-ON. In this mode, the leakage inductance $L_{LK2}$ is discharged into the clamp capacitor $C_1$. A positive voltage is applied across the primary winding of the BIT. The output load is supplied by the output capacitor and the secondary winding of the BIT:

$$I_{Lm2}(t) = i_{D2}(t) + [N(n+1)+1]i_{D4}(t), \quad (4)$$

$$i_{LKb}(t) = Ni_{D4}(t), \quad (5)$$

$$i_{DS1}(t) = I_{Lm1}(t) + i_{D2}(t) + N(n+1)i_{D4}(t), \quad (6)$$

$$i_{D4}(t) = \frac{[N(n+1)+1]V_{C1} + V_{C2} - V_O}{n^2(L_{LK1} + L_{LK2}) + N^2 L_{LKb}}(t - t_2). \quad (7)$$

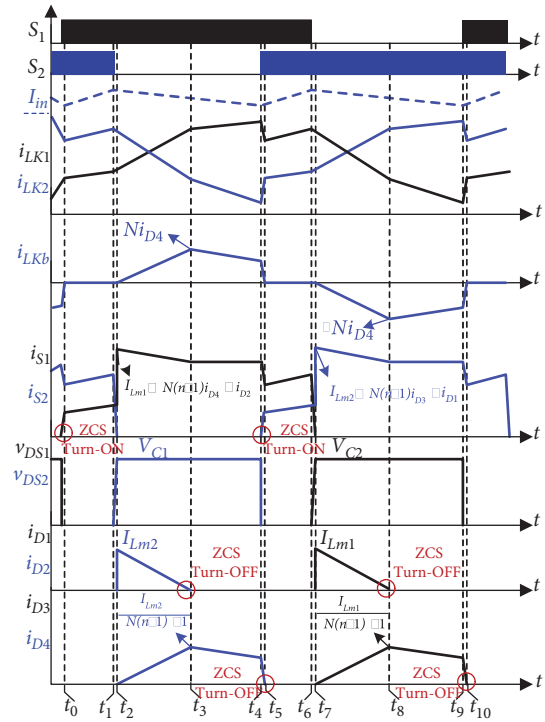


Figure 2: The key waveforms of the proposed converter.

*2.4. Mode 4 $[t_3 - t_4]$.* At $t_3$, the current of diode $D_2$ reaches to zero, and it is turned-OFF with ZCS. During this mode, the clamp capacitor voltage $V_{C1}$ is equal to the voltage across power MOSFET $S_2$. The current flowing through $D_4$ is proportional to the leakage inductor's current $i_{LKb}$. At the end of this mode, the turn-ON pulse is applied to $S_2$ and turns it ON with ZCS performance:

$$I_{Lm2}(t) = [N(n+1)+1]i_{D4}(t), \quad (8)$$

$$i_{DS1}(t) = I_{Lm1}(t) + N(n+1)i_{D4}(t). \quad (9)$$

*2.5. Mode 5 $[t_4 - t_5]$.* At $t_4$, $S_2$ is in ON-state. During this mode, the current through $L_{LKb}$ is decreasing. At the end of this mode, the current flowing through $L_{LKb}$ reches to zero. In addition, the current through $D_4$ decreases and its falling rate is controlled by the leakage inductances:

$$\frac{di_{D4}(t)}{dt} = \frac{V_{C2} - V_O}{n^2(L_{LK1} + L_{LK2}) + N^2 L_{LKb}}. \quad (10)$$

## 3. Performance Analysis

*3.1. Voltage Gain Expression.* The voltage across $L_{m1}$ is equal to $V_{\text{in}}$ and $V_{\text{in}} - V_{C2}$ for the switch $S_1$ being in ON- and OFF-state, respectively. By applying the volt-second balance principle to $L_{m1}$, the voltage across the capacitor $C_2$ can be calculated as

$$V_{C2} = \frac{V_{\text{in}}}{1 - D}. \quad (11)$$

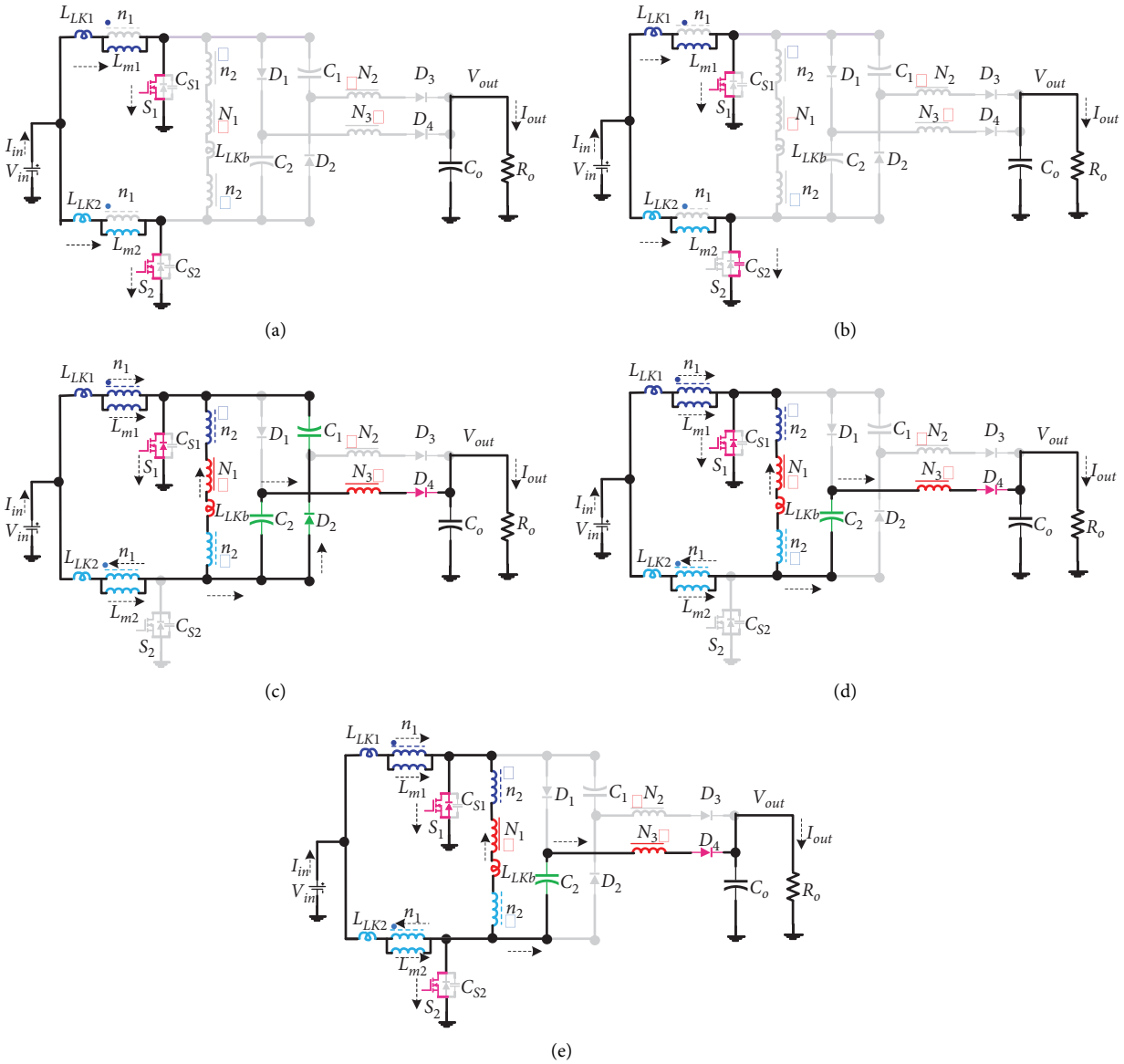


Figure 3: Equivalent circuits of the proposed converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5.

The voltage across $L_{m2}$ is equal to $V_{\text{in}}$ and $V_{\text{in}} - V_{C1}$ for $S_2$ being in ON- and OFF-state, respectively. By applying the volt-second balance principle to $L_{m2}$, the voltage across the capacitor $C_1$ can be obtained as

$$V_{C1} = \frac{V_{\text{in}}}{1 - D}. \tag{12}$$

Using the average currents of the diodes and equations (4) and (8), the curring passing through them diodes can be calculated as

$$i_{D1,\text{Ave}} = \frac{I_{Lm1}}{2} D_{78} = \frac{I_{\text{out}}}{2}, \tag{13}$$

$$i_{D2,\text{Ave}} = \frac{I_{Lm2}}{2} D_{23} = \frac{I_{\text{out}}}{2}, \tag{14}$$

$$i_{D3,\text{Ave}} = \frac{I_{Lm1}}{2[N(n+1)+1]} (2 - 2D - D_{78}) = \frac{I_{\text{out}}}{2}, \tag{15}$$

$$i_{D4,\text{Ave}} = \frac{I_{Lm2}}{2[N(n+1)+1]} (2 - 2D - D_{23}) = \frac{I_{\text{out}}}{2}, \tag{16}$$

$$D_{23} = D_{78} = \frac{2(1-D)}{N(n+1)+2}, \tag{17}$$

where $D_{23}$ and $D_{78}$ are normalized time durations of mode 3 and mode 8, respectively. Using (13)–(17), the average currents of the magnetizing inductances can be obtained as

$$I_{Lm} = I_{Lm1} = I_{Lm2} = \frac{N(n+1)+2}{2(1-D)} I_{\text{out}}. \tag{18}$$

According to Figure 2, the following equation is obtained:

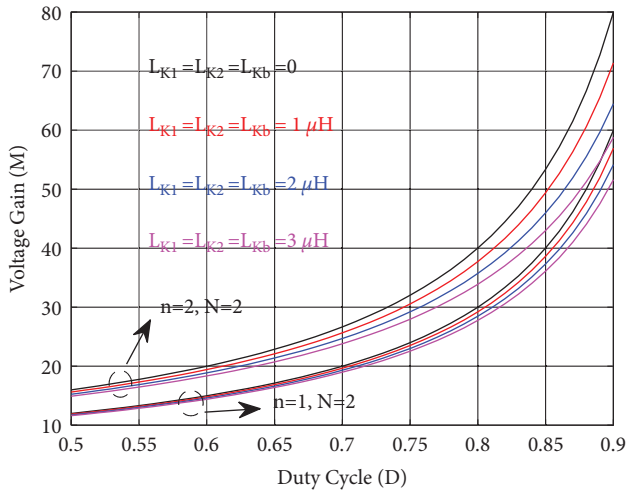


Figure 4: Voltage gain of the proposed converter.

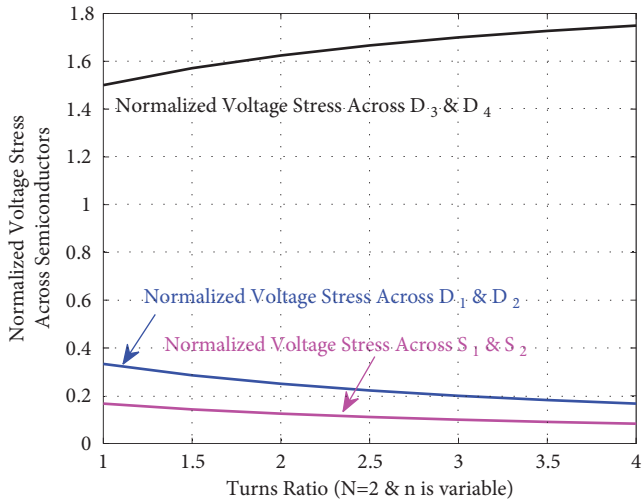


Figure 5: Normalized voltage stress across semiconductor devices.

$$\frac{\Delta i_{D4}}{\Delta t} = \frac{I_{Lm}}{[N(n+1)+1]D_{23}T_S}, \tag{19}$$

By considering the leakage inductances in the steady-state analysis, the voltage conversion ratio is derived as

$$M = \frac{V_O}{V_{in}} = \frac{N(n+1)+2}{(1-D)\left\{1+\left(Q[N(n+1)+2]^2/4(N(n+1)+1)(1-D)^2\right)\right\}}, \tag{20}$$

where $Q = ([n^2(L_{LK1}+L_{LK2})+N^2L_{LKb}]/RT_S)$.

For $Q = 0$, the ideal voltage gain of the proposed converter can be calculated as

$$M = \frac{V_{out}}{V_{in}} = \frac{N(n+1)+2}{1-D}. \tag{21}$$

The effect of the leakage inductance on the voltage gain is shown in Figure 4. As can be seen, the voltage gain of the proposed converter is decreased by increasing the leakage inductances.

*3.2. Voltage Stress Analysis of the Semiconductor.* From the mode 3, voltage stress of the power MOSFETs can be expressed as

$$V_{DS1} = V_{DS2} = \frac{V_{in}}{1-D} = \frac{V_{out}}{N(n+1)+2}. \tag{22}$$

The voltage stress across diodes are given by

$$V_{D1} = V_{D2} = \frac{2V_{out}}{N(n+1)+2}, \tag{23}$$

$$V_{D3} = V_{D4} = V_{out}\frac{2N(n+1)+1}{N(n+1)+2}. \tag{24}$$

Figure 5 shows the normalized voltage stress across the semiconductor devices. As seen, the voltage across MOSFETs is decreased when increasing the turns' ratio of the CI.

*3.3. Current Stress of the Components.* According to Figure 2 and the steady-state analysis, the current stresses of the MOSFETs and diodes are obtained as

$$i_{S1,rms} = i_{S2,rms} = I_{out}\frac{N(n+1)+2}{2(1-D)}\sqrt{2D-1+\frac{[2N(n+1)+1]^2(1-D)}{[N(n+1)+1]^2}}, \tag{25}$$

$$i_{D1,rms} = i_{D2,rms} = I_{out}\sqrt{\frac{N(n+1)+2}{6(1-D)}}, \tag{26}$$

$$i_{D3,rms} = i_{D4,rms} = \frac{I_{out}[N(n+1)+2]}{2(1-D)[N(n+1)+1]}\sqrt{\frac{(1-D)[2+3N(n+1)]}{3[N(n+1)+2]}}, \tag{27}$$

$$i_{C1,rms} = \sqrt{i_{D2,rms}{}^2 + i_{D3,rms}{}^2}. \tag{28}$$

From (26) and (27), the RMS currents through the capacitors $C_1$, $C_2$, and $C_O$ are derived as

$$i_{C2,rms} = \sqrt{i_{D1,rms}^{\ 2} + i_{D4,rms}^{\ 2}}, \tag{29}$$

$$i_{\mathrm{CO}} = \sqrt{i_{D3,\mathrm{rms}}^{\ 2} + i_{D4,\mathrm{rms}}^{\ 2} - I_{\mathrm{out}}^{\ 2}}. \tag{30}$$

Current $i_{LK1}$ ($i_{LK2}$) is equal to $I_{Lm1} - Ni_{C2,\mathrm{rms}}$ ($I_{Lm2} + Ni_{C2,\mathrm{rms}}$), so using (29), its RMS value can be expressed as

$$i_{Lk1,\mathrm{rms}} = i_{Lk2,\mathrm{rms}} = \sqrt{I_{Lm}^{\ 2} + N^2\left(i_{D_{1,\mathrm{rms}}}^{\ 2} + i_{D_{4,\mathrm{rms}}}^{\ 2}\right)}. \tag{31}$$

The RMS value of $i_{LKb}$ can be derived using (27) as below:

$$i_{LKb,\mathrm{rms}} = \sqrt{N^2 i_{D3,\mathrm{rms}}^{\ 2} + N^2 i_{D4,\mathrm{rms}}^{\ 2}}. \tag{32}$$

*3.4. Input Current Ripple.* The input current ripple of the proposed converter is given by

$$\Delta I_{in} = \frac{(2D-1)(1-D)}{[N(n+1)+2]} \times \frac{V_{\mathrm{out}}}{L_m f_S}. \tag{33}$$

The normalized input current ripple with the base value of $V_{\mathrm{out}}/L_m f_S$ is shown in Figure 6. As shown, the input current ripple is decreased by the turns' ratio of the BIT and CI.

*3.5. Efficiency Estimation.* Figure 7 shows the equivalent circuit of the proposed converter together with its parasitic resistances. In fact, the effects of ON-state resistances of MOSFETs and diodes, forward voltage drops of the diodes, switching losses, resistances of the windings of the magnetic devices, and equivalent series resistance (ESR) of the capacitors should be considered to calculate the efficiency.

Due to the ZCS turn-ON condition for MOSFETs, the total power losses in the MOSFETs relates to conduction losses and the switching losses during turning OFF:

$$P_{\mathrm{MOSFETs}} = r_{DS1} i_{\mathrm{S1,rms}}^{\ 2} + r_{DS2} i_{\mathrm{S2,rms}}^{\ 2} + \frac{f_S}{2}\left(V_{DS1} i_{S1}(t_6) t_{\mathrm{OFF1}} + V_{DS2} i_{S2}(t_1) t_{\mathrm{OFF2}}\right), \tag{34}$$

with $r_{DS1}$ and $r_{DS2}$ being the ON-state resistances of $S_1$ and $S_2$, respectively.

ON-state resistance ($r_D$) and forward voltage drop ($v_{FD}$) of the diodes can also contribute to power losses as below:

$$P_D = \sum_{i=1}^{4}\left(r_{Di} i_{Di,\mathrm{rms}}^{\ 2} + v_{F\,Di} i_{Di,\mathrm{Ave}}\right). \tag{35}$$

The windings' losses, including total CI and BIT losses, are given by

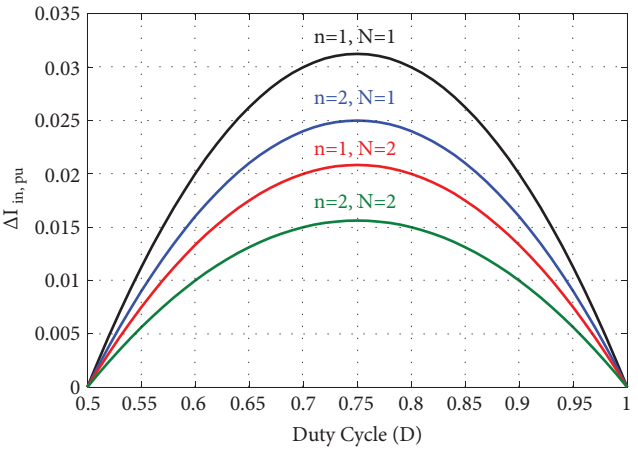


Figure 6: Normalized input current ripple.

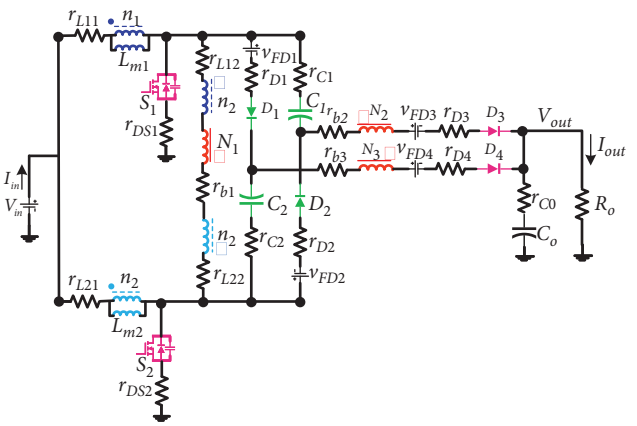


Figure 7: The equivalent circuit of the proposed converter considering the parasitic resistances.

$$P_{\mathrm{Wire}} = \left[r_{L11} i_{LK1,\mathrm{rms}}^{\ 2} + r_{L12} i_{LKb,\mathrm{rms}}^{\ 2} + r_{L21} i_{LLK2,\mathrm{rms}}^{\ 2} + r_{L22} i_{LKb,\mathrm{rms}}^{\ 2}\right]^{CI} + \left[r_{b1} i_{LKb,\mathrm{rms}}^{\ 2} + r_{b2} i_{D3,\mathrm{rms}}^{\ 2} + r_{b3} i_{D4,\mathrm{rms}}^{\ 2}\right]^{\mathrm{BIT}}. \tag{36}$$

The power losses related to equivalent series resistance (ESR) of the capacitors can be written as

$$P_C = r_{C1} i_{C1,\mathrm{rms}}^{\ 2} + r_{C2} i_{C2,\mathrm{rms}}^{\ 2} + r_{\mathrm{CO}} i_{\mathrm{CO,rms}}^{\ 2}. \tag{37}$$

The core losses are given by

$$P_{\mathrm{core}} = A f_S^{\alpha} B^{\beta} V_e, \tag{38}$$

where $V_e$ is the volume of core, $B$ is maximum flux density, $A$, $\alpha$, and $\beta$ are the Steinmetz parameters given in datasheet of the selection core. The calculated core losses for each of the CIs are about 2.25 W, where it is about 1.5 W for the BIT. Therefore, the total dissipations of the cores is about 6 W.

Total power losses of the proposed converter can be written as

$$P_{\mathrm{Loss}} = P_{\mathrm{MOSFETs}} + P_D + P_C + P_{\mathrm{Wire}} + P_{\mathrm{core}}. \tag{39}$$

Table 1: Specifications of the proposed converter.

| Components | Parameters |
|---|---|
| Output power ($p_{out}$) | 600 W |
| Input-output voltages ($V_{in} - V_{out}$) | 27V–400 V |
| Switching frequency ($f_s$) | 50 kHZ |
| Power MOSFETs ($S_1$,$S_2$) | IPP076N12N3 |
| Clamp diodes ($D_1$,$D_2$) | MUR880 |
| Output diodes ($D_3$,$D_4$) | MUR1560 |
| Clamp capacitors ($C_1$,$C_2$) | $5\mu F$ |
| Output capacitor ($C_{out}$) | $5\mu F$ |
| Coupled inductor | Ferrite core EE55, $n = 1$, $L_m = 168\,\mu H$, and $n_1 = n_2 = 19$ turns |
| Built-in transformer | Ferrite core EE55, $N = 2$, $L_m = 800\,\mu H$, and $N_2 = N_3 = 2N_1 = 32$ turns |

Finally, the efficiency and the voltage gain of the proposed converter can be obtained as

$$\eta = \frac{P_{out}}{P_{out} + P_{Loss}}. \tag{40}$$

By calculating the RMS currents through the circuit components in Section 3.3, the power losses related to these components can be calculated. The components specifications of the fabricated prototype in Table 1 are assumed to be as

$$\begin{aligned} r_{DS1} &= r_{DS2} = 7.5m\Omega, \\ r_{C1} &= r_{C2} = 20m\Omega, \\ r_{CO} &= 100m\Omega, \\ r_{Di} &= 12m\Omega, \quad for\ i = \{1,2,3,4\}, \\ v_{FDj} &= 1.2V, \quad for\ j = \{1,2,3,4\}, \\ r_{L11} &= r_{L21} = 12m\Omega, \\ r_{L12} &= r_{L22} = r_{b1} = r_{b2} = r_{b3} = 24m\Omega. \end{aligned} \tag{41}$$

The conversion efficiency and the voltage gain of the proposed converter are plotted in Figure 8. As shown, at a given voltage gain, by implementing of higher turns' ratios, the duty ratio can be decreased.

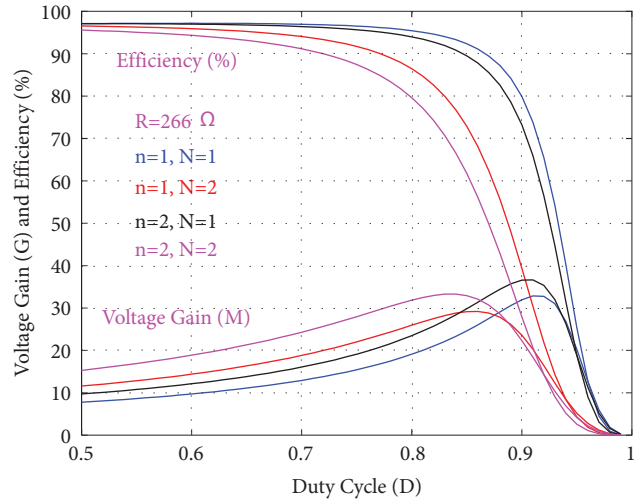


Figure 8: Voltage gain (M) and efficiency (%) of the proposed converter.

## 4. Performance Comparison

A performance comparison is made between the proposed converter and the previously presented interleaved converters in [28, 31, 35, 38–41, 43]. The results are provided in Table 2 and Figure 9. According to Figure 9(a), the voltage gain of the proposed converter with $n = N = 1$ is higher than the proposed converters in [38,43]. The presented converters in [28, 35] have higher voltage gain than the proposed converter; however, as shown in Table 2, these converters have more number of components than the proposed converter. Moreover, Figure 9(b) shows the voltage stress across semiconductor devices versus different turns' ratio. As can be seen, the proposed converter has resulted in the lowest voltage stress across power MOSFETs among all other converters for the turns' ratios more than 3. Moreover, as shown in Table 2, measured efficiency of the proposed converter is 94.6%. According to the output voltage 400 $V$, output power 600 $W$, and switching frequency 50 $kHz$, measured efficiency of the proposed converter is a reasonable and acceptable value. Furthermore, the voltage gain and the voltage stress across the semiconductors in the proposed converter can be controlled by the turns' ratio of the CI and BIT, making the design more flexible than its similar competitors.

## 5. Numerical Design

In this study, the circuit components are designed based on the following values:

$$\begin{aligned} V_{in} &= 27V, \\ V_{out} &= 400V, \\ f_S &= 50kHZ, \\ P_{out} &= 600W, \\ I_{in} &= 23.15A, \\ D &= 0.61\%. \end{aligned} \tag{42}$$

In addition, the turns' ratios of the CI and BIT are assumed to be $n = 1$ and $N = 2$, respectively.

*5.1. CI and BIT Design.* The magnetizing inductors of the CI are designed based on the input current ripple, which is considered 3% of input current:

Table 2: Performance comparison of the proposed converter.

| Converters | Techniques | $V_{out}/V_{in}$ | $V_{DS}/V_{out}$ | $V_D/V_{out}$ | Number of components $S^*/D^*/C^*/W^*/C^{**}/T^*$ | Measured efficiency |
|---|---|---|---|---|---|---|
| [28] | CI* + BIT* + VMC* | $(2Nn + 2N + 2/1 - D)$ | $(1/2Nn + 2N + 2)$ | $(2N(n+1) + 1/2[N(n+1)+1])$ | 2/6/3/7/5/23 | $\eta = 97\%$ $\begin{cases} V_{IN} = 28V, V_{OUT} = 400V \\ D = 60\%, f_S = 50kHz \\ P_{OUT} = 600W \end{cases}$ |
| [31] | CI* + VMC* | $(3N + 1/1 - D)$ | $(1/3N + 1)$ | $(2N/3N + 1)$ | 2/5/2/4/4/17 | $\eta = 97\%$ $\begin{cases} V_{IN} = 40V, V_{OUT} = 400V \\ D = 62\%, f_S = 50kHz \\ P_{OUT} = 400W \end{cases}$ |
| [35] | CI* + BIT* + SC* | $(4 + 4n + 2N/1 - D)$ | $(1/4 + 4n + 2N)$ | $(1 + 2n + N/2 + 2n + N)$ | 2/5/3/7/5/22 | $\eta = 95.53\%$ $\begin{cases} V_{IN} = 16V, V_{OUT} = 400V \\ D = 60\%, f_S = 50kHz \\ P_{OUT} = 200W \end{cases}$ |
| [38] | CI* + VMC* | $(n(1+D) + 2 - D/1 - D)$ | $(1/n(1+D) + 2 - D)$ | $(n + 1/n(1+D) + 2 - D)$ | 2/6/2/6/5/21 | $\eta = 92.6\%$ $\begin{cases} V_{IN} = 48V, V_{OUT} = 380V \\ D = 60\%, f_S = 50kHz \\ P_{OUT} = 2KW \end{cases}$ |
| [39] | CI* | $(2 + 2N/1 - D)$ | $(1/2 + 2N)$ | $(1 + 2N/2 + 2N)$ | 2/6/2/6/5/21 | $\eta = 94\%$ $\begin{cases} V_{IN} = 30V, V_{OUT} = 400V \\ D = 70\%, f_S = 50kHz \\ P_{OUT} = 500W \end{cases}$ |
| [40] | VMC* | $(2K^*/1 - D)$ | $(1/2K^*)$ | $(1/K^*)$ | 2/4/2/2/4/14 | $\eta = 96\%$ $\begin{cases} V_{IN} = 20V, V_{OUT} = 400V \\ D = 70\%, f_S = 50kHz \\ P_{OUT} = 200W \end{cases}$ |
| [41] | VMC* + CI* | $(2N + 2/1 - D)$ | $(1/2N + 2)$ | $(1/N + 1)$ | 2/7/2/4/7/22 | $\eta = 96.7\%$ $\begin{cases} V_{IN} = 32V, V_{OUT} = 800V \\ D = 68\%, f_S = 118kHz \\ P_{OUT} = 400W \end{cases}$ |
| [43] | BIT* | $(n + 2/1 - D)$ | $(1/n + 2)$ | 1 | 2/4/3/5/3/17 | $\eta = 94.7\%$ $\begin{cases} V_{IN} = 48V, V_{OUT} = 380V \\ D = 62\%, f_S = 50kHz \\ P_{OUT} = 3.5KW \end{cases}$ |
| Proposed | CI* + BIT* | $(N(n+1) + 2/1 - D)$ | $(1/N(n+1) + 2)$ | $(2N(n+1) + 1/N(n+1) + 2)$ | 2/4/3/7/3/19 | $\eta = 94.6\%$ $\begin{cases} V_{IN} = 27V, V_{OUT} = 400V \\ D = 61\%, f_S = 50kHz \\ P_{OUT} = 600W \end{cases}$ |

CI*, coupled inductor; BIT*, built-in transformer; VMC*, voltage multiplier cell; SC*, switched capacitor; K*, number of VMC; S*, switch; D*, diode; C*, core; W*, winding; C**, capacitor; T*, total.

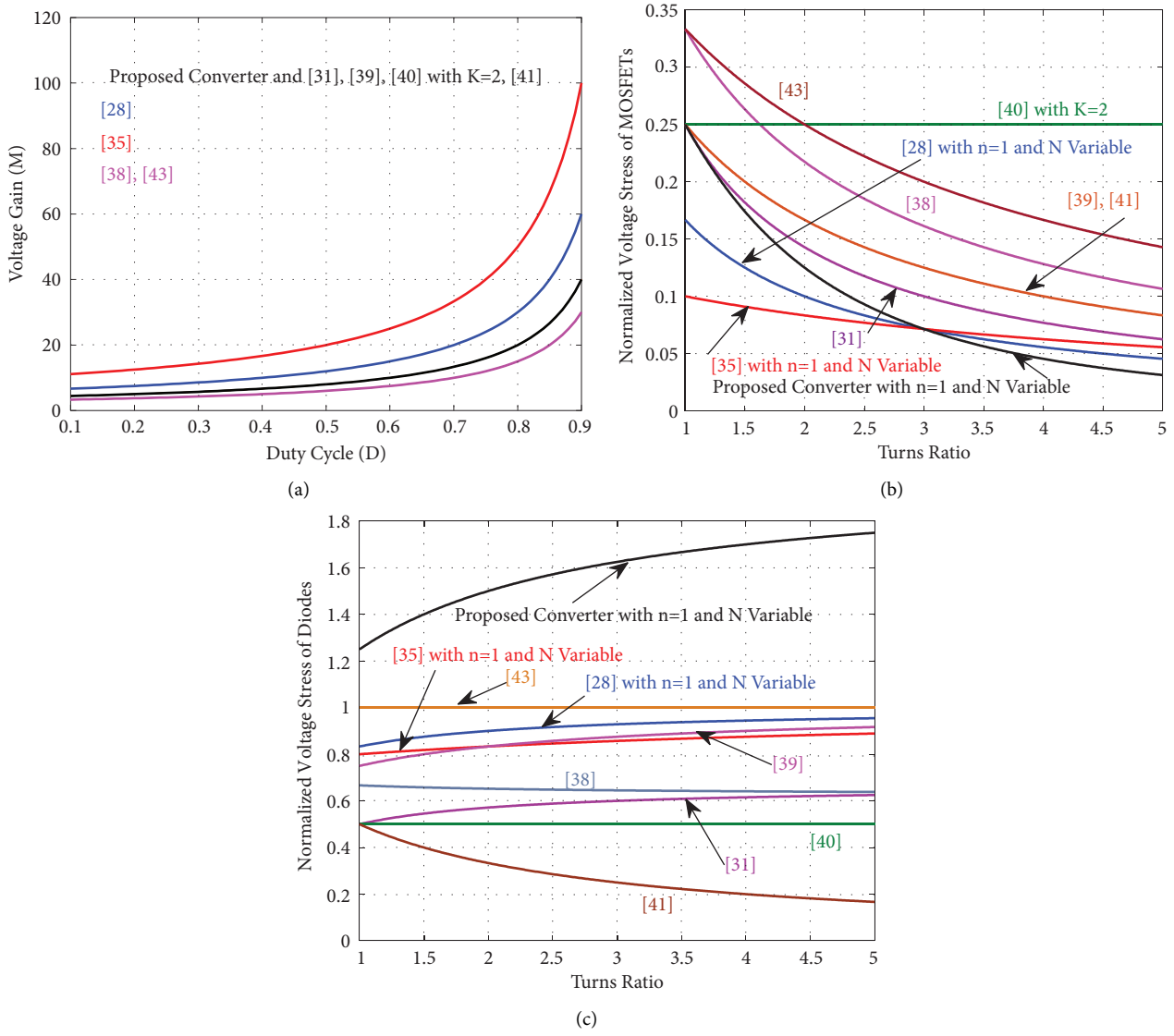


FIGURE 9: Performance comparison: (a) voltage gain, (b) normalized voltage stress across MOSFETs, and (c) normalized voltage stress across diodes.

$$L_{m1} = L_{m2} = \frac{(2D-1)(1-D)}{[N(n+1)+2]} \times \frac{V_{\text{out}}}{\Delta I_{\text{in}} f_S} = \frac{(2\times 0.61-1)\times(1-0.61)\times 400}{6\times 0.03\times 23.8\times 50000} = 160\mu H. \quad (43)$$

EE55 ferrite cores are chosen for CI. The cross-sectional area $A_C$ and the maximum flux density $B_{sat}$ are $354mm^2$ and $320mT$, respectively. $n_1$ is obtained as

$$n_1 = \frac{L_m I_{Lm,\text{Max}}}{B_{\text{Max}} A_C} = \frac{L_m\left(I_{Lm} + \left(DV_{\text{in}}/2L_m f_S\right)\right)}{B_{\text{Max}} A_C}. \quad (44)$$

The value of $n_1$ can be obtained as

$$n_1 = \frac{160\times 10^{-6}\times\left(11.53+\left(0.61\times 27/2\times 160\times 10^{-6}\times 50000\right)\right)}{300\times 10^{-3}\times 354\times 10^{-6}} = 18.9\text{Turns}, \quad (45)$$

where $B_{\text{MAX}} = 300mT$ is the maximum allowed swing of the flux density.

During mode 3, when $S_1$ is in ON-sate and $S_2$ is in OFF-state, the voltage across the primary winding of the BIT can be obtained as

$$V_{P,\text{Built-In Transformer}} = \frac{(n+1)V_{\text{in}}}{1-D} = N_1\frac{\Delta B A_C}{(1-D)T_s}. \quad (46)$$

EE55 ferrite cores are chosen for BIT. The cross-sectional area $A_C$ and the variation of the magnetic flux density $\Delta B$ are $354mm^2$ and $200mT$, respectively. $N_1$ is calculated by

$$N_1 = \frac{(n+1)V_{in}T_s}{\Delta B A_C} = \frac{2\times 27\times 2\times 10^{-5}}{200\times 10^{-3}\times 354\times 10^{-6}} = 15.25\text{Turns}. \quad (47)$$

*5.2. Design of Capacitors.* The capacitors are designed based on their voltage ripple $x$% (which can be extracted according

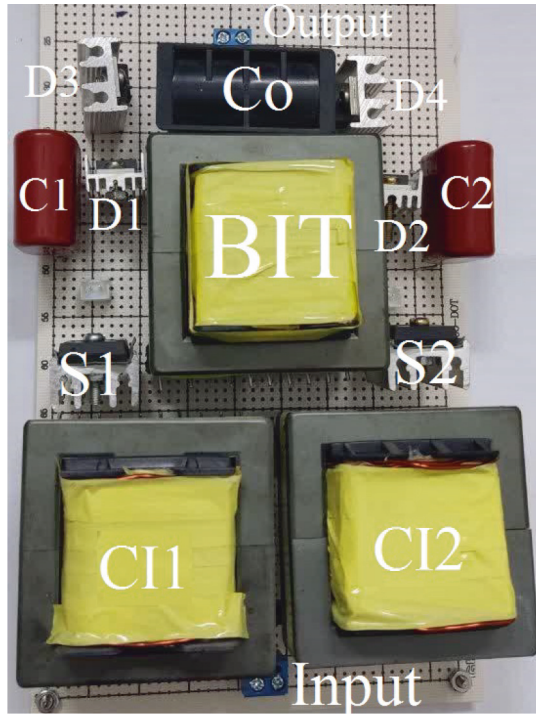


Figure 10: Photograph of the prototype.

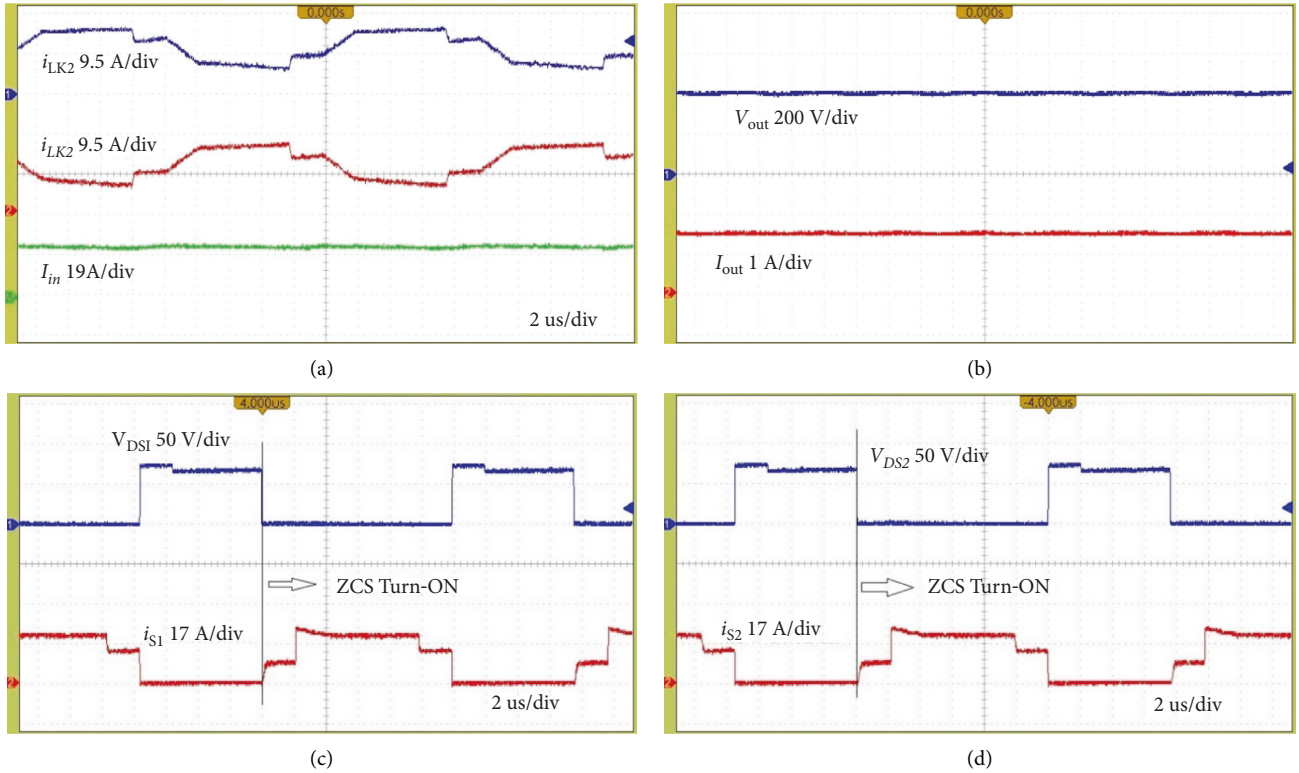


Figure 11: Experimental waveforms of (a) input current and the currents of the leakage inductances of the CI, (b) output voltage and output current, (c) the voltage stress and current of switch $S_1$, and (d) the voltage stress and current of switch $S_2$.

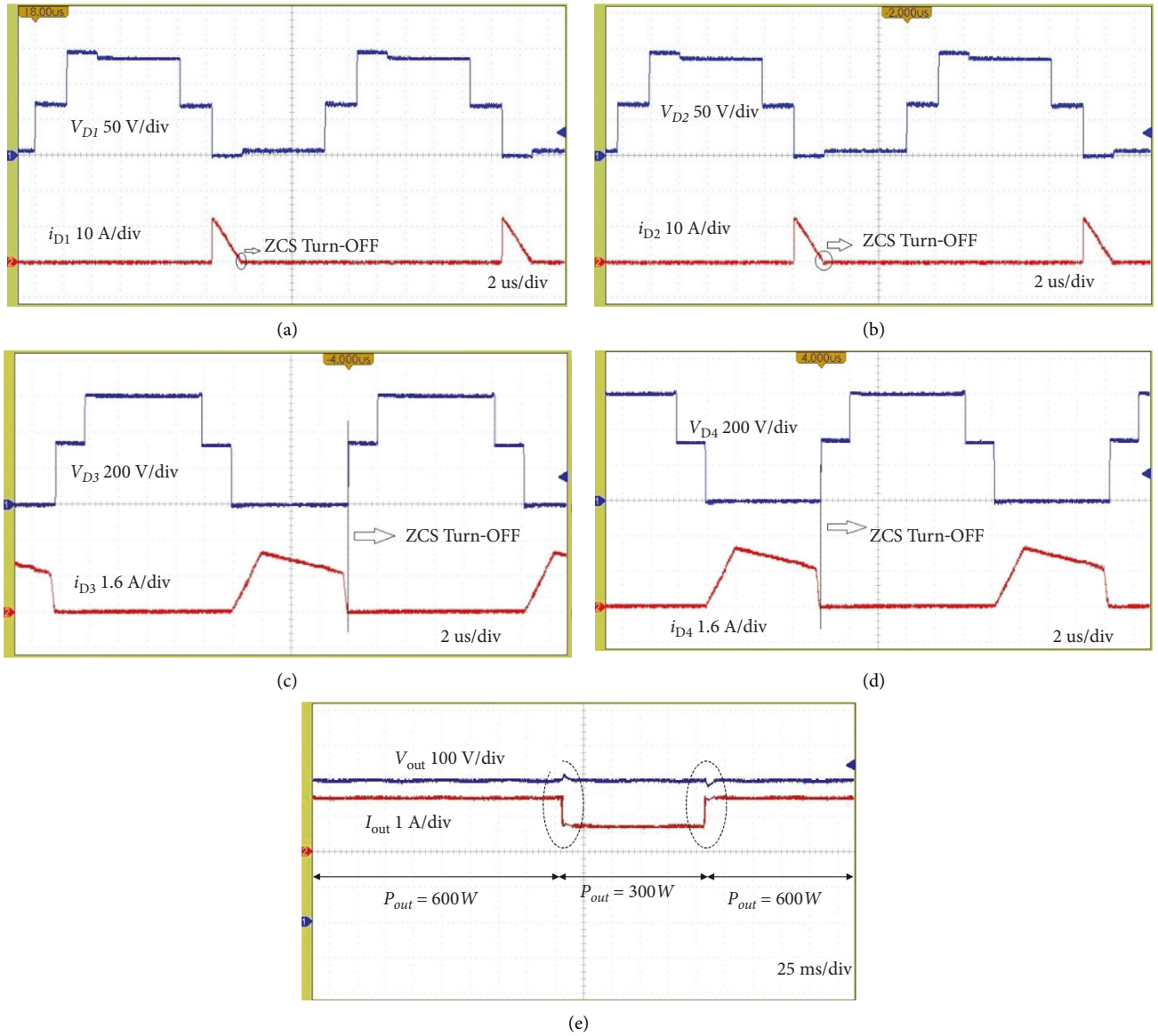


FIGURE. 12: Experimental waveforms of (a) the voltage stress and current of diode $D_1$, (b) the voltage stress and current of diode $D_2$, (c) the voltage stress and current of diode $D_3$, (d) the voltage stress and current of diode $D_4$ {R4-7}, and (e) dynamic response.

to section 3). The voltage across the capacitors $C_1 = C_2$ and $C_{out}$ are 69.2$V$ and 400$V$, respectively.

By assuming the voltage ripples as $x\%V_{C1,2} = 8\%V_{C1,2}$ and $x\%V_{\text{Cout}} = 3\%V_{\text{out}}$, the capacitors' values are obtained as follows:

$$C_1 = C_2 = \frac{P_{\text{out}}}{V_{\text{out}}\Delta V_C f_S} = \frac{P_{\text{out}}[N(n+1)+2]}{x\%{V_{\text{out}}}^2 f_S} = \frac{600 \times 6}{0.08 \times 400^2 \times 50000} = 5.6\mu F, \tag{48}$$

$$C_{\text{out}} = \frac{P_{\text{out}}}{V_{\text{out}}\Delta V_{\text{Cout}} f_S} = \frac{P_{\text{out}}}{x\%{V_{\text{out}}}^2 f_S} = \frac{600}{0.03 \times 400^2 \times 50000} = 2.5\mu F. \tag{49}$$

*5.3. Selection of Semiconductor Devices.* The semiconductor devices are selected according to their voltage stress and the currents flowing through them (the maximum and RMS values). Thus, (25)–(27) can be used to select appropriate semiconductor devices.

## 6. Experimental Verification

To validate the practical feasibility of the proposed topology a 600 W, 27 V input to 400 V output laboratory prototype with the specifications provided in Table 1 is fabricated. The photograph of the prototype is illustrated in Figure 10. The duty ratio is approximately 0.61. In Figure 11(a), the experimental results of the input current and the currents through the leakage inductances of the CI are shown. As shown in this figure, according to the symmetrical configuration, input current phases are equal and also the input

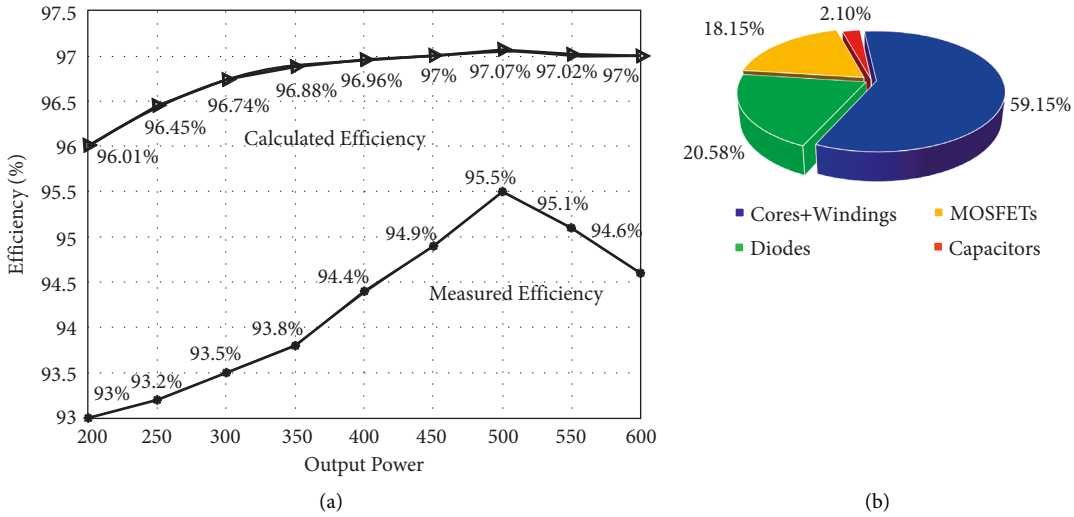


Figure 13: (a) Measured and calculated efficiency of the proposed converter; (b) pie graph of the losses distribution at full load.

current ripple is small. Therefore, due to the equal current sharing between two phases, the ripple cancellation is obtained. Figure 11(b) shows the output voltage and the output current. In Figure 11(c) and Figure 11(d), the experimental results of the voltage and current waveforms of the main switches $S_1$ and $S_2$ are illustrated. As can be observed, ZCS turn-on condition is provided for both switches. Figure 12(a) and Figure 12(b) show the experimental results of the voltage and current of clamp diodes $D_1$ and $D_2$. Also, Figure 12(c) and Figure 12(d) show the experimental results of the voltage and current of the output diodes $D_3$ and $D_4$. From the theoretical analysis in (23) and (24), the voltage stress of diodes are obtained $V_{D1} = V_{D2} = 133.3V$ and $V_{D3} = V_{D4} = 600V$. As it clearly shows, ZCS turn-off condition is achieved for all of diodes. So, the reverse recovery problem of the diodes is alleviated. Dynamic response is shown in Figure 12(e).

Measured and calculated efficiency curve of the proposed converter is illustrated in Figure 13(a). The maximum efficiency of 96.5% is occurred at 500 W. Measured efficiency under full-load condition (600 W) is 94.6% which is almost close to the calculated of 97%.

Figure 13(b) shows pie graph of the losses distribution at full load (600 W) which is 18.51 W. Power losses due to windings, cores, diodes, MOSFETs, and capacitors are 4.95 W, 6 W, 3.81 W, 3.36 W, and 0.39 W. It is seen the calculated and measured conversion efficiencies are almost close and confirm each other.

## 7. Conclusion

An interleaved high step-up converter topology based on the coupled inductor (CI) and built-in transformer (BIT) is proposed in this study. The proposed converter has the following features:

(1) By using BIT and CI, high voltage gain without extreme duty ratio is achieved.

(2) The proposed converter is much more flexible than the converters with only one of this magnetic means because of having an extra degree of freedom with simultaneous implementation.

(3) By increased turns' ratio of CI and BIT, the voltage stress across MOSFETs relatively is decreased which facilitates the utilization of low voltage-rated MOSFETs with low ON-state resistance.

(4) Due to the interleaved structure at the input of this converter, the input current ripple is minimized

(5) The leakage inductances of the BIT and CI provide turned-OFF and turned-ON ZCS conditions for all the diodes and power MOSFETs, respectively.

(6) The energy of the leakage inductances is recycled by the clamp capacitors avoiding high spikes across MOSFETs. Moreover, the reverse recovery problem of the diodes is attenuated due to the leakage inductances of CI.

It is worth noting that the voltage stress across output diodes is higher than the output voltage which is the main advantage of the proposed converter. Finally, a laboratory prototype with 27 V–400 V voltage conversion with the conversion efficiency of 94.6% at full load (600 W) has been implemented and tested to demonstrate performance of the proposed converter. As a result, the proposed converter is suitable for renewable energy system applications.

## Abbreviations

ZCS: Zero current switching
$D$: Duty ratio
$M$: Voltage gain
$n$: Turns' ratio between $n_1$ and $n_2$
$N$: Turns ratio between $N_1$ and $N_2$ and $N_1$ and $N_3$
$\mu F$: Micro-Farad
$\mu H$: Micro-Henry

$L_M$: Magnetizing inductance
$W$: Watt
$A$: Ampere
$V$: Volt
$L_{LK}$: Leakage inductance
$i_{LM}$: Current of magnetic inductance
$KHz$: Kilohertz
$PV$: Photovoltaic system.

## Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

## Conflicts of Interest

The authors declare that they have no conflicts of interest.

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