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Research Article

A High Gain Two-Winding Switched Coupled-Inductor Network

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Summary. This paper proposes a new high-gain quasi-Z-source network (qZSN) with a switched-coupled-inductor (SCL). By employing a two-winding SCL within the impedance network, the proposed topology offers high voltage gains with relatively low shoot-through current and low total voltage stress on switching devices. Other prominent features of the proposed topology can be mentioned as low total voltage stress on the switching devices, continuous dc-input current, and common ground among the input dc-voltage source and the load-side. In addition, the proposed qZSN has a low peak magnetizing current which allows using a smaller size magnetic core for the coupled-inductor. Reduced passive components count along with lower switch current stress lead to lower power losses and converter costs. The superiority of the proposed impedance network is confirmed by comparing its main properties with other successful existing ZS-based topologies. The detailed theoretical analysis and performance principles of the proposed qZSN are validated through experimental results.

1. Introduction

Power electronics converters with boost voltage ability are widely used in many power conversion applications at various voltage and power levels. The increasing demand for reliable, efficient, and high power density step-up converters has been addressed to some extent by using the flyback, forward, push-pull, half-bridge, and full-bridge converters, as well as the second-, third-, and fourth-order boost converters [1, 2]. The Z-source network (ZSN) concept is an effective solution in realizing power electronics converters used in renewable power generation systems, adjustable speed drives, electric vehicles (EVs), etc., in which providing a wide range of voltage gains is the major challenge [3–9]. By inserting the shoot-through intervals into the traditional switching states, Z-source converter (ZSC) offers several advantages such as producing a wide range of output voltages regardless of the input voltage, high reliability, more immunity to EMI noises, and also reducing the output waveform distortion due to the elimination of dead time in the switching pattern. However, the conventional ZSC has some serious shortcomings including relatively low voltage gain, discontinuous dc-input current, and lack of common ground between the input source and the output side [10–12]. Many techniques have been already presented to enhance the boost capability of the ZSNs and improve their performance such as switched-inductors (SL) [13–16], switched-capacitors (SC) [17, 18], cascading techniques including diode-assisted (DA) and capacitor-assisted (CA) [17, 19–21], the combination of active-switched-capacitors and switched-inductors (ASC/SL) [19] and tapped-inductor (TL) [20]. However, all these approaches require a large number of passive/active components and high-rating semiconductor devices, leading to drawbacks such as high cost, large size, and low efficiency. Another approach commonly used to obtain very high voltage gains is to employ coupled-inductors or transformers in the impedance network. Trans-Z-source [21], TZ-source [22], improved trans-Z-source [23], LCCT-quasi-Z-source [24], Γ-Source [25], extended trans-Z-source [26], Y-source [27], quasi-Y-source [28], and Δ-source [29] are some successful coupled-inductors-based topologies which have been gradually reported in recent years. Comparatively, these ZSNs usually use a smaller duty ratio and less number of

passive components to produce the desired voltage gain. However, to obtain higher voltage boost factors, the turn ratio must be increased, which requires more isolation between the windings. Increasing the number of turns and enhancement of isolation between the windings not only increases the magnetic core size and imposes more complexity to coupled-inductors design, but also increase the leakage inductances. Large leakage inductances cause large di/dt, which eventually leads to large voltage spikes across the switching devices. Consequently, the lower winding turn ratios not only simplify the coupled-inductor implementation and decrease the overall size, weight, and cost of the converter but also significantly improve the converter performance. The integration of the boosting techniques with the coupled-inductors is the most recent attempt to obtain high voltage gains with smaller turn ratios [30–34]. In [31], by integrating a three-winding switched-coupled-inductor (SCL) and a switched-capacitor into the traditional quasi-Z-source network (qZSN), the boost ability is significantly enhanced. Two coupled-inductors-based ZSNs have been presented in [33] which can offer high voltage gains with less-than-unity turn ratios. As a modification to the structures in [33], the modified series and tapped switched-coupled-inductors quasi-Z-source networks (mSSCL-qZSN and mTSCL-qZSN) have been recently introduced which not only offer significant high voltage gains but also provide a continuous input current and a common ground point among the input and output sides [34]. Nevertheless, high windings loss of the coupled-inductors is a major drawback of these schemes, which is due to the high currents through the coupled-windings during the shoot-through state. In addition to the difficulties associated with designing and implementing the three-winding coupled-inductors with low leakage inductances, the three-winding SCL-based ZSNs have substantially high shoot-through current stress. The high switch current stress along with high number of passive components potentially increase the power loss, cost and volume of these converters.

With the aim being to alleviate the major drawbacks of the previous coupled-inductors-based ZSNs, this study proposes an impedance network called high gain tapped switched-coupled-inductors quasi-Z-source network (TSCL -qZSN), which incorporates a combination of the SC technique and a tapped two-winding SCL into a qZSN. While retaining all excellent features of the earlier mentioned SCL-based ZSNs, the proposed topology offers a remarkably high voltage gain with short shoot-through durations. The smaller voltage stress on devices makes it possible to use lower voltage rating components in the proposed impedance network. Furthermore, the efficiency of the proposed TSCL-qZSN is considerably improved due to lower shoot-through current stress, as well as employing less number of components in the impedance network. Based on the defined criteria introduced in [29, 35], it has been proved that the proposed qZSN has lower windings losses of the coupled-inductors compared to its other SCL-based counterparts mainly due to the reduced number of turns in the coupled-inductors. Continuous and smooth input current and common ground between the input source and the output side are other advantages of the proposed TSCL-qZSN. The theoretical analysis and comparison with some well-known and successful ZS-based topologies in terms of the boost ability, the rating, sizing and number of the impedance network components, the total voltage stress, the shoot-through current and the efficiency reveal the prominent advantages of the proposed TSCL-qZSN. The theoretical analysis is also verified through experimental implementation of a DC-DC prototype converter.

2. Proposed Topology

Figure 1 shows the structure of the proposed TSCL-qZSN, including a two-winding SCL, two diodes, three capacitors, and one discrete inductor. Similar to other Z-source-based topologies, the operation principle of the proposed qZSN will be extensively discussed into shoot-through (ST) and non-shoot-through (NST) states in this section. For the sake of simplicity, the load side is modeled by an equivalent current source and an ideal switch connected in parallel.

2.1. Shoot-Through State. The equivalent circuit of the proposed network during the shoot-through state is shown in Figure 2(a), where the switch SW is turned on. The magnetizing inductance (L_m) and the leakage inductances of two windings (L_{l1} and L_{l2}) are indicated in this equivalent circuit. The coupling coefficient of the coupled-inductor can be defined as $k = \sqrt{L_m/(L_m + L_l)}$, where L_l is the total leakage inductance referred to the primary winding. In the shoot-through state, the input diode D_1 is reverse-biased and therefore, the capacitor C_1 charges the tapped two-winding SCL, which subsequently increases the currents through windings N_1 and N_2. Also, the capacitor C_3 absorbs energy from the capacitor C_1 through the diode D_2 and the winding N_2. Defining $\alpha = (1 - k^2)/k^2$, and $n = N_2/N_1$ as the turn ratio of the two-winding coupled-inductors, the following steady-state equations can be obtained:

$$V_{\text{Lin}} = V_{\text{in}} + V_{C2}, \tag{1}$$

$$V_{C3} = V_{N2(ST)} = nV_{N1(ST)}, \tag{2}$$

$$(n+1)V_{N1(ST)} + V_{Ll} = V_{C1} \longrightarrow V_{N1(ST)} = \frac{1}{n+1+\alpha}V_{C1}. \tag{3}$$

From (2) and (3), the voltage across the capacitor C_3 can be obtained in terms of VC1 as follows:

$$V_{C3} = \frac{n}{n+1+\alpha}V_{C1}. \tag{4}$$

It should be noted that the capacitors C_1, C_2, and C_3 are sufficiently large to maintain their volatges approximately constant.

2.2. Non-Shoot-Through State. Figure 2(b) shows the equivalent circuit of the proposed TSCL-qZSN during the non-shoot-through state, where the output switch is turned

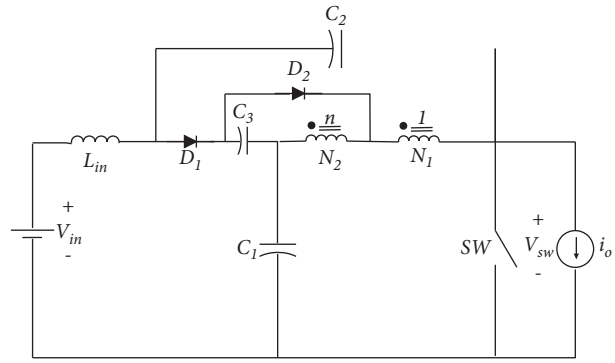

Figure 1: Proposed high gain tapped switched-coupled-inductors quasi-Z-source network (TSCL-qZSN).

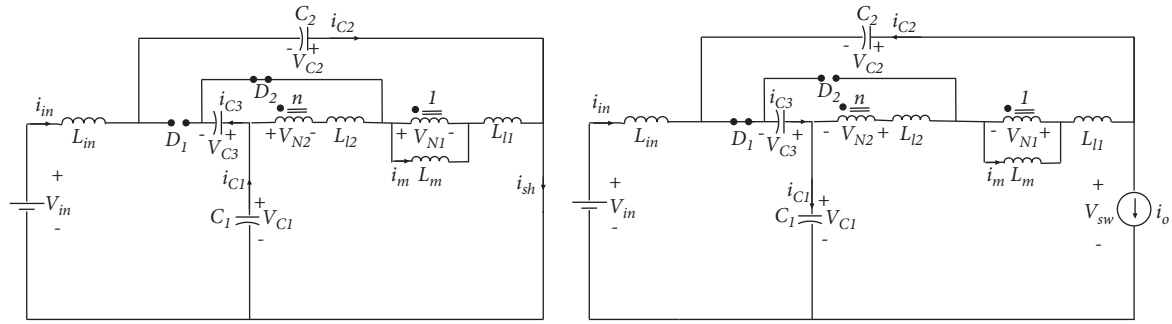

Figure 2: Equivalent circuit of the proposed TSCL-qZSN during (a) shoot-through state and (b) non-shoot-through state.

off and the load-side is represented by the equivalent current source. In this state, the input diode D1 is ON, while diode D2 is reverse-biased. The capacitors C1 and C2 are charged by the input dc-voltage source and the capacitor C3 transfers its stored energy to the load through the windings N1 and N2. Also, the energy stored in the leakage inductances is discharged into the capacitor C2. As a result, the large di/dt created by switching of the windings currents can be effectively suppressed, which results in much lower switching voltage spikes. By applying KVL to the equivalent circuit of the proposed impedance network in the non-shoot-through state, we can obtain the equations as follows:

$$V_{\text{Lin}} = V_{\text{in}} + V_{C3} - V_{C1}, \tag{5}$$

$$V_{N1(\text{NST})} = \frac{1}{n+1+\alpha}\left(V_{C3} - V_{C2}\right). \tag{6}$$

Substituting (4) into (5) and (6) gives

$$V_{\text{Lin}} = V_{\text{in}} - \frac{1}{n+1+\alpha}V_{C1}, \tag{7}$$

$$V_{N1(\text{NST})} = \frac{1}{n+1+\alpha}\left(\frac{n}{n+1+\alpha}V_{C1} - V_{C2}\right). \tag{8}$$

By applying the voltage-second balance on the voltage of the winding N1 over one switching cycle Tsw, VC2 can be related to VC1 as follows:

$$V_{C2} = \frac{n+(1+\alpha)D_{sh}}{(n+1+\alpha)\left(1-D_{sh}\right)}V_{C1}, \tag{9}$$

where Dsh is the shoot-through duty ratio. Similarly, applying the voltage-second balance principle to the voltage across the input inductor Lin from (1) and (7), gives the equation as follows:

$$V_{C1} = \frac{(n+1+\alpha)\left(1-D_{sh}\right)}{1+\alpha-(n+2+2\alpha)D_{sh}}V_{\text{in}}. \tag{10}$$

Finally, the voltage across the switch during the non-shoot-through state can be obtained as follows:

$$V_{sw} = V_{C1} - V_{C3} + V_{C2} = \frac{(n+1+\alpha)}{1+\alpha-(n+2+2\alpha)D_{sh}}V_{\text{in}}. \tag{11}$$

Therefore, the voltage gain of the proposed TSCL-qZSN can be defined as follows:

$$G = \frac{V_{sw}}{V_{\text{in}}} = \frac{(n+1+\alpha)}{1+\alpha-(n+2+2\alpha)D_{sh}}. \tag{12}$$

Figure 3 shows the variations of the voltage gain versus the shoot-through duty ratio and α coefficient. It can be seen that the voltage gain is decreased by increasingα coefficient. Consequently, the leakage inductances of the coupled-inductor decrease the practical voltage gain of the proposed qZSN.

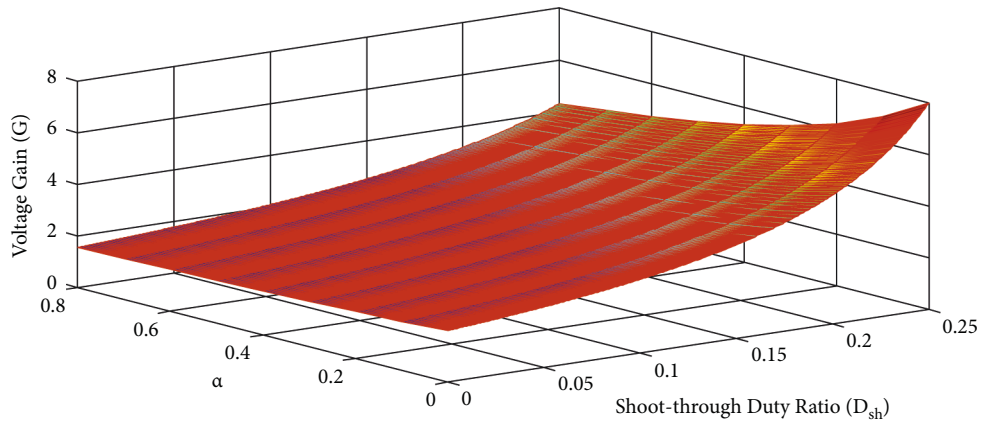

Figure 3: Variations of the voltage gain (G) versus the shoot-through duty ratio (D_{sh}) and α coefficient.

Assuming the unity coupling coefficient and subsequently $\alpha = 0$, the steady-state equations (4), (9), (10), and (12) can be rewritten as follows:

$$V_{C3} = \frac{n}{n+1}V_{C1}, \tag{13}$$

$$V_{C2} = \frac{n + D_{sh}}{(n+1)(1 - D_{sh})}V_{C1}, \tag{14}$$

$$V_{C1} = \frac{(n+1)(1 - D_{sh})}{1 - (n+2)D_{sh}}V_{\text{in}}, \tag{15}$$

$$LptG = \frac{(n+1)}{1 - (n+2)D_{sh}}. \tag{16}$$

Figure 4 compares the voltage gain of the proposed TSCL-qZSN with that of some successful Z-source-based topologies, which have been introduced in recent years. For a fair comparison, the total winding-cell inductance (L_{tot}) should be assumed to be equal for the proposed qZSN and the three-winding SCL-qZSN introduced in [31]. Therefore, by assuming the same magnetizing inductance Lm for both topologies and ignoring the leakage inductances of the coupled inductors, the following equation can be obtained:

$$\left(1 + n_{TSCL}^2\right)L_m = \left(2 + n_{SCL}^2\right)L_m \Rightarrow n_{TSCL} = \sqrt{1 + n_{SCL}^2}. \tag{17}$$

It can be readily observed that for the same turn ratio and shoot-through duty ratio, the proposed impedance network offers a significantly higher voltage gain compared to most networks. It should be noted that although the three-winding SCL-qZSN and mSSCL-qZSN can provide higher voltage gains compared to the proposed topology, they require a higher number of passive components in the impedance network which consequently leads to higher cost and volume and also lower efficiency, as will be discussed later in detail.

3. Theoretical Analysis and Comparison

In this section, the performance of the proposed TSCL-qZSN is evaluated in detail in terms of the magnetizing current, magnetizing inductance, the experienced total voltage stress by the semiconductor devices, and the shoot-through current and the efficiency. For the sake of better investigation, the obtained results are compared with those of other studied topologies.

3.1. Magnetizing Current and Core Size. The magnetizing current (I_m) is one of the most important parameters that need to be precisely determined in the design process of the coupled-inductors. As shown in Figures 2(a) and 2(b), the magnetizing current is measured from the primary winding (N_1). Considering the current of the capacitor C_2 in the shoot-through and non-shoot-through states gives the following equations:

$$i_{C2(ST)} = -I_{\text{in}}, \tag{18}$$

$$i_{C2(NST)} = i_{N1(NST)} - i_o = \frac{I_m}{n+1} - \frac{1 - (n+2)D_{sh}}{(1 - D_{sh})(n+1)}I_{\text{in}}, \tag{19}$$

where I_{in} and I_m are the average values of the input current and the magnetizing current, respectively. By applying the ampere-second balance principle to the above equations, the magnetizing current can be obtained as

$$I_m = I_{\text{in}}. \tag{20}$$

From (20), it can be concluded that for any turn ratio, the current-handling requirement of the two-winding SCL is equal to the input dc-current. A similar result can be obtained for the three-winding SCL-qZSN [31].

The magnetic core size of the coupled-inductors is generally determined based on the maximum stored energy in the core. The maximum energy in a magnetic core is directly related to the square of the peak magnetizing current, which can be expressed in terms of the average and the peak-to-peak ripple values of the magnetizing current as follows [29]

$$W_{\text{Core(max)}} \propto i_{m(\max)}^2 = \left(I_m + \frac{\Delta i_m}{2}\right)^2. \tag{21}$$

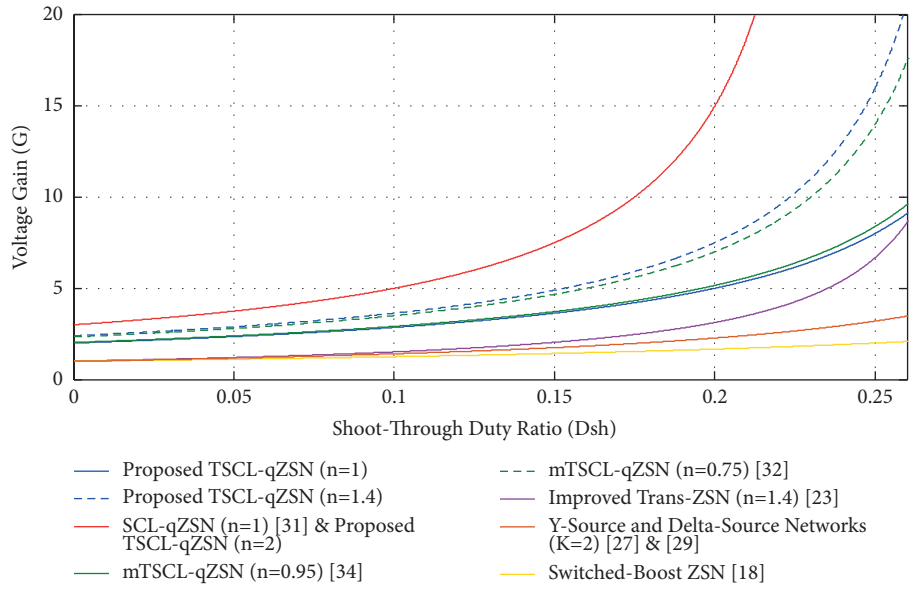

Figure 4: Voltage gain (G) versus the shoot-through duty ratio (D_{sh}).

Since the maximum energy is stored in the core during the shoot-through interval, the following equation is used to calculate the maximum ripple of the magnetizing current.

$$V_{N1(ST)} = L_m \frac{\Delta i_m}{D_{sh} T_{sw}} \Rightarrow \Delta i_m = \frac{V_{N1(ST)} D_{sh} T_{sw}}{L_m}, \tag{22}$$

where $V_{N1(ST)}$ and T_{sw} are the voltage across the winding N_1 during the shoot-through state and the switching time period, respectively.

From (3), (15), and (16) and with assuming $\alpha = 0$, the above equation can be rewritten as

$$\Delta i_m = \frac{(G+1)(G-(n+1))}{G(n+2)^2} \frac{V_{\text{in}}}{f_{sw} L_m}, \tag{23}$$

where V_{in} and f_{sw} are the input dc-voltage and the switching frequency, respectively. By substituting (20) and (23) into (21), the peak magnetizing current for the proposed TSCL-qZSN can be obtained as follows:

$$i_{m(\max)} = I_{\text{in}} + \frac{(G+1)(G-2-n)}{2(3+n)^2 G} i^b_{m(\max)}, \tag{24}$$

where $i^b_{m(\max)} = V^2_{\text{in}} / f_{sw} L_m P_o$ In this equation, P_o is the rated output power of the converter.

Figure 5 compares the square of the peak magnetizing current ($i^2_{m(\max)}$) for all of the coupled-inductors-based networks under consideration for a given operating point. The operating point specifications are as follows: $V_{in} = 40$V, $P_o = 200$W and $f_{sw} = 30$kHz. In this comparison, a magnetizing inductance of $L_m = 150\mu$H is assumed for all Z-source-based topologies. Obviously, for the same output voltage gain and turn ratio, the stored energy in the magnetic core and subsequently the required core volume is much smaller for the proposed impedance network compared to all two-winding coupled-inductors-based topologies, as well as Δ-source network. Although the SCL-qZSN and the mSSCL-qZSN have lower $i^2_{m(\max)}$, it is difficult to practically implement a three-winding coupled-inductors with low leakage inductance. This issue with the three-winding SCL-based ZSNs leads to large voltage spikes across the switching devices. Moreover, large leakage inductances of the coupled-inductors decrease the voltage gain of the converter through reducing the effective shoot-through durations [29]. From Figure 5, it can be also concluded that the proposed network and the mTSCL-qZSN presented in [34] require an almost same core volume for the coupled-inductors in the turn ratios of $n = 1$ and$n = 0.95$, respectively.

3.2. Magnetizing Inductance. The magnetizing inductance of the coupled-inductors is determined according to the magnetizing current ripple during the shoot-through interval. By following the same approach for the calculation of the magnetizing current, if the maximum ripple of I_m in the shoot-through state is limited to β%, the magnetizing inductance can be obtained as

$$L_m = \frac{V_{N1(ST)} D_{sh} T_{sw}}{\beta\% I_m}. \tag{25}$$

From (3) and (20), the magnetizing inductance can be calculated in terms of the output voltage gain and the turn ratio by the following equation:

$$L_m = \frac{(G+1)(G-1-n)}{G(2+n)^2} \frac{V^2_{\text{in}}}{\beta\% f_{sw} P_o} = \frac{(G+1)(G-1-n)}{G(2+n)^2} L^b_m. \tag{26}$$

The normalized required magnetizing inductance is plotted for each coupled-inductors-based network as a function of the voltage gain in Figure 6, based on the equations given in Table 1. As shown in Figure 6, compared

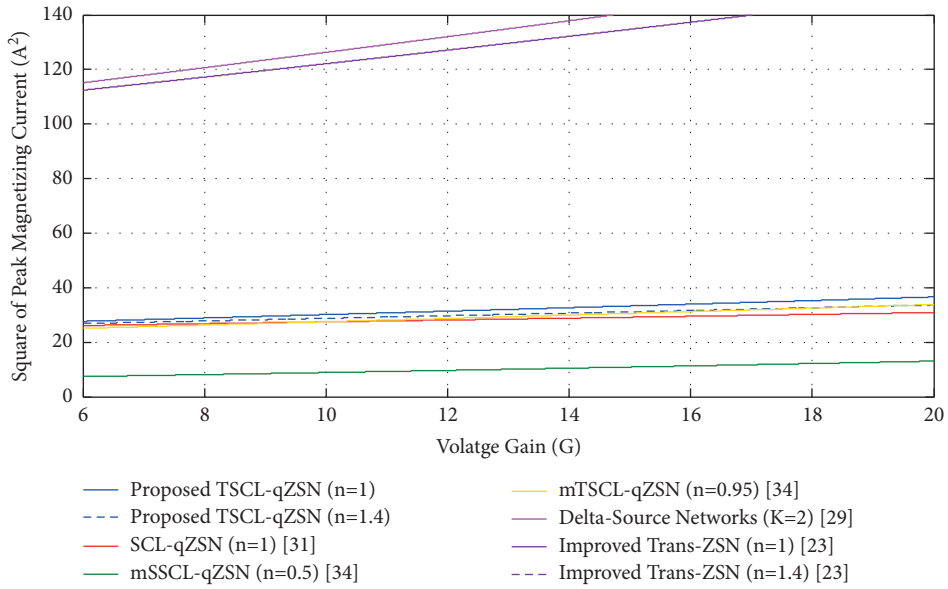

Figure 5: Square of the peak magnetizing current versus voltage gain.

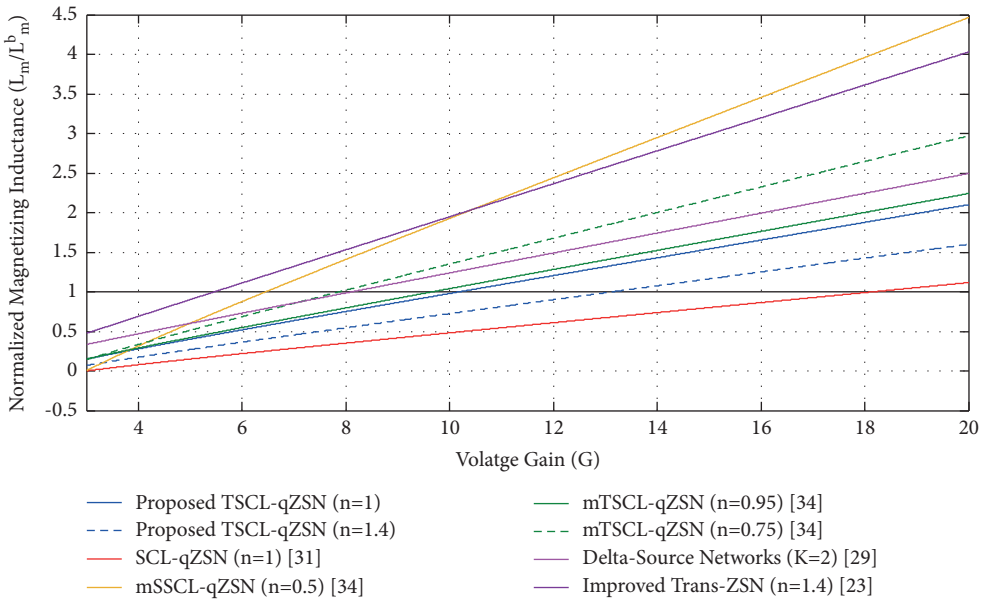

Figure 6: Normalized magnetizing inductance versus voltage gain.

to most the studied topologies, the proposed TSCL-qZSN requires a relatively low magnetizing inductance at a specific voltage gain, resulting in smaller coupled inductors.

3.3. Voltage and Current Stresses. The voltage stress on the load-side switch (V_{sw}) is equal to the peak output voltage of the impedance network, which for the proposed TSCL-qZSN can be expressed as follows:

$$V_{sw} = \frac{(n+1)}{1-(n+2)D_{sh}} V_{\text{in}} = GV_{\text{in}}. \tag{27}$$

Also, the voltage stresses across the diodes of the proposed impedance network can be obtained as in the following equations:

$$V_{D1} = \frac{(n+1)}{1-(n+2)D_{sh}} V_{\text{in}} = GV_{\text{in}},$$
$$V_{D2} = \frac{nG}{(n+1)} V_{\text{in}}. \tag{28}$$

In order to precisely compare the voltage stresses on the switching devices for different ZSN-based competitors, the total voltage stress for each of the topologies is obtained and

Table 1: Comparison of peak magnetizing current, magnetizing inductance, total voltage stress, and shoot-through current.

	Peak magnetizing current	Magnetizing inductance	Total voltage stress	Shoot-through current
Proposed TSCL-qZSN	$I_{in} + ((G+1)(G-1-n)/2(2+n)^2G)i^b_{m(\max)}$	$((G+1)(G-1-n)/(2+n)^2G)L^b_m$	$((2+3n)G/(1+n))V_{\text{in}}$	$((2+n)(G-1)/G-(1+n))I_{\text{in}}$
SCL-qZSN [31]	$I_{\text{in}} + ((G+1)(G-2-n)/2(3+n)^2G)i^b_{m(\max)}$	$((G+1)(G-2-n)/(3+n)^2G)L^b_m$	$(2(3+2n)G/(2+n))V_{\text{in}}$	$((3+n)(G-1)/G-(2+n))I_{\text{in}}$
mSSCL-qZSN [34]	$(1-n)I_{\text{in}} + ((G+1)(G-1-1/1-n)/2(1-n)(2+1/1-n)^2G)i^b_{m(\max)}$	$((G+1)(G-1-1/1-n)/(1-n)^2(2+1/1-n)^2G)L^b_m$	$(2(3-n)G/(2-n))V_{\text{in}}$	$((2+1/1-n)(G-1)/G-(1+1/1-n))I_{\text{in}}$
mTSCL-qZSN [34]	$nI_{\text{in}} + ((G+1)(G-1-1/n)/2n(2+1/n)^2G)i^b_{m(\max)}$	$((G+1)(G-1-1/n)/n^2(2+1/n)^2G)L^b_m$	$((2n+3)G/1+n)V_{\text{in}}$	$((2+1/n)(G-1)/G-(1+1/n))I_{\text{in}}$
Δ-Source network[a] [29]	$K_\Delta I_{\text{in}} + ((G-1)(G(K_\Delta-1)+1)/2K^2_\Delta G)i^b_{m(\max)}$	$((G-1)(G(K_\Delta-1)+1)/K^3_\Delta G)L^b_m$	$K_\Delta GV_{in}$	$(1+K_\Delta)I_{\text{in}}$
Y-source network[a] [27]	$(1/(1+N_1/N_3))I_{\text{in}} + (1/(1-N_2/N_3)),((G-1)(G(K_Y-1)+1)/2K^2_Y G)i^b_{m(\max)}$	$(1/(1+N_1/N_3))^2$, $((G-1)(G(K_Y-1)+1)/K^3_Y G)L^b_m$	$K_Y GV_{in}$	$K_Y I_{in}$
Improved trans-ZSN [23]	$(1+n)I_{\text{in}} + ((G-1)((n+1)G+1)/2G(2+n)^2)i^b_{m(\max)}$	$((G-1)((n+1)G+1)/(2+n)^2G)L^b_m$	$(2+n)GV_{\text{in}}$	$(2+n)I_{\text{in}}$
ASC/SCL-ZSN [19]	NA[b]	NA	$5GV_{in}$	$(3G+1/2G)I_{\text{in}}$
Switched-boost ZSN [18]	NA	NA	$(G+\sqrt{G(5G+4)})V_{\text{in}}$	$(G+\sqrt{G(5G+4)}/2G)I_{\text{in}}$

[a]The winding factors are defined as $K_\Delta = N_1/N_3$ and $K_Y = ((N_3+N_1)/(N_3-N_2))$ for Δ-source and Y-source networks, respectively. [b]NA: not applicable.

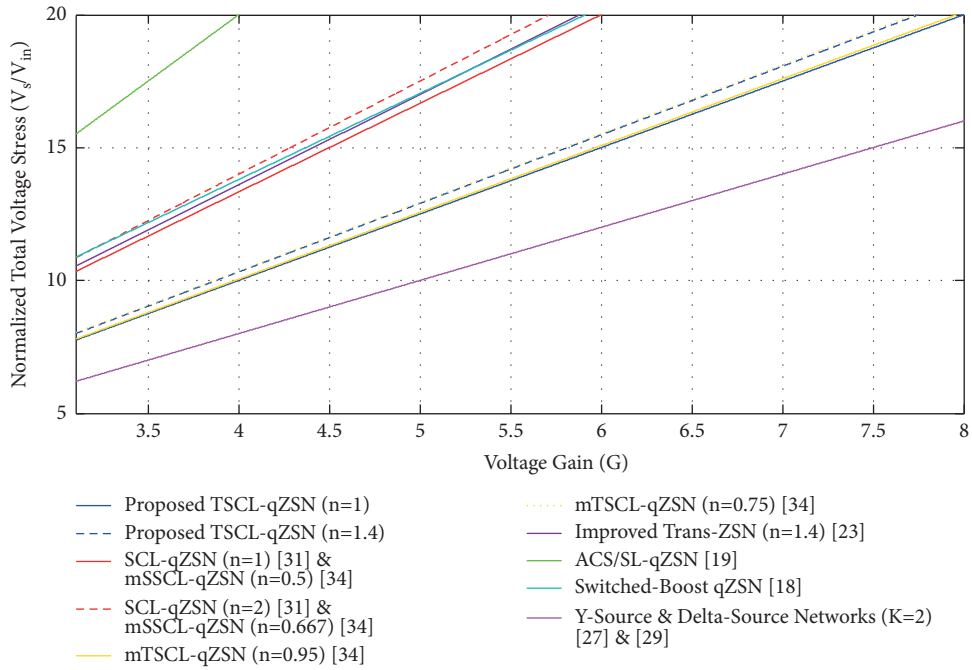

Figure 7: Normalized total voltage stress versus voltage gain.

listed in Table 1. The normalized total voltage stress of the proposed qZSN is compared with that of the other ZSNs in Figure 7. From this comparison, it is clear that even for the higher turn ratios, the total voltage stress across the switching semiconductors for the proposed qZSN is lower than that of most other networks, which allows using lower voltage rating switches and diodes. This can lead to lower switching losses and can also reduce the cost associated with the switching devices. The similar total voltage stress for the proposed qZSN and the mTSCL-qZSN can be concluded from Figure 7. It is worth mentioning since the Δ− source and Y-source structures employ only one diode in the impedance network, their total voltage stresses are lower compared to the proposed qZSN.

The shoot-through current (I_{sh}) is a key parameter in the selection of the output switches. High shoot-through current leads to higher switch losses and higher rating requirements for the active switches. Based on the parameters listed in Table 1, the normalized shoot-through current of the proposed TSCL-qZSN is plotted in Figure 8 and compared against that of the mTSCL-qZSN, mSSCL-qZSN, and SCL-qZSN, which show the most similar behavior to the proposed topology among other works. This figure verifies the superiority of the proposed qZSN in terms of the low shoot-through current operation. It can be clearly seen that the mSSCL-qZSN and SCL-qZSN have substantially higher shoot-through currents compared to the proposed topology, especially at low voltage gains.

3.4. Efficiency. In the impedance networks, the switches loss, the cores and windings losses of the inductors, and the conduction loss of the diodes are the main power losses. Among them, the switch loss and the inductors loss have the major contributions in the overall power loss. The output switch loss consists of the switching and conduction losses which can be approximated as [36]

$$P_{sw} = \frac{V_o I_{sh}}{2T_{sw}}\left(t_r + t_f\right), \tag{29}$$

$$P_{\text{con}} = I_{sh}^2 R_{on} D_{sh}. \tag{30}$$

In the above equations, I_{sh} is the shoot-through current of the proposed impedance network, R_{on} is the on-resistance of the semiconductor switch and t_r and t_f are the rise and fall times of the switch, respectively.

The normalized switching and conduction losses for the proposed qZSN and other SCL-based networks are plotted in Figure 9 which verifies the lower switch loss of the proposed TSCL-qZSN. In this regard, P_{sw}^b and P_{con}^b are defined as follows:

$$P_{sw}^b = P_o f_{sw}\left(t_r + t_f\right), \tag{31}$$

$$P_{\text{con}}^b = \frac{P_o^2}{V_{\text{in}}^2} R_{\text{on}}. \tag{32}$$

Ignoring the off-state blocking loss, the power dissipation of a diode can be calculated by the following equation [37, 38]

$$P_D = V_{T0} I_{F(ave)} + r_T I_{F(rms)}^2, \tag{33}$$

where r_T is the dynamic resistance which is determined from the diode characteristic, V_{T0} is the threshold voltage that corresponds to the voltage at the intersection of the r_T line and the V_F-axis in the V–I characteristic of the diode, and

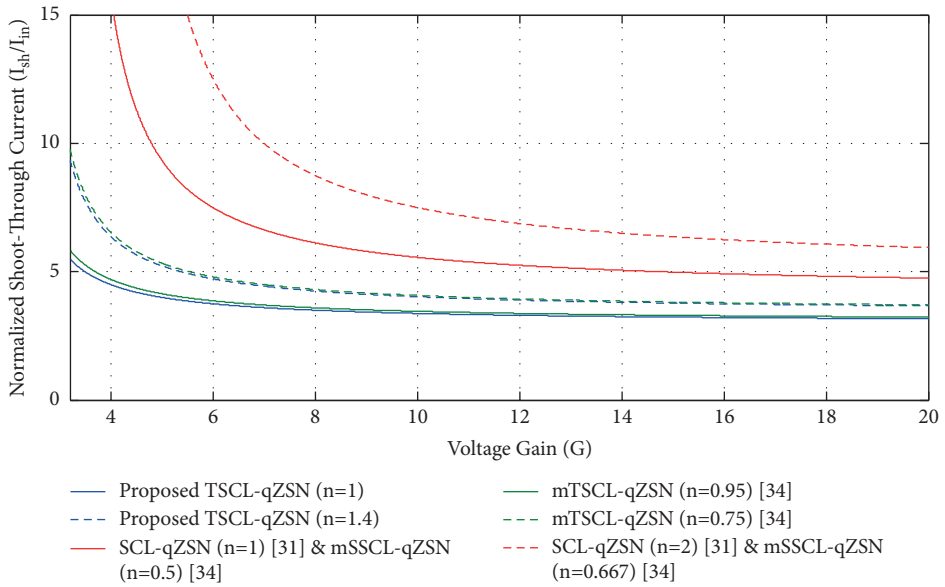

Figure 8: Normalized shoot-through current versus voltage gain.

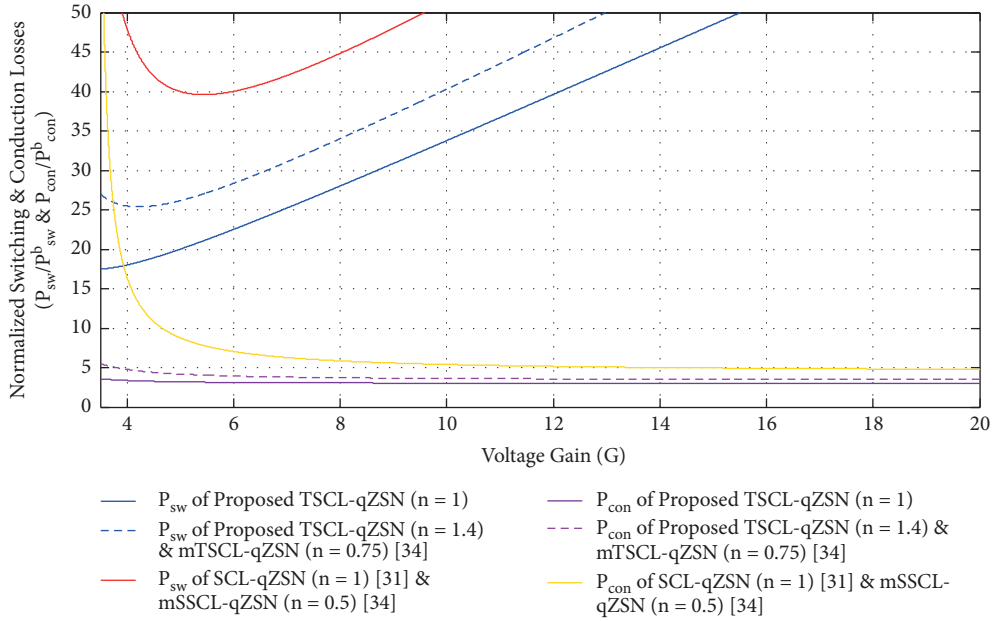

Figure 9: Normalized switching and conduction losses versus voltage gain.

$I_{F(ave)}$ and $I_{F(rms)}$ are the average and rms values of the diode current, respectively. $I_{F(rms)}$ can be calculated by $I_{F(rms)} = aI_{F(ave)}$, where a is the form factor, depending on the waveform of the diode current. Based on (33) and assuming all the diodes in the proposed impedance network are similar, the dissipated power by the diodes can be obtained as follows:

$$P_{D1} = I_{\text{in}}\left(V_{T0} + a_1{}^2 r_T I_{in}\right), \tag{34}$$

$$P_{D2} = I_{\text{in}}\left(V_{T0} + a_2^2 r_T I_{\text{in}}\right). \tag{35}$$

Therefore, according to (34) and (35), the total diode loss of the proposed TSCL-qZSN can be calculated as

$$P_{D(\text{loss})} = \sum_{i=1}^{2} P_{Di} = I_{\text{in}}\left(2V_{T_0} + \left(a_1^2 + a_2^2\right) r_T I_{\text{in}}\right). \tag{36}$$

An almost similar result can be obtained for the total power dissipation of the diodes in the mTSCL-qZSN, the SCL-qZSN, and the mSSCL-qZSN.

The winding and core losses of the coupled-inductors can be calculated using the method introduced in [23]. Due to the lower peak magnetizing current requirement of the

coupled-inductors in the proposed TSCL-qZSN, a smaller core size is needed to place the primary and secondary windings of the coupled-inductors. As a result, the mean length per turn (MLT) which is a function of the core size will be smaller in the proposed network. Additionally, for a given voltage gain and magnetizing inductance, the core loss of the coupled-inductors in the proposed topology will be lower compared to most other topologies. Furthermore, since the proposed impedance network needs a low magnetizing inductance for the two-winding coupled-inductors, the primary and secondary windings of the coupled-inductors will require a low number of turns. Therefore, to sum up, the coupled-inductors windings in the proposed TSCL-qZSN will have lower total resistance and subsequently lower ohmic loss compared to other coupled-inductors-based topologies.

To validate the aforementioned theoretical analysis, the efficiencies of the proposed topology, the mTSCL-qZSN, the SCL-qZSN and the mSSCL-qZSN have been investigated through the simulation results performed in PSIM. To ensure a fair and accurate comparison, simulations have been performed under the same operating conditions and based on the parameters given in Table 2. The windings losses of the coupled-inductors can be approximated as $P_W = \sum_{i=1} R_{Ni} i^2_{Ni(rms)}$. The effective windings resistances mainly depend on the number of windings turns. Consequently, it is reasonable to suppose that the windings losses of the coupled-inductors will be proportional to $\sum_{i=1} N_i i^2_{Ni(rms)}$ [29–35]. Assuming $G = 5, V_{in} = 40\text{V}$, $P_o = 200\text{W}$, $L_m = 150\mu\text{H}$ and using similar core for all topologies, the above-defined criteria for each network is presented in Table 3. It is clearly concluded that the windings losses associated with the coupled-inductors in the proposed qZSN is considerably lower than that of the mTSCL-qZSN, SCL-qZSN, and mSSCL-qZSN. Figure 10 presents the efficiencies of the three impedance networks as a function of voltage gain. It can be observed that for all four converters, efficiency decreases with increasing voltage gain. Moreover, as expected from theoretical analysis, the proposed TSCL-qZSN has a higher efficiency compared to other SCL-based networks. It should be noted that the relatively high windings losses of the mTSCL-qZSN and the mSSCL-qZSN are due to the high currents through their windings N_2 and N_3, respectively, during the shoot-through state.

3.5. Number of Components. Finally, the number of the passive and active components and the size of magnetic elements of the under-study impedance networks are compared in Table 4. Evidently, despite the mentioned advantages for the proposed qZSN, it contains a relatively less number of components, as well as smaller inductive elements.

4. Simulation Results

To verify the behavior of the proposed qZSN under the steady-state and transient conditions, several simulations are performed using PSIM software based on the parameters summarized in Table 5. To simulate the proposed impedance network as a conventional DC-DC converter, a 200 W load is connected to the output switch through a diode and a capacitor as shown in Figure 11. To produce the 200 V output voltage from the dc-input voltage of 40 V, a voltage gain of $G = 5$ is required. According to (16), to achieve this gain, the shoot-through duty ratio must be set to $D_{sh} = 0.2$ with $n = 1$. Accordingly, the theoretical values of the voltages of the capacitors can be calculated as $V_{C1} = 160$ V, $V_{C2} = 120$ V, and $V_{C3} = 80$ V in a steady state. Figures 12 and 13 show the waveforms of the voltages across the output switch and the capacitors, respectively. These results match well with the aforementioned theoretical values. The small difference between the obtained values and the expected ones from the theoretical analysis is chiefly due to the adverse effects of the parasitic elements i.e. the leakage inductances of the coupled-windings and the equivalent series resistances (ESR) of the windings and the capacitors on the voltage gain. The simulated waveforms of the input and the windings currents are shown in Figures 14 and 15. It is clear that the destructive startup current is effectively suppressed by the input inductor. Thus, one can expect that the harmful effects of the huge startup current spikes on the switching semiconductors are appreciably avoided. The waveforms of the windings currents illustrated in Figure 14 verify the theoretical analysis described in Section 2, where the energy transfer between the coupled-inductors and the capacitors can be obviously seen through charging and discharging of the two coupled-windings.

In order to investigate the transient performance of the proposed impedance network, the open-loop responses of the voltages and currents are simulated under sudden changes in the input voltage, the load, and the shoot-through duty ratio. Figures 16–18 show the simulation results when the proposed TSCL-qZSN is subjected to a step change in the input voltage (from 40 V to 60 V), the load (from 200 W to 250 W), and the shoot-through duty ratio (from 0.2 to 0.15), respectively. It can be seen from these waveforms that the proposed topology has been able to successfully damp both voltage and current transients in a relatively short period of time.

5. Experimental Results

In order to validate the operation of the proposed TSCL-qZSN, a 200 W laboratory prototype was built using the parameters listed in Table 4. The proposed qZSN is tested as a DC-DC converter, where a resistive load is connected to the output terminals. The photograph of the implemented prototype is shown in Figure 19. The PWM signals for the output switch *SW* are generated by an ARM microcontroller STM32F407. As illustrated in Figure 20, the switching signal can be simply generated by comparing the shoot-through signal with a 30 kHz triangular carrier signal. To significantly minimize the leakage inductances of the windings, the coupled-inductors are fabricated by winding copper foils on an ER42 ferrite core. The magnetizing inductance measured from the primary side is 150 μH. The experimental results of the proposed converter for the shoot-through duty ratio of $D_{sh} = 0.2$ are shown in Figure 21. According to the

Table 2: Parameters used for efficiency calculation in PSIM.

Parameter	Specification
MOSFET switch	IRFP460
Diodes	CS24050
Input inductor core	C05590A2
SCL core	EE70/33/32
Capacitors	C4AQLBW6100A3MK $(100\mu F/500V)$ESR = 3 $m\Omega$
Copper wire resistivity (ρ)	$1.724 \times 10^{-6}\Omega.m$

Table 3: Comparison of winding losses.

	Proposed TSCL-qZSN ($n = 1.4$)	mTSCL-qZSN ($n = 0.75$)	SCL-qZSN ($n = 1$)	mSSCL-qZSN ($n = 0.5$)
$N_1 i^2_{N1(rms)}$	(16) (2.2^2)	(16) (3.7^2)	(16) (2.8^2)	(16) (2.78^2)
$N_2 i^2_{N2(rms)}$	(22) (3.72^2)	(12) (5.98^2)	(16) (2.8^2)	(16) (2.78^2)
$N_3 i^2_{N3(rms)}$	—	—	(16) (3.73^2)	(8) (7.35^2)
$\sum_{i=1} N_i i^2_{Ni(rms)}$	381.89 turn. A^2	648.16 turn. A^2	473.49 turn. A^2	679.49 turn. A^2

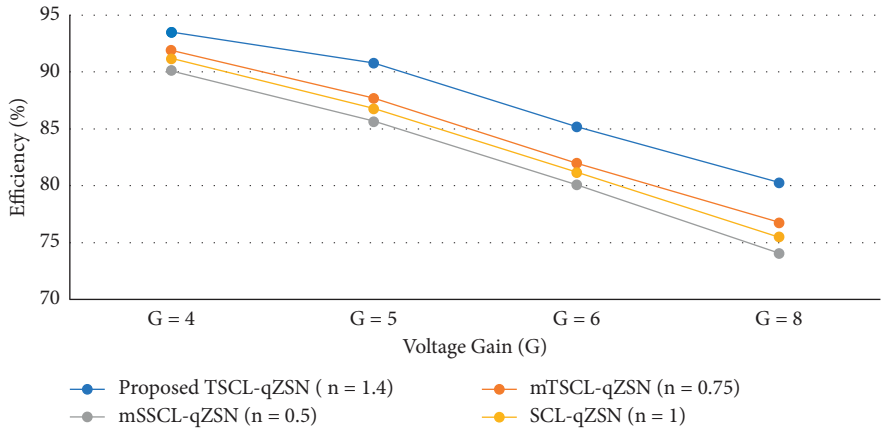

Figure 10: Efficiency comparison of the proposed TSCL-qZSN, the mTSCL-qZSN, the SCL-qZSN, and the mSSCL-qZSN.

Table 4: Numerical comparison between the proposed qZSN and other ZS networks.

Topology	No. of inductors	No. of capacitors	No. of diodes	No. of switches	Size of magnetic cores
Proposed TSCL-qZSN	L_{in}: 1 L_1 and L_2: 2	3	2	Not applicable	Small
SCL-qZSN [31]	L_{in}: 1 L_1, L_2 and L_3: 3	3	3	Not applicable	Medium
mSSCL-qZSN [34]	L_{in}: 1				
L_1, L_2 and L_3: 3	3	3	Not applicable	Small	
mTSCL-qZSN [34]	L_{in}: 1 L_1 and L_2: 2	3	2	Not applicable	Small
Δ-Source network [29]	L_1, L_2 and L_3: 3	1	1	Not applicable	Large
Y-source network [27]	L_1, L_2 and L_3: 3	1	1	Not applicable	Large
Improved trans-ZSN [23]	L_{in}: 1 L_1 and L_2: 2	2	1	Not applicable	Large
ASC/SCL-ZSN [19]	L_1 and L_2: 2	1	5	1	Large
Switched-boost ZSN [18]	L_1 and L_2: 2	2	2	1	Large

theoretical equations of the proposed TSCL-qZSN, a voltage gain of $G = 5$ is attainable with $n = 1$ and $D_{sh} = 0.2$. Therefore, for the input voltage equal to 40 V, the peak voltage across the output switch and the voltages of the steady-state capacitors can be calculated as V_{out} = 200V, V_{C1} = 160V, V_{C2} = 120V and V_{C3} = 80V.

Table 5: Parameters used for simulation and experimental tests.

Parameter	Specification
Input voltage (V_{in})	40 V
Voltage gain (G)	5
Shoot-through duty ratio (D_{sh})	D_{sh} = 0.2
Input inductance (L_{in})	L_{in} = 1 mH
Magnetizing inductance (L_m)	L_m = 150 μH
Output switch (SW)	G4PH50UD
Diodes D_1, D_2 and D_O	D92-02
Capacitors C_1, C_2 and C_3	Film capacitor, 22 μF
Capacitor C_O	100 μF
Coupled-inductors core	Ferrite ER42/22/15
Input inductor core	Toroidal KT 201-26
Winding turn ratio	n = 1 (25 : 25)
Copper wire resistivity (ρ)	$1.724 \times 10^{-6} \Omega.m$
Switching frequency	30 kHz

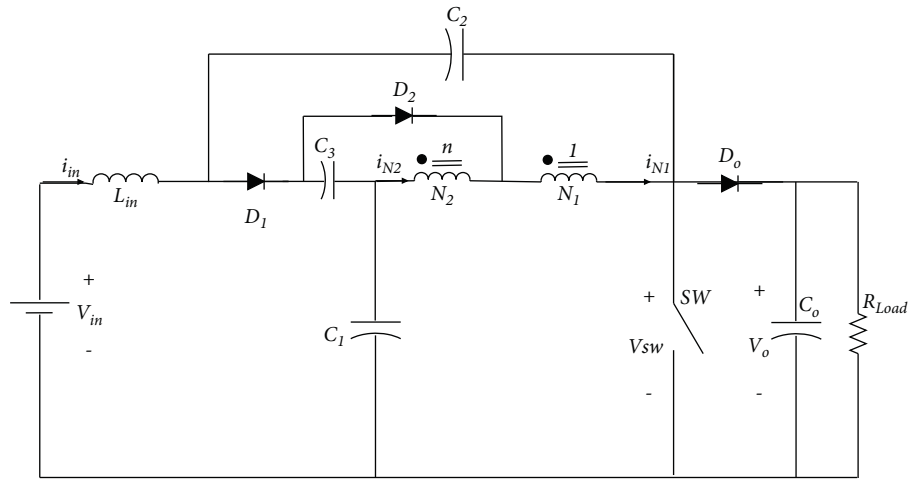

Figure 11: The circuit of the proposed DC-DC converter used in the simulation and experimental tests.

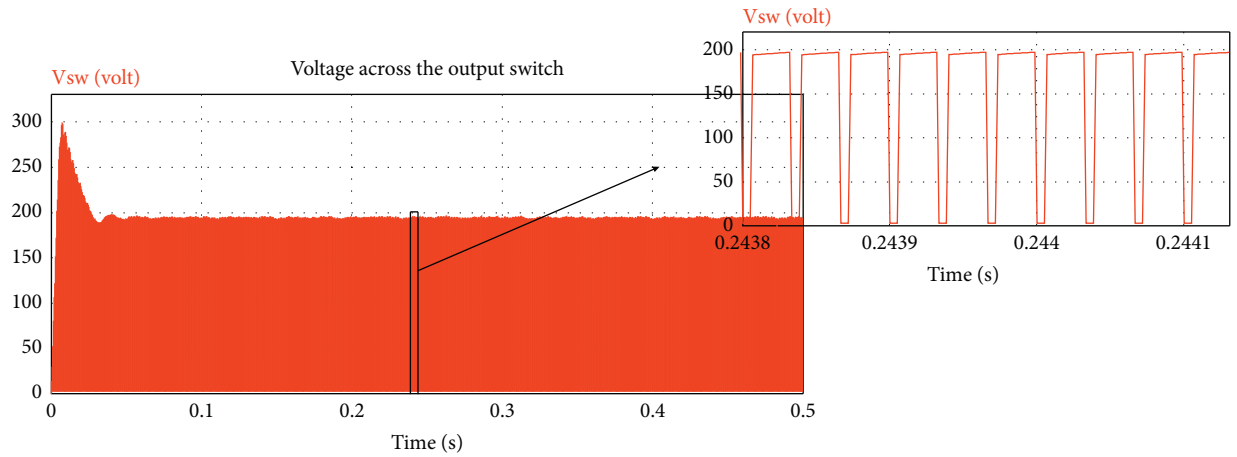

Figure 12: Voltage across the output switch.

Assuming unity efficiency for the proposed converter, the average of the input and the magnetizing currents are obtained as $I_{in} = I_m = 4.05$A.

Figures 21(a) and 21(b) show the experimental waveforms of the voltages across different parts of the proposed network. From these figures, it is clearly seen that the 40 V

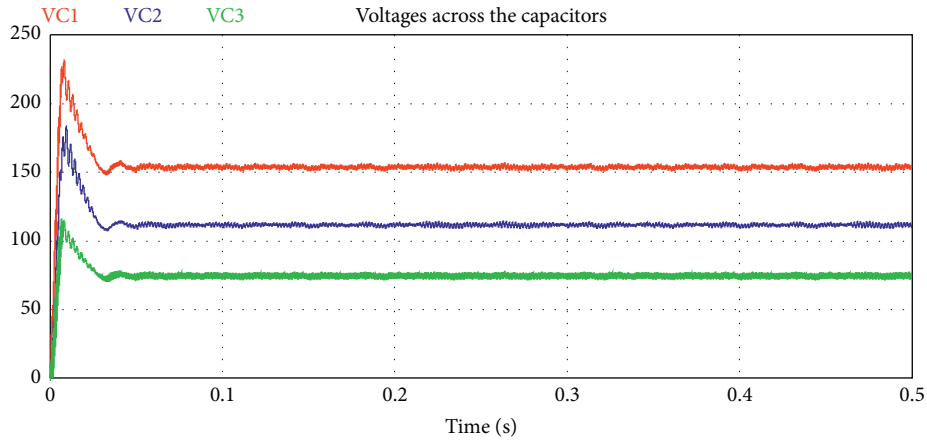

Figure 13: Voltages across the capacitors.

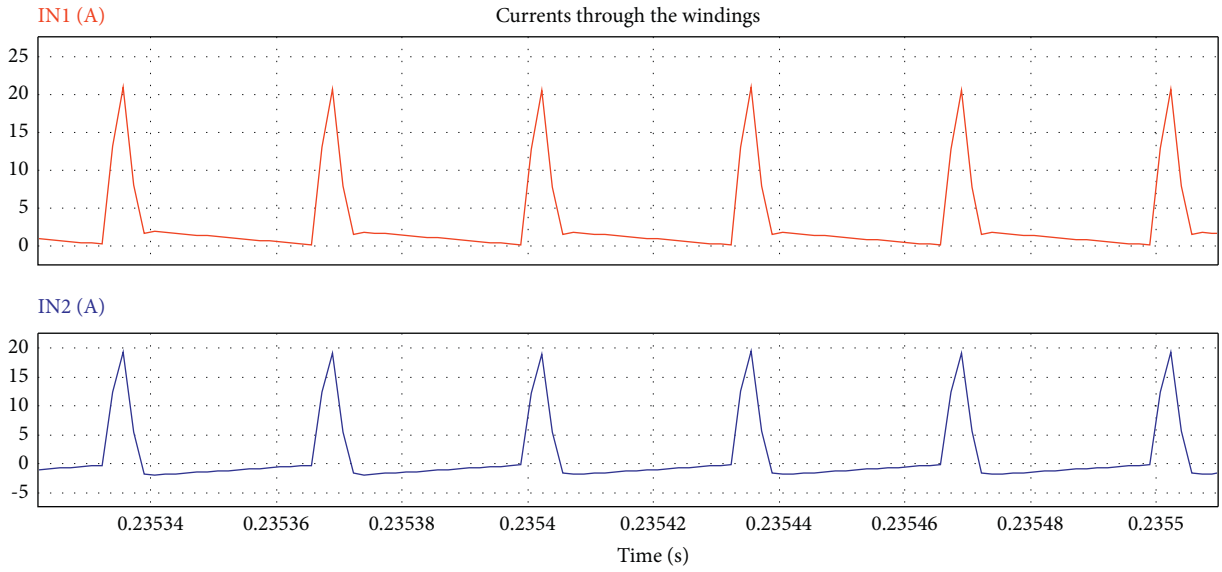

Figure 14: Currents through the coupled-windings.

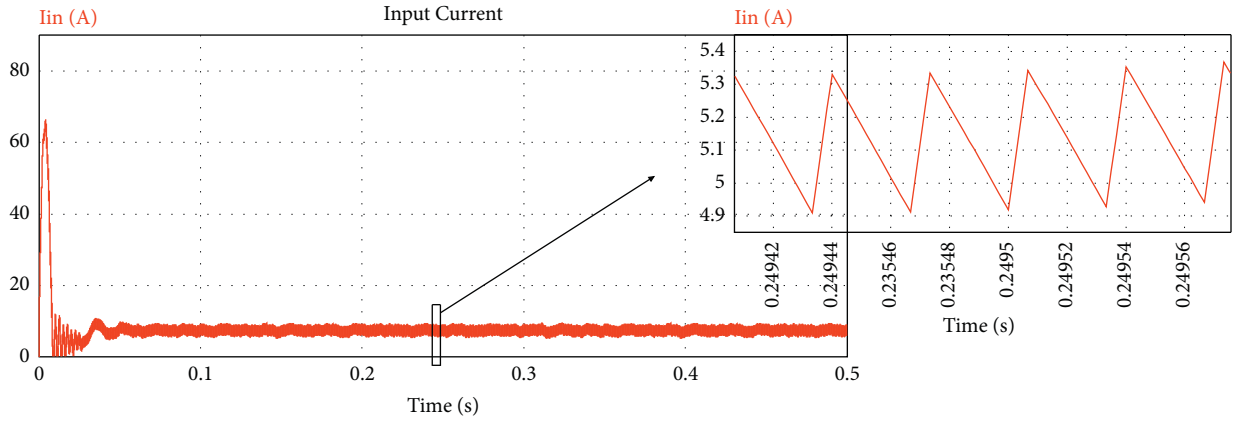

Figure 15: Input current.

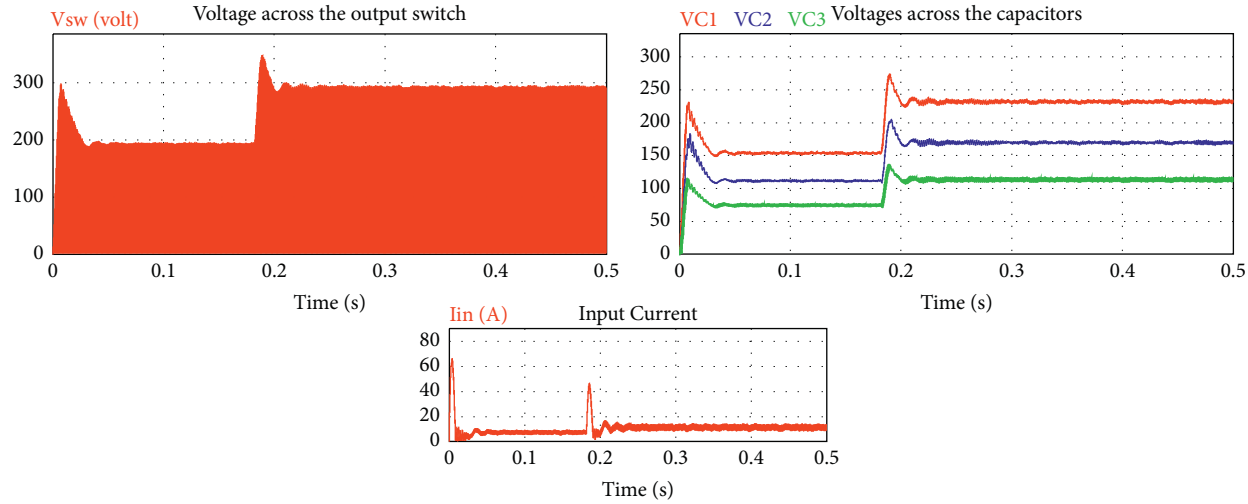

FIGURE 16: Open-loop transient responses of the proposed TSCL-qZSN to a step change of the input voltage.

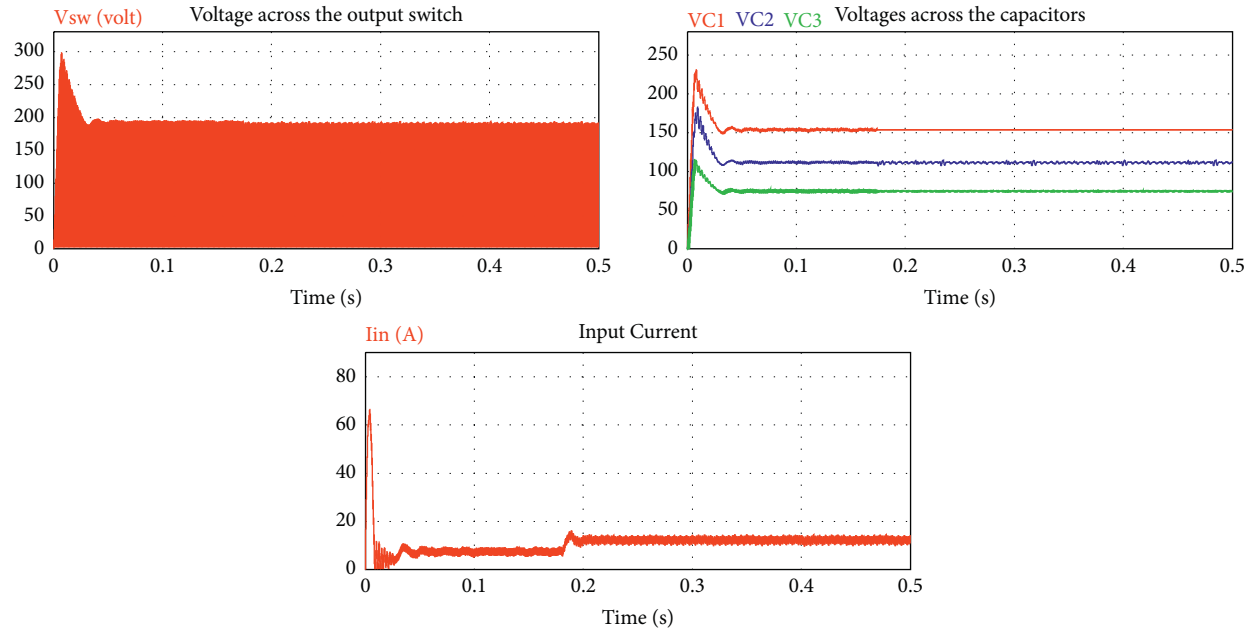

FIGURE 17: Open-loop transient responses of the proposed TSCL-qZSN to a step change of the output power.

input voltage is boosted to about 189 V across the output switch during non-shoot-through states. Evidently, the steady-state value of the load-side output voltage is 192 V, which confirms the high boost ability of the proposed impedance network. The measured voltages across the capacitors are V_{C1} = 153V, V_{C2} = 109V and V_{C3} = 75V, which are consistent with the expected values from the theoretical analysis. The small drops in the output and the voltages of the capacitors compared to the calculated values are mainly due to the voltage drops across the parasitic resistances of the passive components and the conduction voltage drops of the semiconductor devices. Also, the small leakage inductances of the two-winding coupled-inductors slightly reduce the effective shoot-through intervals and subsequently reduce the voltage gain. As evident from Figures 21(a) and 21(b), the output voltage ripple is slightly lower than the voltage ripples across capacitors. This is mainly due to the increase in the load capacitance during non-shoot-through intervals, which effectively reduces the output voltage ripple. The waveforms of the voltages across D_1 and D_2 are shown in Figure 21(b). As expected from the theoretical steady-state operation analysis of the proposed TSCL-qZSN, D_1 is blocking during the shoot-through states while D_2 conducts the current through the winding N_2. Figure 21(c) shows the experimental waveforms of the input, the magnetizing and the two windings currents. It can be seen that the winding N_1 current

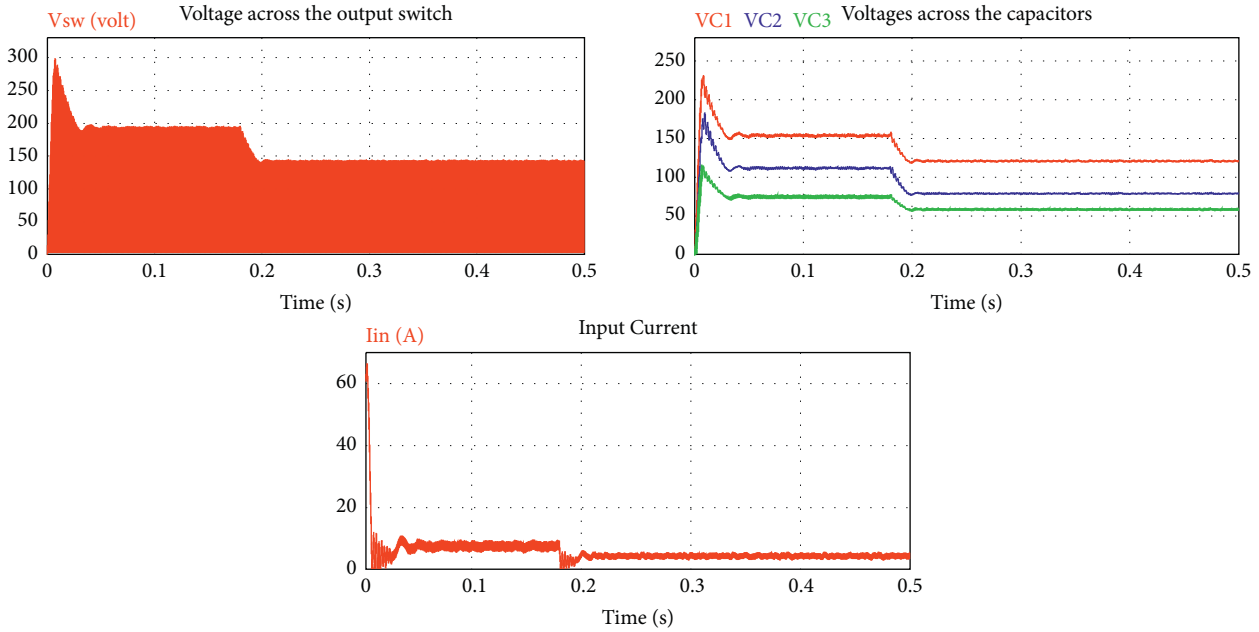

Figure 18: Open-loop transient responses of the proposed TSCL-qZSN to a step change of the shoot-through duty ratio.

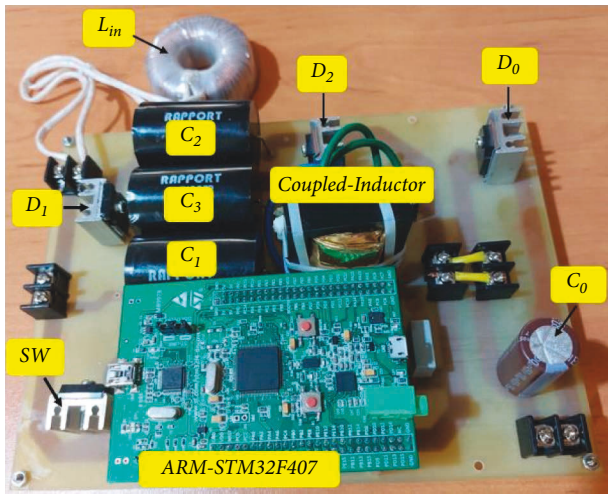

Figure 19: Photograph of the prototype TSCL-qZSN.

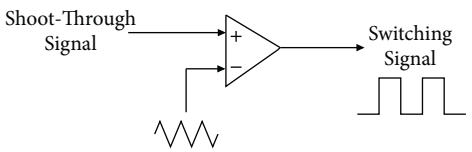

Figure 20: Switching signal generation.

flows in a same direction during the switching period unlike the current through the winding N_2. The average of the input current is $I_{in} = 4.52$A, which is slightly higher than the calculated one. This is due to the fact that the efficiency of the proposed converter is practically lower than unity. As can be observed, by selecting the input inductor as $L_{in} = 1$mH, the input current ripple is limited to 42%. Referring to the magnetizing current to the primary winding, it can be calculated as $N_1 i_m = N_1 i_{N1} + N_2 i_{N2}$. Thus, for $n = 1$, the magnetizing current can be obtained by summing the primary and secondary windings currents. From Figure 21(c), the average magnetizing current is measured as $I_m = 5.01$A. As already expected from (16), the average of the magnetizing current is nearly that of the input current. The minor

Table 6: Measured values of the parameters.

Parameter	Measured value	Parameter	Measured value
V_O	**192 V**	V_{C3}	**75 V**
$V_{SW(peak)}$	**189 V**	Δv_{C3}	**4 V**
V_{C1}	**153 V**	I_{in}	**4.25 A**
Δv_{C1}	**6 V**	Δi_{in}	**1.8 A**
V_{C2}	**109 V**	I_m	**5.01 A**
Δv_{C2}	**4.5 V**	Δi_m	**7.9 A**

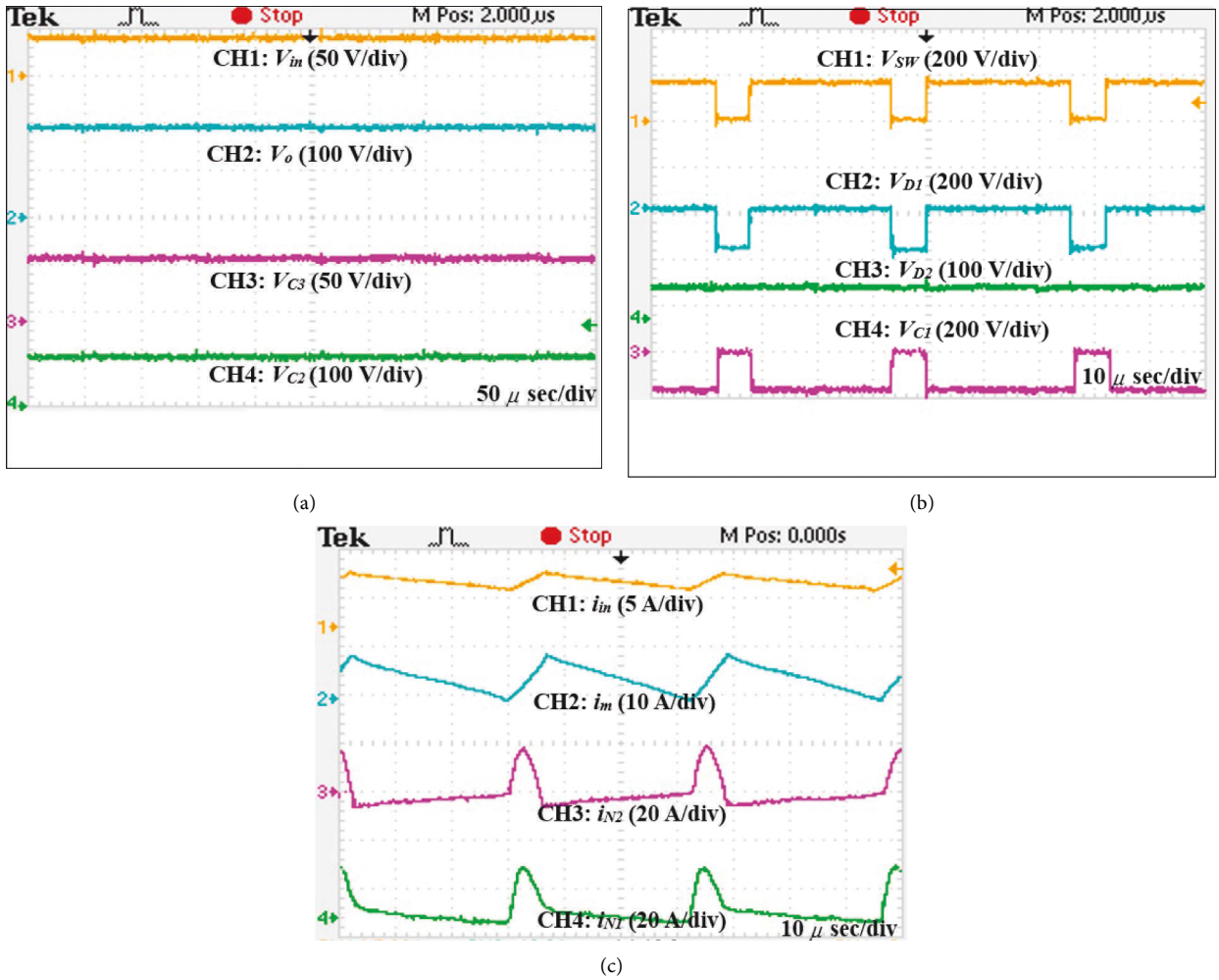

Figure 21: Experimental results of the proposed TSCL-qZSN: (a) the input, the output and the capacitors voltages, (b) the voltages across *SW*, C_1, and the diodes, and (c) the input, the magnetizing and the windings currents.

difference between the values of the two parameters is due to this fact that in the calculation of the magnetizing current requirement of the coupled-inductors described in subsection 3.1, the input and the magnetizing currents are assumed to be constant during both shoot-through and non-shoot-through states. The measured steady-state values of the voltages and currents have been presented in Table 6. It is evident that these values are in a good agreement with the simulation results shown in Figures 12–14. Due to the resonance between the leakage inductances of the coupled-inductors and the capacitors C_1 and C_3 during the shoot-through state, a sinusoidal positive half cycle resonance appears in the currents through the windings, as seen in Figure 21(c). To reduce the voltage spikes across the switching devices and the losses associated with them, it is essential to complete the positive half cycle sinusoidal resonance that occurred between the leakage inductances and the capacitors before ending the shoot-through interval. In fact, with ending the positive half cycle resonance current, the shoot-through current through the output switch is reduced to I_{in}. Therefore, in addition to the reduction in the switching losses, the destructive voltage spikes across the switching devices are effectively eliminated.

Despite the very short duration of the shoot-through state, the appropriate designation of the two-winding coupled-inductors with low leakage inductances guarantees the proper operation of the proposed impedance network.

6. Conclusion

A high gain impedance network is introduced in this paper. The proposed TSCL-qZSN is applicable to various types of converter topologies, including DC-DC, DC-AC, and AC-AC converters. In the proposed topology, the voltage gain is significantly increased by incorporating a combination of a switched-capacitor and a tapped two-winding SCL into the impedance network. Moreover, high voltage gains can be achieved with short shoot-through durations. The size of magnetic core for the coupled-inductors is relatively small in the proposed network, since it needs a low peak magnetizing current. As a prominent feature, the proposed qZSN has a lower shoot-through current and total voltage stress compared to previous well-known SCL-based ZSNs, which leads to lower switch loss and reduction in the passive components and output switch ratings requirement. Additionally, a reduced number of components and employing the two-winding coupled-inductors with smaller core size and less turns number result in lower power losses associated with the diodes and the coupled-inductors. Other outstanding features of the proposed TSCL-qZSN can be summarized as continuous input current, common ground between the input voltage source and the load-side, and low coupled-inductors current-handling requirement. The theoretical analysis is successfully verified through experimental results.

Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no known conflicts of interest.

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