Research Article

A Novel Structure for Transformerless Grid-Connected PV Inverter to Eliminate Common-Mode Current under Mismatch Condition

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Common-mode current is one of the major challenges in transformerless grid-connected photovoltaic (PV) inverters. This current is affected when the PV arrays are exposed to different environmental conditions and its value increases. This paper attempts to investigate the effect of mismatched condition on voltage balance of PV arrays, which leads to the increment of common-mode current. A new circuit structure is presented for compensating for voltage drop caused by partial shading and ambient temperature and removing the effect on the common-mode current. To validate the proposed structure, a laboratory prototype of this circuit is implemented.

1. Introduction

In recent years, grid-connected photovoltaic (PV) systems have become increasingly significant due to rising prices of fossil fuel, sustainability of solar energy, and its reliability. Two categories of inverters (with transformer isolation and transformerless) can be employed for connecting PV systems to the grid. Transformerless inverters have attracted more attention due to some advantages such as smaller size, lower price, and higher efficiency [1–3].

Mismatched condition is one of the major problems of photovoltaic systems, which leads to the reduction of the generated energy by the PV arrays. Many structures are presented to solve this problem by balancing the input voltage or creating bypass path for the current [8–13].

One type of these structures is switched-capacitor converters which balance the input voltage through charging and discharging of capacitors [8, 9]. The resonant switched capacitors are used for balancing input voltage by transferring additional energy from an array with higher voltage to an array with lower voltage [10]. A switched-capacitor converter with one capacitor and several switches is presented in [11], which performs balancing. Other converters include buck-boost converters and multiwinding transformers [12, 13]. In [14], a single-stage transformerless PV inverter topology and the PWM strategy are proposed for producing continuous power from the PV during any condition of solar radiance. The objective of paper [15] is to present a new modulation strategy for the leakage current reduction of Z source four-leg inverter for transformerless PV systems. In [16], a new circuit configuration for the
An inverter having a single DC link capacitor and seven IGBTs is proposed. The common-mode voltage is kept at a constant value and the ground leakage current is suppressed. The aim of [17] is to present a new type of transformerless inverters, which is a common ground-based topology and can improve the performance of the system by its inherent boosting feature and unipolar PWM scheme. In [18], a new inverter topology is proposed. The proposed inverter develops a four-level voltage through four switches, two diodes, and four capacitors.

A major challenge in connecting PV arrays to the power grid through transformerless inverters is the common-mode current. It flows through parasitic capacitors and is located between photovoltaic arrays and ground, which leads to some major issues [19, 20]. It causes loss increase, quality reduction of the injected current to the grid, electromagnetic interference, inaccurate performance of the protective relays, and especially some issues related to the personal safety [21, 22].

Therefore, suppression or elimination of common-mode current has turned into a hot topic over the recent decades through inventing many structures by separating PV arrays from AC source or adding an extra clamped circuit [23–26]. In the separating method, the panel is separated from the grid by adding one or more switches to the main structure. The main converters in this category are H5 [23], H6 [24], HERIC [25], and the high-efficiency transformerless inverter presented in [26]. In clamp circuit method, an additional circuit is employed for clamping the midpoint voltage of the inverter legs. A common-mode reduction method is to connect grid negative terminal to the midpoint of DC link capacitors, which causes a constant common-mode voltage equal to half of input value [27].

Many of the recent solutions for common-mode current elimination in two-subarray PV system were only successful with equal DC link capacitors. Environmental condition leads to variation of DC link voltages, which increases common-mode current.

Different topologies are presented to solve this problem. A new inverter topology is proposed in [4], which is derived by combining two half bridge inverters along with their respective AC bypass. Two serially connected arrays are controlled individually by these two half bridge inverters. As the voltage across parasitic capacitors has only low frequency components, the magnitude of leakage current is low and remains within the standard permissible range (see Figure 1(a)). In [28], each PV array is controlled by a buck-boost-based inverter.

In [5], two subarrays are connected in series. The neutral point clamped-based structure of the inverter leads to elimination of leakage current (see Figure 1(b)). Despite the fact that all these topologies are able to eliminate leakage current during environmental condition, they lose output power significantly in this condition.

In this paper, a structure is introduced which eliminates the common-mode current considering partial shading and ambient temperature effect. Among all topologies that were mentioned before, those in [4, 5] and proposed topology are the only structures that considered leakage current during environmental condition.

The remainder of the paper is organized as follows: an investigation of the common-mode current is presented in Section 2; an introduction and investigation of the presented circuit are presented in Section 3; simulation and experimental results are presented in Section 4; ultimately, conclusions are provided in Section 5.

2. Investigating the Common-Mode Current and the Effects of Environmental Condition

Figure 2 shows the common-mode current loop, where $C_{PV}$ is the parasitic capacitance and its value depends on size and frame of the PV array, humidity, and so forth. Points A and B are the midpoints of inverter legs and N is the negative terminal of DC link.

Common-mode voltage ($V_{CM}$) and differential-mode voltage ($V_{DM}$) are related to $V_{BN}$ and $V_{AN}$, which are expressed as follows [29]:

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2}, \quad (1)$$

$$V_{DM} = V_{AN} - V_{BN}. \quad (2)$$

$V_{DM}$ causes generation of additional common-mode voltage ($V_{CM,DM}$) and influences on common-mode current which is obtained as [30]

$$V_{CM-DM} = \frac{V_{AN} - V_{BN}}{2} \times \frac{L_1 - L_2}{2(L_1 + L_2)}. \quad (3)$$
where \( L_1 \) and \( L_2 \) are grid side filters. Therefore, the total common-mode voltage and common-mode current will be equal to

\[
V_{CM\text{-all}} = V_{CM} + V_{CM\text{-DM}} = \frac{V_{AN} + V_{BN}}{2} + \frac{V_{AN} - V_{BN}}{2} \times \frac{L_1 - L_2}{2(L_1 + L_2)} \tag{4}
\]

\[
I_{CM} = C_{PV} \times \frac{dV_{CM\text{-all}}}{dt} \tag{5}
\]

Obviously, if \( L_1 \) and \( L_2 \) are equal, \( V_{CM\text{-DM}} \) will be zero and the value of the total common-mode voltage will be equal to \( V_{CM} \) [31]. It is concluded that the common-mode current would be zero by keeping \( V_{CM} \) constant.

Normally, in order to eliminate the common-mode current in grid-connected transformerless inverters, they can be restructured by adding some other switches and elements in order to stabilize common-mode voltage at a certain level using special switching states. Switching modes of Figure 1 can be categorized into the three following states:

To generate \(+ V_{DC}\) output voltage, legs A and B are connected to points P and N of DC link input, respectively, and, therefore, common-mode voltage is calculated:

\[
V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{AP} + V_{PN} + V_{BN}}{2} \tag{6}
\]

To generate \(- V_{DC}\) zero output voltage, legs A and B are connected to point O and PVs are separated from the source. In this state, the common-mode voltage is obtained as

\[
V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{AO} + V_{ON} + V_{BO} + V_{ON}}{2} = \frac{0 + V_{DC}/2 + 0 + (V_{DC}/2)}{2} = \frac{V_{DC}}{2} \tag{7}
\]

To generate \(- V_{DC}\) output voltage, legs A and B are connected to N and P, respectively. Like the first state, the common-mode voltage is equal to

\[
V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{AN} + V_{BP} + V_{PN}}{2} = \frac{0 + 0 + V_{DC}}{2} = \frac{V_{DC}}{2} \tag{8}
\]

Therefore, the common-mode voltages of all states are the same and equal to \( V_{DC/2} \), which does not generate common-mode current. This condition is valid until the voltages of both capacitors are equal. However, if a \( PV \) array is subjected to different environmental condition, the voltage of the related array will be reduced, which leads to unbalanced capacitors voltages. For example, in Figure 2, in case of mismatched condition on the upper subarray, \( V_{C1} \) reduces to \( V_{DC/2} - \Delta V \) (\( \Delta V \) is the voltage drop caused by mismatched condition) and \( C_2 \) capacitor’s voltage will be equal to \( V_{DC/2} \). Therefore, the common-mode voltages during achieving output voltages of \(+ V_{DC}\), 0, and \(- V_{DC}\) respectively, are

\[
V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{(V_{DC}/2) - \Delta V + (V_{DC}/2) + 0}{2} = \frac{V_{DC} - \Delta V}{2} \tag{9}
\]

\[
V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{(V_{DC}/2) + (V_{DC}/2) + 0}{2} = \frac{V_{DC}}{2}, \tag{10}
\]

\[
V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{(V_{DC}/2) - \Delta V + (V_{DC}/2) + 0}{2} = \frac{V_{DC} - \Delta V}{2} \tag{11}
\]

As can be observed, the common-mode voltage would have different values in every state, which leads to the generation of common-mode current. As the amount of partial shading and ambient temperature increases, the amount of voltage drop increases, too.

3. Circuit Topology and Its Operating Principals

The general structure of proposed circuit is shown in Figure 3. This circuit consists of primary section which is applied for common-mode current elimination and the effect of mismatched condition and secondary section which is an inverter for grid-connection purposes. At first, it is assumed that the circuit is in a normal no-mismatch condition.

3.1. Circuit Performance in Normal Condition. In this case, switches \( S_7 \) and \( S_8 \) are turned off which exit inductors of the primary section (\( L_1, L_2 \)) and the circuit has four modes of operation (see Figure 4). Hence, assuming that the voltages of \( C_1 \) and \( C_2 \) are \( V_{DC/2} \), the performance states of the circuit are expressed as follows (see Figure 5):

State A-1: switches \( S_1 \), \( S_4 \), \( S_5 \), and \( S_6 \) are on. Here, \( V_{AN} \), \( V_{BN} \), and output voltage are equal to \( V_{DC/2} \), 0, and \( V_{DC} \). The common-mode voltage in this state is \( V_{DC/2} \) (see Figure 4(a)).

State A-2: switches \( S_1 \), \( S_2 \), \( S_5 \), and \( S_6 \) and diode \( D_3 \) are on. Here, \( V_{AN} \) and \( V_{BN} \) are equal to \( V_{DC/2} \), and the output voltage is 0. In this case, \( PV \) is disconnected from the grid for freewheeling. The common-mode voltage for this state is \( V_{DC/2} \) (see Figure 4(b)).
State A-3: In this case, switches S2, S3, S5, and S6 are on. Here, $V_{AN}$ is equal to 0 and $V_{BN}$ is equal to $V_{DC}$, and the output voltage is equal to $-V_{DC}$. The common-mode voltage in this state is $V_{DC}/2$ (see Figure 4(c)).

State A-4: In this case, switches S4, S3, and S5 and diode $D_4$ are on. Here, $V_{AN}$ and $V_{BN}$ are equal to $V_{DC}/2$, and the output voltage is 0. In this state, $PV$ is disconnected from the grid for freewheeling. The common-mode voltage in this state is $V_{DC}/2$ (see Figure 4(d)).

As can be observed, $V_{CM}$ is $V_{DC}/2$ for all states, which causes the elimination of the common-mode current according to equation (5).
3.2. Circuit Performance under Mismatch Condition. As mentioned in Figure 3, proposed circuit has two primary and secondary sections with the function of capacitor voltage balancing and grid connection, respectively.

3.2.1. Considering the Circuit without Primary Circuit (S7 and S8: OFF). If mismatch condition occurs at first subarray, $V_{C1} = V_{DC}/2 - \Delta V$ and $V_{C2} = V_{DC}/2$. Therefore, common-mode voltages at states A-1 to A-4 in mismatch condition will be as follows:

\[
\text{State A - 1: } V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{(V_{DC}/2) - \Delta V + (V_{DC}/2) + 0}{2} = \frac{V_{DC} - \Delta V}{2},
\]

\[
\text{State A - 2: } V_{CM} = \frac{(V_{DC}/2) + (V_{DC}/2)}{2} = \frac{V_{DC}}{2},
\]

\[
\text{State A - 3: } V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{(V_{DC}/2) - \Delta V + (V_{DC}/2) + 0}{2} = \frac{V_{DC} - \Delta V}{2},
\]

\[
\text{State A - 4: } V_{CM} = \frac{(V_{DC}/2) + (V_{DC}/2)}{2} = \frac{V_{DC}}{2}.
\]

3.2.2. Considering the Circuit with Primary Circuit (S7 and S8: ON). As can be observed, the common-mode voltage for each state is different from the other ones, which creates common-mode current according to equation (5). Therefore, a balancing circuit is required. In this case, depending on the location of shading and ambient temperature (upper or lower subarrays), the mismatch effect on the common-mode current can be eliminated by switching switches $S_7$ or $S_8$. It is worth mentioning that switching of these two switches is independent of other circuit components.

When the mismatch occurs on the PVs, the circuit has six modes of operation (see Figures 6 and 7). Assuming that the shading falls on the upper PV, common-mode voltages for these six states are as follows:

\begin{figure}
\centering
\includegraphics[width=\textwidth]{normal_operating_modes_diagram.png}
\caption{Normal operating modes diagram.}
\end{figure}

State B-1: switches $S_1$, $S_4$, $S_5$, and $S_6$ are on. Here, $V_{AN}$ is equal to $V_{DC}$ and $V_{BN}$ is equal to 0, and the output voltage is equal to $V_{DC}$. By turning switch $S_8$, $L_2$ inductor current begins to increase (see Figure 6(a)).

State B-2: like the first state, switches $S_1$, $S_4$, $S_5$, and $S_6$ are on, and $V_{DC} = V_{ANS}$, $V_{BN} = 0$, and the output voltage is $V_{AB} = V_{DC}$. Here, by turning switch $S_8$ off, inductor $L_2$ which is charged by the lower subarray will be discharged on capacitor $C_1$ and cause an increase in capacitor voltage (see Figure 6(b)).

State B-3: according to Figure 7(a), switches $S_1$, $S_2$, and $S_6$ and diode $D_3$ are on, and PV is disconnected from the grid for freewheeling. Here, $V_{AN}$ and $V_{BN}$ are equal to $V_{DC}/2$ and output voltage is 0. Here, by turning switch $S_8$ on, inductor $L_2$ is charged by capacitor $C_2$.

State B-4: like state 3, switches $S_1$, $S_2$, and $S_6$ and diode $D_3$ are on, $V_{BN}$ and $V_{AN}$ are equal to $V_{DC}/2$, and the output voltage is 0. Here, by turning switch $S_8$ off, inductor $L_2$ which
was previously charging begins to discharge in capacitor \( C_1 \) (see Figure 7(b)).

State B-5: In this case, according to Figure 8(a), switches \( S_2, S_3, S_5, \) and \( S_6 \) are on. Here, \( V_{AN} \) is 0 and \( V_{BN} \) is equal to \( V_{DC} \). and the output voltage is equal to \( -V_{DC} \). In this state, by turning switch \( S_8 \) on, inductor \( L_2 \) is charged by capacitor \( C_2 \).

State B-6: In this case, like state 5, switches \( S_2, S_3, S_5, \) and \( S_6 \) are on, and \( V_{AN} \leq 0, V_{BN} = V_{DC}, \) and \( V_{AB} = -V_{DC} \). Here, by turning switch \( S_8 \) off, inductor \( L_2 \) is discharged in capacitor \( C_1 \) (Figure 8(b)).

As can be observed in all the above six states, regardless of the inverter conditions, the primary circuit can charge or discharge \( L_2 \) by turning \( S_7 \) off and switching of \( S_8 \). Therefore, it compensates the voltage drop caused by partial shading on the upper PV. The conceptual waveforms of gate signal of the switches, leg voltages, and common-mode voltage of all possible states are brought in Figure 9(a). The same procedure can be carried out for partial shading of lower subarray. In this case, signals of \( S_1 \) and \( S_8, S_2 \) and \( S_5, S_3 \) and \( S_6 \) and \( S_8 \) and \( S_7 \) will be replaced with each other (see Figure 9(b)).

3.3. Switching Method. When the insolation level and ambient temperature of subarray \( PV1 \) are different from those of \( PV2 \), the MPP parameters of the two subarrays differ from each other. By considering that both subarrays are operating at their respective MPP and neglecting the losses incurred in power processing stages, the average power involved with \( C_1 \) and \( C_2 \) over a cycle can be assumed equal to the power extracted from \( PV1 \) and \( PV2 \). Therefore,

\[
P_{C1} + P_{C2} = P_{PV1} + P_{PV2}.
\]  

(16)

The average power injected to the grid, \( P_g \), can be written as

\[
P_g = P_{PV1} + P_{PV2},
\]

(17)

and

\[
P_g = V_{grid}I_{grid} \cos \phi = \frac{1}{2} V_m I_m \cos \phi,
\]

(18)

where \( V_m \) and \( I_m \) are the amplitude and current of the grid voltage (\( V_{grid} \) and \( I_{grid} \)), respectively. The relation of output and input voltage of inverter can be expressed as

\[
V_m = m_c(V_{C1} + V_{C2}),
\]

(19)

where \( m_c \) is the modulation index of the inverter.
By combining the above equations, the power injected to the grid can be expressed as

\[
P_g = \frac{1}{2} m_a (V_{C1} + V_{C2}) I_m \cos \phi = P_{PV1} + P_{PV2}. \tag{20}\]

Hence,

\[
P_{PV1} = \frac{1}{2} m_a V_{C1} I_m \cos \phi. \tag{21}\]

Similarly,

\[
P_{PV2} = \frac{1}{2} m_a V_{C2} I_m \cos \phi. \tag{22}\]

Therefore,

\[
V_{C1} = \frac{2P_{PV1}}{m_a I_m \cos \phi}, \tag{23}\]

\[
V_{C2} = \frac{2P_{PV2}}{m_a I_m \cos \phi}. \tag{24}\]

By combining (20), (21), and (22),

\[
V_{C1} = \frac{V_m P_{PV1}}{m_a (P_{PV1} + P_{PV2})}, \tag{25}\]

\[
V_{C2} = \frac{V_m P_{PV2}}{m_a (P_{PV1} + P_{PV2})}. \tag{26}\]

Based on the above equations, the control strategy of the proposed scheme is shown in Figure 10.

In this control strategy, both subarrays operate at their corresponding MPPT simultaneously. Two separate MPP trackers are employed to determine the values of $PV_1$ and $PV_2$, which are required to estimate $V_{C1}$ and $V_{C2}$. Using (25) and (26), $V_{C1}$ and $V_{C2}$ are estimated [4, 28]. $V_{C1}$ and $V_{C2}$ are compared to $V_{ref2}$ (which in this case is 200 V) and after two separate PI controllers and a PWM block for every two, $S_7$ and $S_8$ are determined. Hence, two voltage sensors that otherwise would have been required to determine $V_{C1}$ and $V_{C2}$ get eliminated.

The switching method of the presented circuit is unipolar SPWM which is displayed in Figure 11. First (second) cycles occur when the shading falls on upper (lower) $PV$, where $V_c$ is triangular waveform and $V_{ref}$ is reference.
waveform which is obtained as feedback from the grid. By comparing these two waveforms, depending on where the mismatch occurs, the switching method of switches is determined. Control method of the circuit is shown in Figure 12.

Switching states of $S_7$ and $S_8$ are directly determined by Figure 10.

3.4. Stability. Given Table 1 and Figure 13, new $S_a$, $S_b$, and $S_c$ functions are defined for switching of the proposed inverter.

$$S_a = S_1 - S_2,$$

$$S_b = S_2 - S_1,$$

$$S_c = S_4 - S_3,$$

$$S_d = S_3 - S_2,$$

$$S_e = S_1 - S_4,$$

and, using Table 1 and Figure 13, the inverter model can be written as

$$V_{\text{out}} = S_a V_{DC} + S_b V_{C1} + S_c V_{C2} + S_d V_{L1} + S_e V_{L2}.$$

The capacitors dynamics are expressed as

$$I_{C1} = C_1 \frac{dV_{C1}}{dt} = -S_b i_g + S_c I_{L1},$$

$$I_{C2} = C_2 \frac{dV_{C2}}{dt} = -S_b i_g + S_c I_{L1},$$

and the inductors dynamics are expressed as

$$V_{L1} = S_b V_{C1} - S_c V_{C2},$$

$$\frac{di_{L1}}{dt} = \frac{1}{L_1} (S_b V_{C1} - S_c V_{C2}),$$

$$V_{L2} = S_c V_{C2} - S_b V_{C1},$$

$$\frac{di_{L2}}{dt} = \frac{1}{L_2} (S_c V_{C2} - S_b V_{C1}),$$

while the grid model and the current dynamics can be written as

$$\frac{di_g}{dt} = \frac{1}{L_g} - r_g i_g + \frac{1}{L_g} (V_{\text{out}} - V_g).$$

One can define the grid current error as $X_1 = i_g - i_g^*$, where $i_g^*$ represents the grid current reference signal.
Similarly, the capacitors voltage errors may be defined as $X_2 = V_{C1} - V_{C1}^{*}$ and $X_3 = V_{C2} - V_{C2}^{*}$, where $V_{C1}$ and $V_{C2}$ are constant DC voltages. The inductors current errors may be defined as $X_4 = -I_{L1}^{*} + I_{L1}$ and $X_5 = -I_{L2}^{*} + I_{L2}$, where $I_{L1}$ and $I_{L2}$ are constant DC currents.

From the above equations, the current error derivative can be written as $x_1 = \frac{di_g}{dt} = \frac{di_g}{dt}$.

Using (13), $i_g = X_1 + i_g^{*}$, $V_{C1} = X_2 + V_{C1}^{*}$, $V_{C2} = X_3 + V_{C2}^{*}$, $I_{L1} = X_4 + I_{L1}^{*}$, and $I_{L2} = X_5 + I_{L2}^{*}$, one can obtain

$$x_1 = \frac{1}{L_g} \left[ S_a V_{DC} + S_b (X_2 + V_{C1}^{*}) + S_c (X_3 + V_{C2}^{*}) + S_d \left( S_b (X_2 + V_{C1}^{*}) - S_c (X_3 + V_{C2}^{*}) \right) + S_e \left( S_c (X_3 + V_{C2}^{*}) - S_b (X_2 + V_{C1}^{*}) \right) - \left( r_g \left( X_1 + i_g^{*} + V_g + L_g \frac{di_g}{dt} \right) \right) \right].$$

Similarly, after substituting the expressions of $i_g = X_1 + i_g^{*}$, $I_{L1} = X_4 + I_{L1}^{*}$, and $I_{L2} = X_5 + I_{L2}^{*}$ in (7) and (8), the capacitors voltage errors may be written as

$$x_2 = \frac{1}{C_1} \left( S_b i_g + S_c I_{L2} \right) = \frac{1}{C_1} \left( S_b (X_1 + i_g^{*}) + S_c (X_5 + I_{L2}^{*}) \right).$$

$$x_3 = \frac{1}{C_2} \left( S_b i_g + S_c I_{L1} \right) = \frac{1}{C_2} \left( S_b (X_1 + i_g^{*}) + S_c (X_4 + I_{L1}^{*}) \right).$$

Similarly, after substituting the expressions of $V_{C1} = X_2 + V_{C1}^{*}$ and $V_{C2} = X_3 + V_{C2}^{*}$ in (10) and (12), the inductors current errors may be written as

$$x_4 = \frac{1}{L_1} \left( S_b (X_2 + V_{C1}^{*}) - S_c (X_3 + V_{C2}^{*}) \right).$$

$$x_5 = \frac{1}{L_2} \left( S_c (X_3 + V_{C2}^{*}) - S_b (X_2 + V_{C1}^{*}) \right).$$

The Lyapunov function can be defined in terms of system state errors, represented by vector $x$. Assume that the equilibrium of controlled system is at the origin $x=0$. When the energy function becomes zero, the system is settled at the equilibrium point, and if the energy function is rapidly increasing, then the system is unstable, and it is asymptotically stable if the energy is decreasing. The stability of a system is guaranteed if the following conditions hold:

1. $V(x)$ is positive definite
2. $-V(x)$ is negative definite
3. $V(x)$ goes to $\infty$ as $|x| \to \infty$

A Lyapunov function in terms of system’s errors is suggested as follows:

$$V(x) = \frac{1}{2} a_1 x_1^2 + \frac{1}{2} a_2 x_2^2 + \frac{1}{2} a_3 x_3^2 + \frac{1}{2} a_4 x_4^2 + \frac{1}{2} a_5 x_5^2,$$

where $a_1$ and $a_2$ are real positive numbers, which must be properly selected. It is clear that the above function is positive definite. Lyapunov control theory states that stability of the controlled system presented above is guaranteed if we ensure that, for all values of $x$, $\dot{V}(x) < 0$. 

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**Table 1: Switching states and terminal voltages.**

<table>
<thead>
<tr>
<th>$V_{out}$</th>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>$S_4$</th>
<th>$S_5$</th>
<th>$S_6$</th>
<th>$S_7$</th>
<th>$S_8$ on</th>
<th>$S_8$ off</th>
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<td>+1</td>
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<td>1</td>
<td>1</td>
<td>1</td>
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<table>
<thead>
<tr>
<th>$C_1$ charging</th>
<th>$C_1$ discharging</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_2$ charging</td>
<td>$C_2$ discharging</td>
</tr>
</tbody>
</table>

**Figure 13: Schematic of the proposed inverter.**
\[ \dot{v}_x = a_1 x_1 \dot{x}_1 + a_2 x_2 \dot{x}_2 + a_3 x_3 \dot{x}_3 + a_4 x_4 \dot{x}_4 + a_5 x_5 \dot{x}_5. \]  

(46)

Using equations (40)–(44) in (46), one can get

\[
\begin{align*}
\dot{v}_x &= X_1 x_2 (a_2 S \nu (S_d - S_e)) / L_g - a_5 S \nu / C_1 + x_1 x_3 (a_1 S_c (S_e - S_d)) / L_g - a_5 S \nu / C_2 - x_2 x_5 (a_5 S c / C_1 + a_5 S \nu / L_2) - x_3 x_4 (a_3 S d / C_2 + a_3 S \nu / L_1) + x_3 \nu (a_2 S c / C_1 + a_4 S \nu / L_1) + x_5 \nu (a_3 S c / L_2) + x_5 \nu (a_4 S c / L_2) - x_5^2 (a_1 r / L_g) + x_5^2 (a_1 V_{DC} + V_{C1} (S_b + S_d S_b + S_e S_e) + V_{C2} (S_c + S_d S_c + S_e S_e) - r_g i^* - V_g) / L_g - a_1 (d i^* / d t) + x_3 \left( (a_3 (-S_b i^* + S_d i^*_L + S_e i^*_L)) / C_1 \right) + x_4 \left( (a_4 S v_{C1} - S_c V_{C2}) / C_2 \right) + x_4 \left( (a_4 S v_{C2} - S_b V_{C1}) / C_2 \right) / L_1 + x_5 \left( (a_5 (S_c v_{C2} - S_b V_{C1})) / L_2 \right) (36).
\end{align*}
\]

After eliminating \( X_1 x_2, X_1 x_3, X_2 x_5, X_3 x_4, X_2 x_4, \) and \( X_3 x_5 \) terms, we have

In order to eliminate \( X_1 x_2, X_1 x_3, X_2 x_5, X_3 x_4, X_2 x_4, \) and \( X_3 x_5 \) terms, gains are chosen to satisfy

\[ \alpha_1 = \frac{L_g}{C_1 (S_d - S_e)} \alpha_2, \]  

(47)

\[ \alpha_3 = \frac{S_c C_2 (S_c - S_d)}{L_g S_b} \alpha_1, \]  

(48)

\[ \begin{align*}
\dot{v}_x &= -X_1^2 \left( \frac{a_1 r_g}{L_g} \right) + X_1 \left( \frac{a_1 (V_{DC} + V_{C1} (S_b + S_d S_b + S_e S_e) + V_{C2} (S_c + S_d S_c + S_e S_e) - r_g i^* - V_g)}{L_g} - \frac{a_1 i^*}{d t} \right) \\
&+ X_2 \left( \frac{a_2 (-S_b i^* + S_d i^*_L + S_e i^*_L)}{C_1} \right) + X_3 \left( \frac{a_3 (-S_b i^* + S_d i^*_L + S_e i^*_L)}{C_2} \right) \\
&+ X_4 \left( \frac{a_4 (S_c v_{C1} - S_b V_{C2})}{L_1} \right) + X_5 \left( \frac{a_5 (S_c v_{C2} - S_b V_{C1})}{L_2} \right).
\end{align*} \]  

(53)

Then we have

\[ \begin{align*}
\dot{v}_x &= -X_1^2 \left( \frac{a_1 r_g}{L_g} \right) + X_1 \left( \frac{a_1 (V_{DC} + V_{C1} (S_b + S_d S_b + S_e S_e) + V_{C2} (S_c + S_d S_c + S_e S_e) - r_g i^* - V_g)}{L_g} - \frac{a_1 i^*}{d t} \right) \\
&+ X_2 \left( \frac{a_2 (-S_b i^* + S_d i^*_L + S_e i^*_L)}{C_1} \right) + X_3 \left( \frac{a_3 (-S_b i^* + S_d i^*_L + S_e i^*_L)}{C_2} \right) \\
&+ X_4 \left( \frac{a_4 (S_c v_{C1} - S_b V_{C2})}{L_1} \right) + X_5 \left( \frac{a_5 (S_c v_{C2} - S_b V_{C1})}{L_2} \right).
\end{align*} \]  

(54)
In order to make \( \dot{\nu}_{(a)} < 0 \),
\[
\left( \lambda_1 - \frac{\alpha_1 r_g}{L_g} \right), \quad \lambda_2, \lambda_3, \lambda_4, \lambda_5 < 0.
\] (55)

3.5. Reliability. Reliability evaluation of the proposed converter circuit is presented using Markov approach. Note that hazard rates of power electronic components are only considered in their useful life and other phases such as debugging (which are related to manufacturing errors) and fatigue phases of the components are not considered in the analysis. Figure 14 shows the Markov chain of the mentioned system, which is not employing any fault tolerant scheme.

It has only three states:

State1: proposed topology completely feeds power to the grid and eliminates common-mode current.
State2: proposed topology completely feeds power to the grid but cannot eliminate the common-mode current.
State3: failure.

\( \lambda_{12} \) is expressed as
\[
\lambda_{12} = \lambda_S + \lambda_d + \lambda_D + \lambda_A + \lambda_L + \lambda_C, \tag{56}
\]
\[
\lambda_{23} = \sum_{i=0}^{6} \lambda_S + \sum_{i=3}^{12} \lambda_D + \lambda_A + \lambda_L + 2\lambda_C, \tag{57}
\]
\[
\lambda_{13} = \sum_{i=0}^{6} \lambda_S + \sum_{i=3}^{12} \lambda_D + \lambda_A + \lambda_L + 2\lambda_C. \tag{58}
\]

\( \lambda_S, \lambda_d, \lambda_D, \lambda_A, \lambda_L, \) and \( \lambda_C \) are the failure rates of switches, diodes, inductors, and capacitors, respectively, which are calculated as
\[
\lambda_S = \lambda_k \pi_T \pi_A \pi_Q \pi_E, \tag{59}
\]
\[
\lambda_d = \lambda_k \pi_T \pi_S \pi_C \pi_Q \pi_E, \tag{60}
\]
\[
\lambda_D = \lambda_k \pi_C \pi_Q \pi_E, \tag{61}
\]
\[
\lambda_A = \lambda_k \pi_C \pi_Q \pi_E. \tag{62}
\]

For each component, \( \lambda_k, \pi Q, \) and \( \pi E \) are basic failure rate factor, quality factor, and environment factor of mentioned components, respectively. \( \pi A \) is the application factor of the switch. \( \pi CV \) and \( \pi C \) are capacitance factor and inductor construction factor, respectively. Also, \( \pi S \) is the electrical stress factor of the diode. Mentioned parameters can be easily extracted from [32] regarding the type of the component and its application. \( \pi T \) is the temperature factor for switches and diodes.

In the above two equations, \( T_{js} \) and \( T_{ja} \) are the junction temperatures of the switch and diode, respectively.
\[
T_{js} = T_A + R_{jAs} \times P_{LOSS}, \tag{65}
\]
\[
T_{ja} = T_A + R_{jAd} \times P_{LOSS}, \tag{66}
\]

\( T_A \) is the ambient temperature. \( P_{LOSS} \) and \( P_{LOSS} \) are the losses of the switch and diode, respectively. \( R_{jAs} \) and \( R_{jAd} \) are the junction ambient resistance. According to Figure 1 and mentioned equations, the probability of each state is calculated as
\[
\frac{d}{dt} \begin{bmatrix} P_1(t) \\ P_2(t) \\ P_3(t) \end{bmatrix} = \begin{bmatrix} \lambda_{11} & \lambda_{12} & \lambda_{13} \\ \lambda_{21} & \lambda_{22} & \lambda_{23} \\ \lambda_{31} & \lambda_{32} & \lambda_{33} \end{bmatrix} \begin{bmatrix} P_1(t) \\ P_2(t) \\ P_3(t) \end{bmatrix}, \tag{67}
\]
where \( P_1, P_2, \) and \( P_3 \) are probabilities of states 1, 2, and 3, respectively. \( \lambda \) is the transition matrix, where
\[
\lambda_{11} = -\lambda_{12}, \tag{68}
\]
\[
\lambda_{22} = -\lambda_{23}, \tag{68}
\]
\[
\lambda_{31} = \lambda_{21} = \lambda_{32} = 0. \tag{68}
\]

Assuming that the chain is started from state 1, which is healthy state, the following initial condition occurs and the reliability is calculated as
\[
P(0) = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}. \tag{69}
\]

The reliability is calculated as
\[
R(t) = P_1(t) + P_2(t), \tag{70}
\]
and the mean time to failure (MTTF) is obtained as
\[
MTTF = \int_0^\infty R(t) dt. \tag{71}
\]
Table 2: Circuit parameters and devices used in simulation and experiment.

<table>
<thead>
<tr>
<th>Parameter or devices</th>
<th>Symbol</th>
<th>Value or model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>$V_{DC1}$, $V_{DC2}$</td>
<td>200 V, 30 V</td>
</tr>
<tr>
<td>Input capacitors</td>
<td>$C_{in1}$, $C_{in2}$</td>
<td>300 µF, 330 µF</td>
</tr>
<tr>
<td>Equivalent parasitic capacitor</td>
<td>$C_{pv}$</td>
<td>10 nF, 10 nF</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>$f_{sw}$</td>
<td>10 KHz, 10 KHZ</td>
</tr>
<tr>
<td>Boost inductors</td>
<td>$L_{1}$, $L_{2}$</td>
<td>830 µH, 830 µH</td>
</tr>
<tr>
<td>Diodes</td>
<td>$D_{1}$, ..., $D_{6}$</td>
<td>—, MU560</td>
</tr>
<tr>
<td>Switches</td>
<td>$S_{1}$, ..., $S_{8}$</td>
<td>—, IRF640B</td>
</tr>
</tbody>
</table>

4. Simulation and Experimental Results

To verify the accuracy of the performance of the presented circuit, the circuit is simulated in MATLAB using parameters in Table 2 and then an experimental setup is implemented. The frequency of the proposed topology is 10 KHz, and $L_{1}$ and $L_{2}$ are the output filters. Control parameters are set as $K_{p1}$ = 20 and $K_{i1}$ = 30 and solar modules have been used in simulation.

Simulation results are brought in Figures 15–18. Insolation of PV2 is maintained at 100%, while insolation level of PV1 is at 50% and the temperature of PV1 is increased by 5°C. Figure 15 shows the voltages of $V_{C1}$ and $V_{PV1}$. Output voltage of inverter (Vout), $V_{AN}$, and $V_{BN}$ are shown in Figures 16(a)–16(c), respectively. Figure 17 shows grid voltage and output current of inverter, respectively. According to Figure 18(a), common-mode voltage is constant on 200 V which causes the elimination of the common-mode current, as shown in Figure 18(b).

Figure 19 shows experimental results. The proposed topology is connected to the grid. However, due to some limitations in lab, the circuit is tested by the input voltage of 60 Volt, and, instead of using PV, DC source voltage is employed. Parasitic capacitor between PV and ground is replaced by an external capacitor ($C_{pv}$).

Figure 19(a) shows the grid-connected voltage, current, and the output voltage of inverter ($V_{AB}$). The Total Harmonic Distortion (THD) of the grid-connected voltage is 4.85%. Further, $V_{AN}$, $V_{BN}$, and $2V_{CM}$ are shown in Figure 19(b). According to Figure 18(b), the common-mode voltage is constant, which causes the elimination of the common-mode current, as shown in Figure 19(c).

For displaying waveforms, Gwinstek GDS-2204E oscilloscope and Gwinstek GOP-050 differential probe are applied. As can be observed in Figure 19(b), VCM is 30 V and is constant in all cycles, which results in elimination of $I_{CM}$.

Figure 20(a) shows performance of the transformerless inverter without proposed balancing stage during mismatched condition. As can be seen from this figure, the voltage of PV1 is dropped due to the different environmental condition. As a result, the output voltage of inverter ($V_{AB}$) is decreased and the leakage current is increased to about 5 Amps.

Figure 20(b) illustrates the performance of the proposed topology with proposed balancing stage during mismatched condition. As can be seen from Figure 20(b), the voltage of PV1 is dropped due to the different ambient condition. However, because of proposed balancing stage, inverter output voltage ($V_{AB}$) remains unchanged and the leakage current is eliminated.

Figure 21 shows the efficiency curve of the proposed inverter during mismatch condition for the ranges between 100 watts and 800 watts, where the peak of efficiency is 98.21%.

In order to evaluate the performance of the proposed topology during mismatched condition, a 2.5 KW version of the proposed inverter is simulated. In this simulation, insolation of PV2 is maintained at 100%, while insolation level of PV1 varies from 100% to 10%. The result is compared to the following inverters (which are simulated with the same condition): (1) H-bridge based inverter presented in [26] which has the highest efficiency reported in the literature and (2) inverters presented in [4, 5] which have capability of servicing two separate subarrays under mismatched atmospheric condition. Considering the fact that, among all topologies that are mentioned in this paper, those in [4, 5] are the only topologies that eliminate the leakage current under mismatch condition, the result of this comparison is shown in Figure 22. It can be inferred from this figure that although all of these topologies eliminate the leakage current, the proposed topology is the most effective among the mentioned topologies.
Figure 16: (a) $V_{out}$, (b) $V_{AN}$ and (c) $V_{BN}$.

Figure 17: Grid voltage ($V_{grid}$) and current ($i_g$).

Figure 18: Common-mode simulation results. (a) $V_{CM}$; (b) $I_{CM}$. 
Figure 19: Experimental results of proposed topology. (a) $V_{\text{grid}}$, $I_{\text{grid}}$, and $V_{AB}$. (b) $V_{AN}$, $V_{BN}$, and $2V_{CM}$. (c) $V_{\text{grid}}$, $V_{AB}$, and $I_{CM}$. 
5. Conclusion

Mismatched environmental condition and common-mode current (in transformerless inverters) are the most important challenges faced in the applications of the PV arrays. Many structures have been proposed so far. In this paper, first, the partial shading and ambient temperature effect on the common-mode current are investigated. Then, a circuit was presented which can eliminate common-mode current in PV arrays connected to the grid with transformerless inverters in both normal and mismatched environmental conditions. Results of simulation and practical implementation of the proposed circuit prove the accuracy of the circuit performance.
Data Availability

The data used to support the findings of this study are included within the article.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References


