Hindawi
International Transactions on Electrical Energy Systems
Volume 2022, Article ID 4129314, 15 pages
https://doi.org/10.1155/2022/4129314

Research Article

The Improved Unified Power Quality Conditioner with the Modular Multilevel Converter for Power Quality Improvement

T. M. Thamizh Thentral,[1] **R. Palanisamy**,[1] **S. Usha**,[1] **Pradeep Vishnuram**,[1] **Mohit Bajaj**,[2] **Naveen Kumar Sharma**,[3] **Baseem Khan**,[4] **and Salah Kamel**[5]

[1]*Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Kattankulathur, Tamilnadu 603203, India*
[2]*Department of Electrical Engineering, Graphic Era (Deemed to Be University), Dehradun 248002, India*
[3]*Electrical Engineering Department, I. K. G. Punjab Technical University, Jalandhar, India*
[4]*Department of Electrical Engineering, Hawassa University, Hawassa, Ethiopia*
[5]*Electrical Engineering Department, Faculty of Engineering, Aswan University, Aswan 81542, Egypt*

Correspondence should be addressed to Baseem Khan; baseem.khan04@ieee.org

Received 20 May 2022; Revised 24 August 2022; Accepted 27 August 2022; Published 29 September 2022

Academic Editor: Julio C. Rosas-Caro

Nowadays, researchers focus on the modular multilevel converter (MMC), due to its modularity structure, effective sharing of voltages among the submodule switches, and betterment in the quality of the voltage and current waveforms. First, the conventional unified power quality conditioner is developed with two level voltage source converters connected back-to-back, which are proposed to mitigate both the voltage and current related power quality problems. Later, to improve the performances (voltage sag, swell, current harmonics, etc.) of the conventional method, multilevel inverters are used. In this paper, a modified unified power quality conditioner based on a modular multilevel converter is implemented to mitigate the voltage and current related power quality issues. The design of the MMC is very simple with a modular structure, and it also improves the performance of the system compared to the conventional methods. In this proposed topology, the voltage related compensation is implemented with a seven-level MMC, and the current compensation is achieved with a reduced four switch voltage source inverter. The developed system is simulated in the MATLAB platform, and results are validated by hardware implementation with a FPGA controller. It is observed that the developed system has less % of total harmonic distortion and reduction in voltage sag as per the prescribed IEEE 519–2014 standards and practices.

1. Introduction

Over the years, engineers and researchers have focused their interest on modular multilevel converters (MMCs), which are not only used to reduce the switching devices' voltage rating effectively but also to significantly enhance the quality of the output voltage. The MMC is described as a better solution for high voltage DC transmission systems, variable speed drive systems, and custom power devices. Both shunt and series converters are composed of full-bridge or half-bridge submodules and are distinct from one another. To obtain the $(2\,N + 1)$ level of output voltages, the shunt and series converter is composed of 2 N half-fridge submodules. Due to its modular structure design, the reliability of the MMC-UPQC is increased [1–3].

The modular multilevel inverters are applied to the HVDC system [4]. In various articles, authors have discussed the advantages of the MMC in terms of modularity, scalability, improvement in the performance of the system, boost supply reliability, and economy. The MMC can be used in multiterminal direct current (MTDC) grids for providing interconnections between the main power systems and various renewable energy resources. The various topologies based on the submodules of the MMC are the

half-bridge (HB) inverter, the full-bridge (FB) inverter, the unipolar-voltage full bridge (UFB) inverter, the clamp double (CD) MMC, and 3-level/5-level cross-connected MMCs. Various converter cells are used in the MMC, and functionalities of the MMC are used in the HVDC system. Voltage and current source converter topologies, building blocks, multilevel converters, and hybrid MMCs are discussed for HVDC applications [5].

The MMC based on the unified power quality conditioner, which is used to suppress the circulating current among the six phases, is developed. The averaged control method for the modeling of the converter is developed, and the nearest level modulation method is used for generating the reference current [6]. The seven-level inverter is implemented for low voltage renewable energy applications. In this topology, a switched capacitor with a single voltage source is used. Two switched capacitors with ten reduced switches are adopted to obtain the triple voltage output with reduced voltage stress. The level shifted sinusoidal pulse modulation technique is used to control the switches in the seven-level inverter [7, 8]. A single phase multilevel inverter is implemented with the pulse width modulation method of selective harmonic elimination to achieve the seventy-one-level output [9]. The proposed MMC is designed with an adaptive carrier-based phase disposition pulse width modulation method. This topology uses only one carrier having flexibility with fault-tolerant capability. The MMC system is tested by considering one submodule in fault conditions to obtain the nine-level output [10].

The development of new circuit configurations, the converter model, control schemes, and modulation strategies are discussed in [11]. Authors have mentioned the various merits of the MMC such as the modular structure, transformer-less operation, easy stability in terms of voltage and current, low expense for redundancy and fault-tolerant operation, high availability, utilization of standard components, and excellent quality of output waveforms.

The performance of the MMC is compared with three different modulation techniques. The authors have selected the phase-shifted sinusoidal pulse width modulation, the space vector modulation, and the nearest level modulation to investigate the harmonics produced by these three modulation methods. To control the submodule voltage, the capacitor voltage balancing method is used. A resonant current controller is used to minimize the circulating current [12]. The various voltage and current control methods used for regulating the DC link voltage and reactive power are analysed [13] for unbalanced and distorted network problems. The structure of the MMC, module topologies, and fundamental equations are derived from the MMC; capacitor balancing is also discussed in detail. The current modulators such as current control with constant excitation and current control with excitation proportional to the error are analysed. The performance of the system with voltage and the current modulator for balanced grids, unbalanced grids, and distorted grids are discussed.

Various structures, modeling, working, and applications of the MMC are discussed [14]. The performance of the system is analysed with the p-q theory, the d-q theory, and the proportional resonant controller. The MMC with a single modular structure and superior control characteristics are mentioned [15]. The four-quadrant operation of a single-phase AC to an AC converter is discussed. While discussing the MMC, authors have considered the parameter requirements such as the capacitor energy storage, the semiconductor, gate driver circuits, and their power supplies and converter efficiency. Steady-state and transient operating characteristics of the converter are also explained.

The chopper-based MMC with the carrier phase-shifted PWM (CPSPWM) to obtain the voltage balancing, reduction in harmonic content, and balancing of submodule capacitor voltage is elaborated [16]. The improved SVPWM also analysed with an increase in the output voltage level, voltage stress on the buffer inductor, and influences on voltage balancing of the submodules. Voltage-balancing and the linearization control method for pulse sorting without arm current measurement are used. The voltage balancing algorithm is implemented in each carrier wave period, which reduces the computational intensity; burden and arm current can also be improved by this control method [17].

The MMC includes various features such as high power/high voltage applications, highly redundant, each arm of the converter is made up of a large number of identical submodules with inner storage capability and very high voltage with DC link capacito [18]. A fast-sorting method for voltage balancing is called the tortoise, and the hare sorting method is analysed. The modular multilevel matrix converter (M3C) topology-based single-phase UPQC for medium and high voltage applications is proposed [19]. The type of the M3C considered has four identical multilevel converter arms and associated filtering inductors. The DC circulating current is used to balance the instantaneous active power of each arm and prevent the capacitor voltages from divergence in inter- and intra-arms to achieve voltage balance. The design of the arm inductance and submodule capacitance is studied.

A thirteen-level MMC-based UPQC for power quality mitigations is considered. The control technique used to extract the reference signal is the park transformation method [20]. The control methods of each shunt and series inverter are discussed separately. Series inverter mitigates all kinds of disturbances from the supply side, and the shunt inverter provides the reactive power compensation and harmonic current elimination generated by the nonlinear loads. The multicell UPQC with a discrete-time linear control strategy is introduced [21]. The multilevel three-phase UPQC with single-phase power cells is used to design the topology. The compensation of reactive power and fundamental frequency disturbances are analysed. Single variable linear controllers with the root locus approach are used to choose the controller parameters.

The modeling and control of the sixty-one level MMC for the HVDC system under balanced and unbalanced grid conditions are described [22]. The dynamics of positive, negative, and zero-sequence components are derived from the generalised mathematical model. The dual control with a positive and negative sequence current controller is applied to the MMC. The zero-sequence controller is also considered

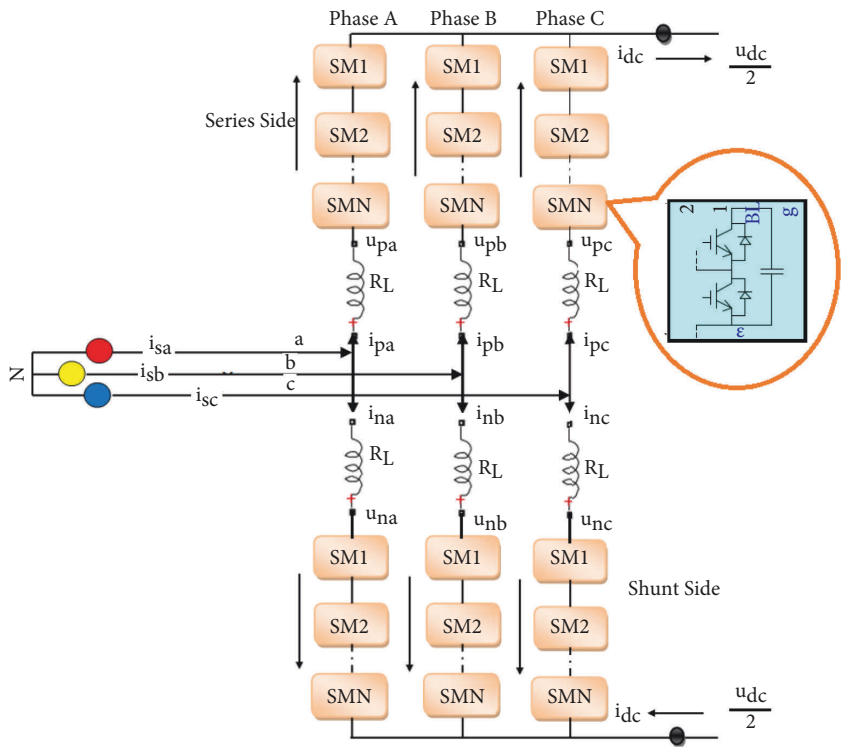


Figure 1: Structure of the MMC.

along with the positive and negative sequence current controllers. The predictive controller-based MMC is discussed for low-frequency switching and a reduced number of capacitors [23]. If the switching frequency is reduced, then the capacitor voltage increases, which leads to an increase in the voltage ripple in the individual submodule. The predictive algorithm is proposed to control the converter by stored energy in the submodule capacitor voltage when it reaches its maximum value and is evenly distributed among all the submodules [24].

The improved steady-state performance of MMCs using modulated model predictive control is discussed. The new modulated technique is discussed to directly capture the optimal modulation references at every sampling period based on the duty cycles of the two fixed voltage levels. Then, the optimal modulation references are fed into the modulation stage to generate gate signals [25].

The proposed work concentrated on seven-level MMC-based UPQC to compensate the variations in supply voltage by using series active power filter (APF) and current harmonics using shunt APF. In the proposed modified modular multilevel converter-based UPQC series part of the UPQC is implemented with a seven-level MMC to regulate the voltage related power quality issues. The shunt part of the modified MMC-based UPQC is implemented with reduced switches to mitigate the current related issues. The two level shunt part of the UPQC is designed with reduced four switches.

Section 2 describes about the design and analysis of modified MMC-based UPQC. Section 3 deals with simulation results and discussion of the modified MMC-based UPQC for power quality enhancement. The hardware implementation and its analysis are explained in section 4. The proposed work is concluded in section 5.

2. Design and Analysis of Modified Modular Multilevel Converter-Based UPQC

The structure for the modular multilevel converter is shown in Figure 1. The MMC consists of three arms in the upper part and three arms in the lower part. Each arm of the MMC can be connected with several submodules. A series connection of submodules makes the arm of the converter to build the output voltage step-wise. Submodules are either half-bridge or full-bridge converters. With n submodules in the arm of the converter, the output voltage has $n+1$ level. The MMC has the advantages of less THD, better voltage sharing among the semiconductors, lesser dv/dt on devices, scalable, and no limitations in DC link voltage, and the mechanical construction is not complex. Due to the redundancy in the structure, failed modules can be easily replaced.

The submodule of the MMC and the four modes of operation of the submodule are given in Figure 2. Figure 2(a) denotes the submodule of the MMC-based UPQC. During this mode of operation, the capacitor is charged. The discharging mode of the capacitor is illustrated in Figure 2(b). In this mode, the capacitor is discharged through switch S_1. It is noted from Figure 2(c) that the arm current is greater than zero, and it is flowing through diode D_2 when the module is not inserted. The direction of the arm current is reversed, and it flows through the switch S_2 as shown in Figure 2(d) by bypassing the submodule. The capacitor is

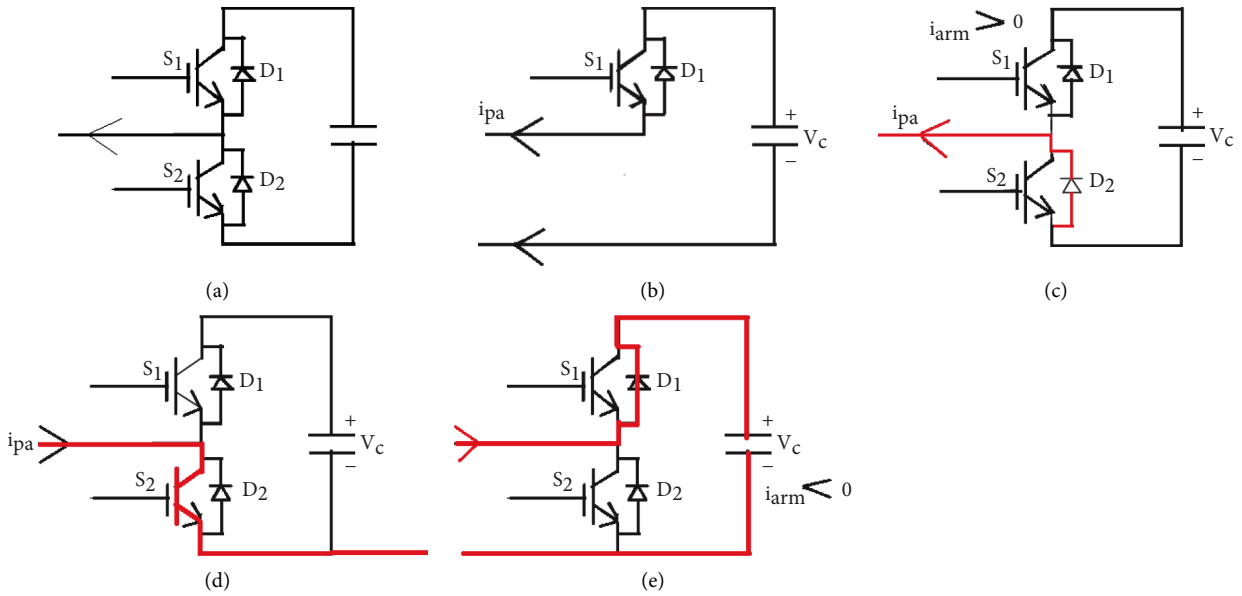


FIGURE 2: Different modes of operation of the MMC. (a)MMC submodule operations. (b)Capacitor in the discharge mode, (c)submodule by the passed mode, (d)submodule by the passed mode, and (e)submodule-inserted capacitor in the charge mode.

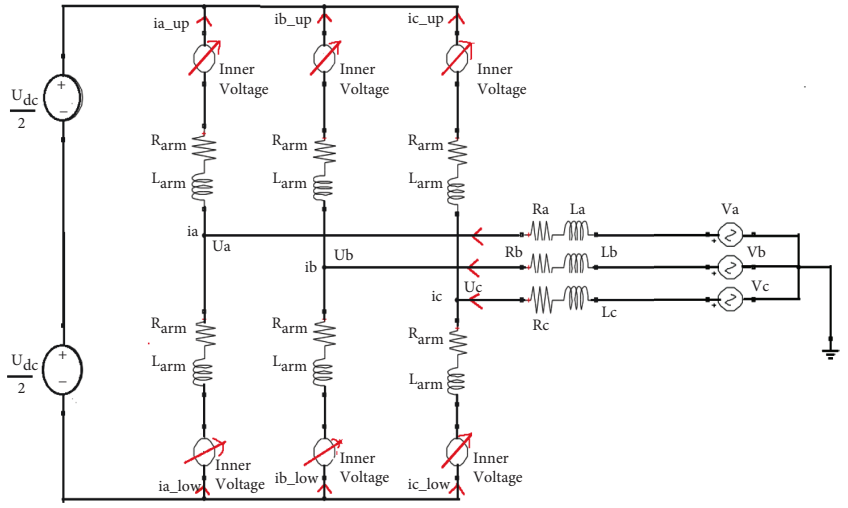


FIGURE 3: Equivalent circuit of the MMC.

charged through diode D1 as shown in Figure 2(e). In this mode of operation, a submodule was inserted, and the arm current is lesser than zero.

The equivalent circuit of the MMC is shown in Figure 3. Each arm of the converter is equivalent to a controlled voltage source and a series inductor. The magnitude of arm voltage is given as

$$\frac{(n_{\text{active}} * U_{\text{dc}})}{N}, \tag{1}$$

where n_{active} is the number of submodules inserted in the arm of the MMC.

U_{dc} is the voltage applied to the MMC.

N is the number of submodules.

The number of submodules inserted in the MMC is

$$N \geq \frac{U_{\text{dc}}}{U_{\text{sm}}}, \tag{2}$$

where U_{sm} is the voltage in the arm with respect to ground

The arm voltage is

$$V_{\text{arm}} = \sum_{i=0}^{n} V_{\text{sm}} + L_{\text{arm}} \frac{\mathrm{d}i_{\text{arm}}}{\mathrm{d}t} + R_{\text{arm}} i_{\text{arm}}. \tag{3}$$

Here, L_{arm} is the inductance in the arm.

R_{arm} is the resistance in the arm.

i_{arm} is the current flowing through the arm.

The output voltage of the MMC is

$$V_k - U_0 = V_{\text{arm}}. \tag{4}$$

Table 1: Arm current and conducting states of the submodule.

Arm current status	Conducting switch	Change in voltage	Device on state	Switch states	Sub-module voltage
$I_{arm} > 0$	S_1 or D_2	$(dV_{arm\ ref}/dt) > 0$, $(dV_{arm\ ref}/dt) < 0$.	S_1 D_2	S_1 = On S_2 = Off	V_c
$I_{arm} < 0$	S_2 or D_1	$(dV_{arm\ ref}/dt) > 0$, $(dV_{arm\ ref}/dt) < 0$.	D_1 S_2	S_1 = Off S_2 = On	0

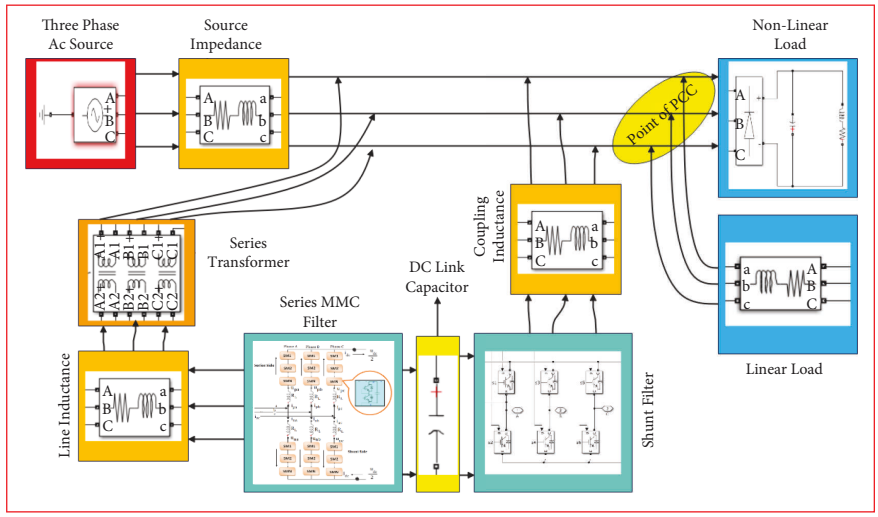


Figure 4: Proposed model of the MMC-based UPQC.

Here, k is a number of arms in the MMC.

V_k is the total arm voltage.

U_0 is the output voltage of the MMC.

The circulating current is

$$i_{cr} = \frac{i_p + i_n}{2}. \tag{5}$$

Here, i_p is the current in the upper arm, and i_n is the current in the lower arm.

The arm current flowing out of the submodule is considered a positive current and inside as negative. The direction of the current decides the switching states of the device. The voltage rating of the submodule decides which module is inserted and which module is not inserted. Table 1 shows the arm current value and conducting devices.

The proposed model of the MMC-based UPQC to enhance power quality is shown in Figure 4. Each arm is connected with 6 numbers of submodules. Submodules are designed with HB converters. Each submodule has a capacitor with an average voltage of U_{dc}. 6 submodules in the arm of the converter output voltage have 7 levels. In the proposed model, the series filter is designed with MMC structure, and the shunt filter is designed with reduced four switches.

In order to obtain the three-phase connection, the third leg of the shunt filter is considered with a split capacitor. The MMC as the series filter is connected in series to the line through the series transformer. The shunt filter is connected to the line in parallel to maintain the harmonic current as sinusoidal and balancing the voltage at the point of common coupling. The coupling inductor is used in between the shunt filter and the line to smoothen the current injected to the line.

The series filter provide the seven level output to provide ripple-free voltage to the capacitor connected in between the shunt and the series filter. Also, we provide the voltage sag compensation and remove the voltage harmonics generated in the system for 3rd and 11th harmonic order. The control signal for both shunt and series filter is obtained by using the hysteresis current controller (HCC).

The compensating signal to regulate the UPQC system is extracted by the decoupled double synchronous reference frame (DDSRF) algorithm. This control method completely eliminates the detection error. A double synchronous reference frame (SRF) is generated to separate both the positive and negative sequence components of the utility voltage. These two components are successfully extracted by developing decoupling networks. The implementation of the DDSRF method has a very fast response; precise operation and robust positive sequence voltage detection can be achieved. The procedure to decouple the sequence current is explained as with equations (6) to (15), The three-phase AC voltage is segmented as positive, negative, and zero sequence elements.

$$\begin{bmatrix} V_{\mathrm{sa}} \\ V_{\mathrm{sb}} \\ V_{\mathrm{sc}} \end{bmatrix} = V_a \begin{bmatrix} \cos(\omega t + \varphi_0) \\ \cos(\omega t + \varphi_0) \\ \cos(\omega t + \varphi_0) \end{bmatrix} + V_b \begin{bmatrix} \cos(\omega t + \varphi_1) \\ \cos\left(\omega t - \frac{2\pi}{3}\varphi_1\right) \\ \cos\left(\omega t - \frac{2\pi}{3}\varphi_1\right) \end{bmatrix} + V_c \begin{bmatrix} \cos(\omega t + \varphi_2) \\ \cos\left(\omega t - \frac{2\pi}{3}\varphi_2\right) \\ \cos\left(\omega t - \frac{2\pi}{3}\varphi_2\right) \end{bmatrix}, \tag{6}$$

where V_{sa}, V_{sb}, V_{sc} are three phase AC voltages; V_a, V_b, and V_c are zero, positive, and negative sequence voltages.

$$V_s = \begin{bmatrix} V_{\mathrm{sa}} \\ V_{\mathrm{sb}} \\ V_{\mathrm{sc}} \end{bmatrix} = \begin{bmatrix} V_{\mathrm{a0}} \\ V_{\mathrm{b0}} \\ V_{\mathrm{c0}} \end{bmatrix} + \begin{bmatrix} V_{\mathrm{a1}} \\ V_{\mathrm{b1}} \\ V_{\mathrm{c1}} \end{bmatrix} + \begin{bmatrix} V_{\mathrm{a2}} \\ V_{\mathrm{b2}} \\ V_{\mathrm{c2}} \end{bmatrix}. \tag{7}$$

The three-phase source current is represented as follows:

$$I_s = \begin{bmatrix} I_{\mathrm{sa}} \\ I_{\mathrm{sb}} \\ I_{\mathrm{sc}} \end{bmatrix} = \begin{bmatrix} I_{\mathrm{a0}} \\ I_{\mathrm{b0}} \\ I_{\mathrm{c0}} \end{bmatrix} + \begin{bmatrix} I_{\mathrm{a1}} \\ I_{\mathrm{b1}} \\ I_{\mathrm{c1}} \end{bmatrix} + \begin{bmatrix} I_{\mathrm{a2}} \\ I_{\mathrm{b2}} \\ I_{\mathrm{c2}} \end{bmatrix}. \tag{8}$$

The apparent power is given as

$$\begin{aligned} S_s &= P_s + \mathrm{j}Q_s \\ &= V_s I_s^*. \end{aligned} \tag{9}$$

The DDSRF theory general equation is given as

$$S_{s012} = S_{l012} + S_{f012}. \tag{10}$$

The 0, 1, 2 represents the zero, positive, and negative sequence powers, and the total power injected to the grid is calculated as

$$\begin{aligned} &S_{l012} = S_{s012} + S_{h012}, \\ &S_{l012} = p_{s012}(t) + Q_{s012}(t) + p_{h012}(t) + Q_{h012}(t). \end{aligned} \tag{11}$$

The term $P\&Q$ represents the active and reactive power of the system.

The input three phase potential and flows are converted to $\alpha\beta 0$ variables by Clark transformation.

$$\begin{aligned} V_{\alpha\beta 0} &= \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} V_s, \\ I_{\alpha\beta 0} &= \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} I_s. \end{aligned} \tag{12}$$

The $\alpha\beta$ parameters are estimated from the above equation

$$\begin{aligned} V_{\alpha\beta} &= \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} V_s, \\ I_{\alpha\beta} &= \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} I_s. \end{aligned} \tag{13}$$

From the positive and negative sequence elements $\alpha\beta$, variables are estimated as follows:

$$\begin{aligned} V_{\alpha\beta} &= V_1 \begin{bmatrix} \cos(\omega t + \varphi_1) \\ \sin(\omega t + \varphi_1) \end{bmatrix} + V_2 \begin{bmatrix} \cos(-\omega t + \varphi_2) \\ \sin(-\omega t + \varphi_2) \end{bmatrix}, \\ V_{\mathrm{dq1}} &= V_{\alpha\beta} \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix}, \\ V_{\mathrm{dq2}} &= V_{\alpha\beta} \begin{bmatrix} -\cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & -\cos(\omega t) \end{bmatrix}, \\ V_{\mathrm{dq1}} &= V_1 \begin{bmatrix} \cos(\varphi_1) \\ \sin(\varphi_1) \end{bmatrix} + V_2 \begin{bmatrix} \cos(\varphi_2) & \sin(\varphi_2) \\ -\sin(\varphi_2) & \cos(\varphi_2) \end{bmatrix} \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix}, \\ V_{\mathrm{dq1}} &= V_1 \begin{bmatrix} \cos(\varphi_1) \\ \sin(\varphi_1) \end{bmatrix} + V_{\mathrm{d2}} \begin{bmatrix} \cos(2\omega t) \\ -\sin(2\omega t) \end{bmatrix} + V_{\mathrm{q2}} \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix}, \\ V_{\mathrm{dq2}} &= V_2 \begin{bmatrix} \cos(\varphi_2) \\ \sin(\varphi_2) \end{bmatrix} - V_{\mathrm{d1}} \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} + V_{\mathrm{q1}} \begin{bmatrix} \sin(2\omega t) \\ -\cos(2\omega t) \end{bmatrix}. \end{aligned} \tag{14}$$

The reference signals from DDSRF theory are estimated for UPFC as given in the following equation:

Table 2: Specifications of the proposed model.

Components	Rating
Source voltage	230 V
Source current	20 A
Split capacitor (MMC)	20 μf
Load (uncontrolled bridge rectifier with RL load and ripple capacitor + linear RL load)	Bridge rectifier $R = 20\,\Omega$, $L = 20$ mH, ipple filter $C = 1000\,\mu$f RLinear RL load $R = 5\,\Omega$, $L = 10$ mH
Output load current	20 A
Switching frequency	10 kHZ

$$P_0 = \frac{3}{2}\left[V_{d1} - V_{q1} - V_{d2}V_{q2}\right]\begin{bmatrix} i_{q2} \\ i_{d2} \\ i_{q1} \\ i_{d1} \end{bmatrix},$$

$$Q_0 = P_2 = \frac{3}{2}\left[V_{d1}V_{q1}V_{d2}V_{q2}\right]\begin{bmatrix} i_{d2} \\ i_{q2} \\ i_{d1} \\ i_{q1} \end{bmatrix}. \quad (15)$$

3. Simulation Results and Discussion

The distribution system is considered with both linear and nonlinear load at the point of common coupling. When the load is varying accordingly, the filter compensates the variations occurred in the load as well as source current and maintains the % THD as per the recommended value. The specifications of the proposed system are given in Table 2.

The % THD on the source current before and after the implementation of UPQC is given in Figures 5(a)–5(c) . Figure 5(a) shows that the % THD of system without UPQC is 16.38%. Figure 5(b) depicts that after the injection of shunt compensating current, the % THD of the system is reduced to 2.87%.

The reduction in percentage THD is achieved, when UPQC is provided the shunt compensation with the yield of reduced 4 switch shunt compensator. When the system is subjected to different loaded conditions, the variations in the % THD are depicted in Figure 5(c). The variations in the % THD are compared with the reference %THD. It is set as 3%. As per the recommendations of IEEE 519, it should be below 5%.

The % THD for different harmonic orders with and without UPQC is given in Table 3. It shows that the fundamental harmonic order at fundamental supply frequency is 100%. Apart from that, the major harmonic order present in the system with the application of linear and nonlinear load is 3, 5, 7, 11, 13, 17, and 19.

The compensating signal from the UOQC is applied to the system at 0 second. Figure 6(a)shows that from 0 to 0.3 seconds with the application of UPQC both the voltage and current are sinusoidal in shape. Between 0.3 and 0.5 seconds, 3rd and 11th order voltage harmonics are generated in the system, which is shown in Figure 6(b). The same manner voltage sag created between 0.4 second and 0.6 second on the system voltage is shown in Figure 6(c). The MMC-based series compensator of the UOQC mitigates the voltage harmonics and compensates the voltage sag which is depicted in Figure 6(d).

During 0.8 second to 1 second, both the linear and nonlinear loads are connected to the proposed system. The change in voltage with application of linear load is shown in Figure 6(e). The voltage at the point of common coupling is maintained constant with the help of a shunt compensator which is given in Figure 6(d). The variations in source current due to different stages of voltage are mentioned in Figure 6(f), and the compensated current is given in Figure 6(g). The per phase waveform of voltage and current subjected to different voltages is given in Figure 6(h).

Figures (7(a)–7(c)) show the various voltage, current, and power waveforms obtained from the MMC-based UPQC system. DC link voltage of the system is shown in Figure 7(a). The waveform shows that based on the variations in the load, the voltage across the capacitor is also controlled by the PI controller to provide the constant voltage at the PCC.

The voltage across the MMC is shown in Figure 7(b). It is a pulsating DC voltage with multiple levels, which is applied to the DC link capacitor to maintain constant voltage across the capacitor. Figure 7(c) depicts the real and reactive power at the source side. With suitable PWM techniques, the series converter maintains the constant DC voltage. The constant voltage to the load is applied through the shunt converter of the UPQC.

The proposed UPQC system improves the active power and compensates the reactive power. The load side active power is shown in Figure 8(a). The active power of the transmission system increased because nonlinear load was absorbed by the series filter in PCC as depicted in Figure 8(b), and the power injected from the shunt filter is denoted in Figure 8(c). The proposed UPQC system reduces the reactive power to enhance the power quality.

4. Hardware Results' Discussion

The hardware implementation of the MMC-based UPQC is shown in Figure 9. An autotransformer is connected at the source side to provide variable input voltage to the system. The performance of the system is analysed with varying linear and nonlinear load. The shunt converter is connected at the load side to provide constant voltage at PCC and to maintain the source current without harmonics. The MMC is connected at the load side through the transformer to provide ripple free voltage at the DC side.

The uncompensated voltage and current at the source side are shown in Figure 10(a). The voltage and current after compensation are given in Figure 10(b). It shows that the

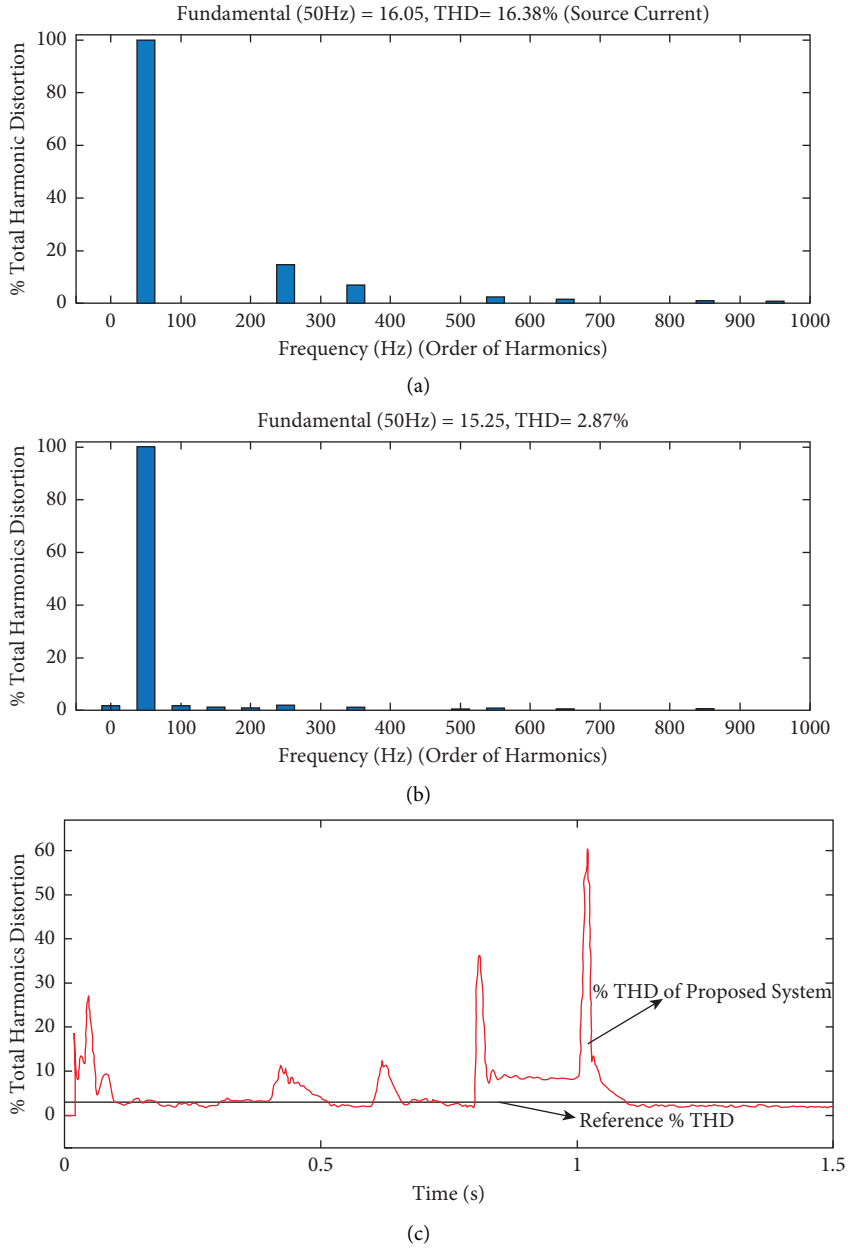
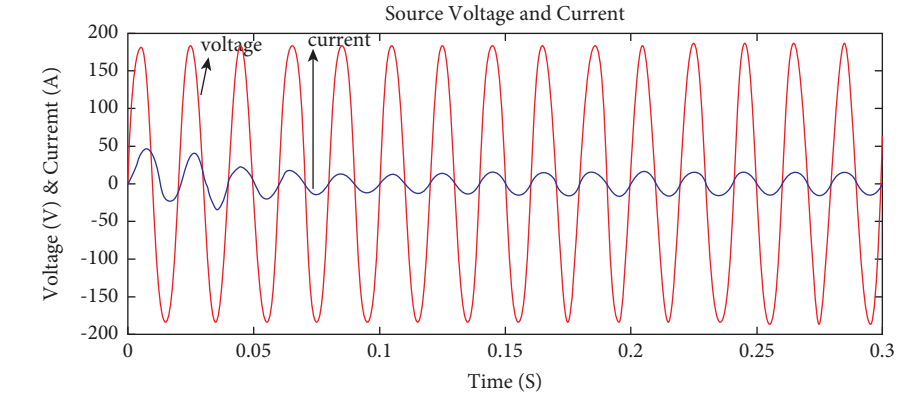


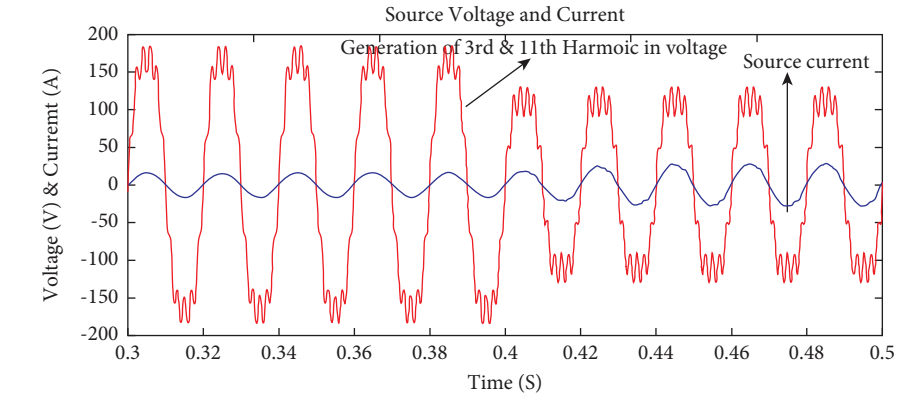
Figure 5: (a) FFT waveform for % THD without MMC-based UPQC, (b)FFT waveform for % THD of with MMC-based UPQC, (c) reference % THD, and % THD of the proposed system.

Table 3: % THD of the proposed system with the harmonic order.

Order of harmonics	% THD only with nonlinear load (without filter)	% THD with linear and nonlinear load	% THD only with nonlinear load (with filter)
1	100	100	100
3	0	2.40	0
5	14.54	3.39	1.83
7	6.86	1.45	0.94
11	2.38	0.58	0.64
13	1.62	0.43	0.44
17	0.61	0.22	0.40
19	0.74	0.16	0.15



(a)



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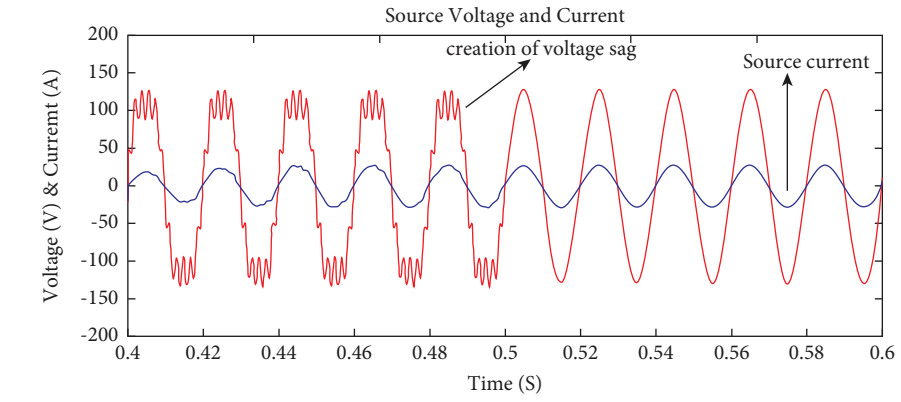

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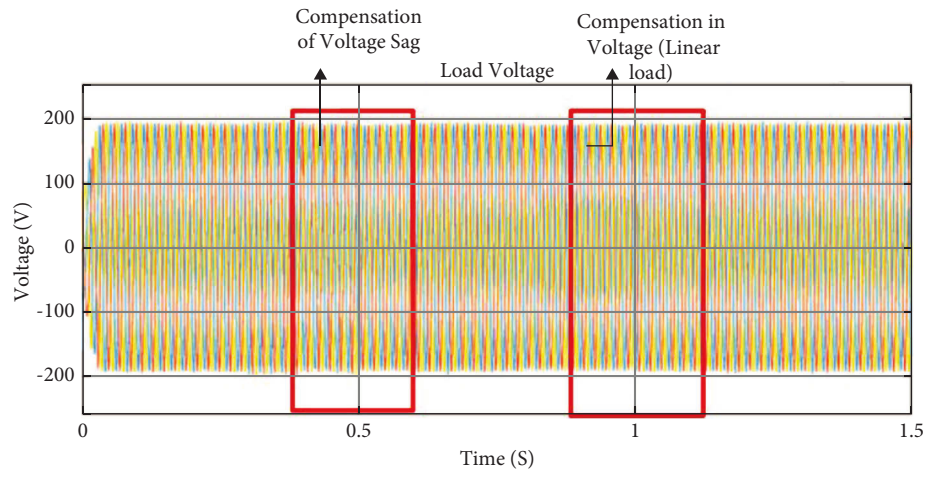
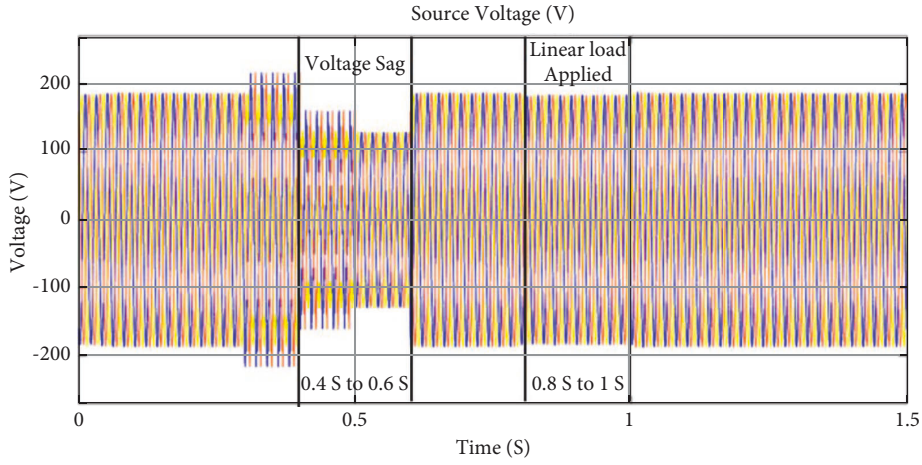


(d)

Figure 6: Continued.



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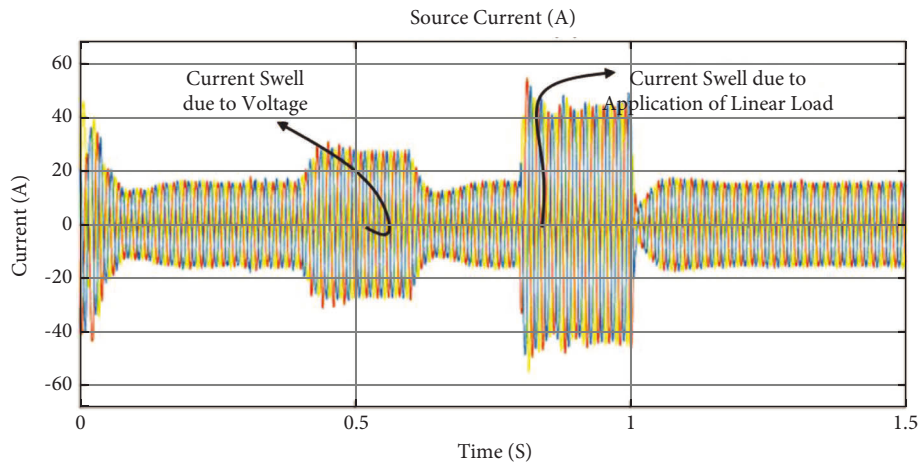
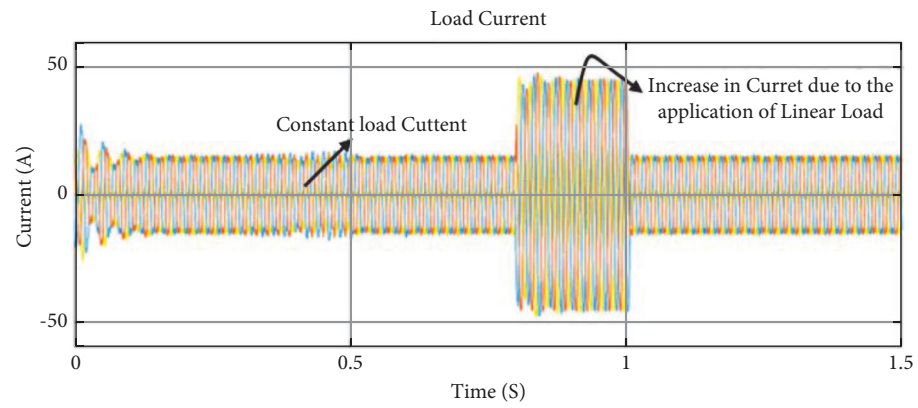
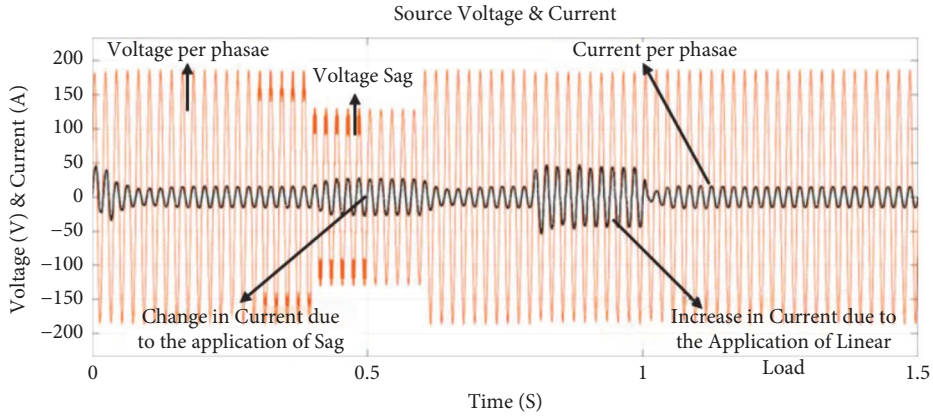


(f)



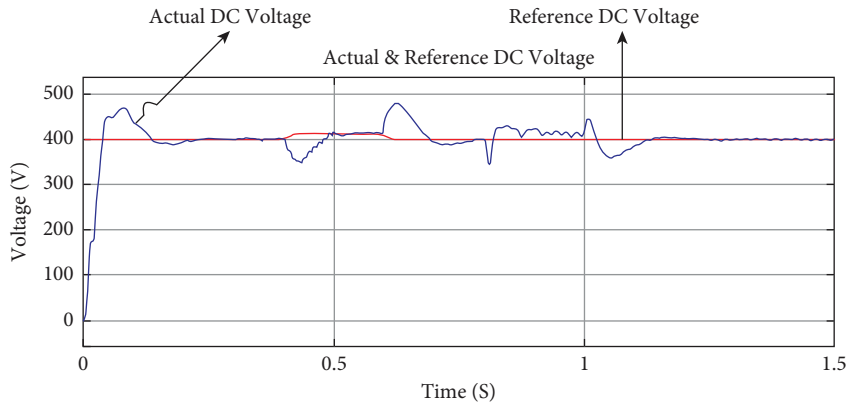
(g)

Figure 6: Continued.

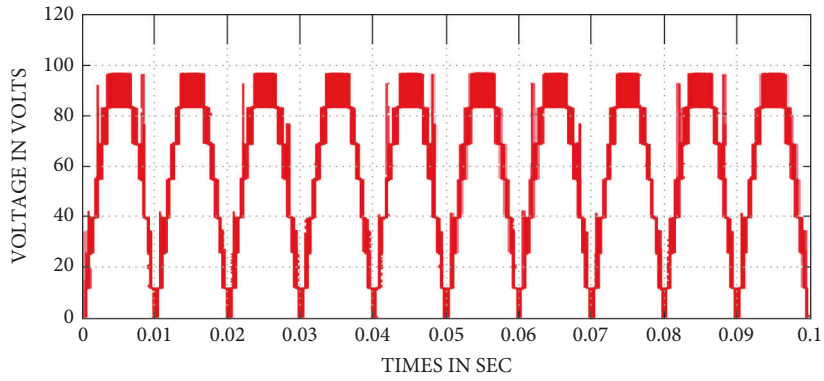


(h)

Figure 6: (a) Source voltage and current, (b)3rd and 11th order voltage harmonics, (c)source voltage with sag, (d)compensated voltage, (e) uncompensated voltage, (f)uncompensated current, (g)compensated current, and (h)per phase source voltage and current.

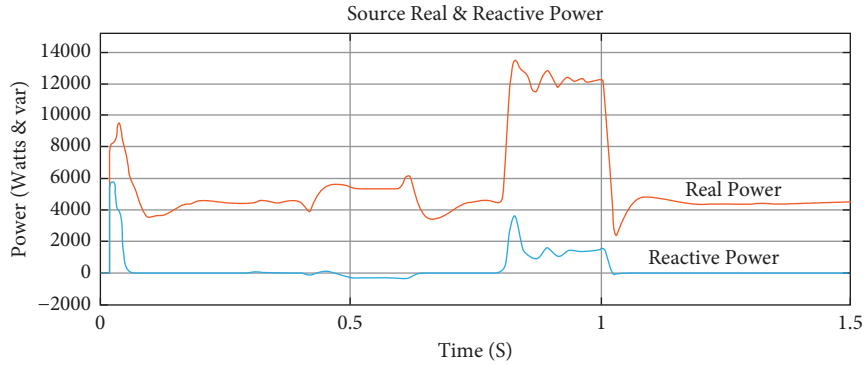


(a)



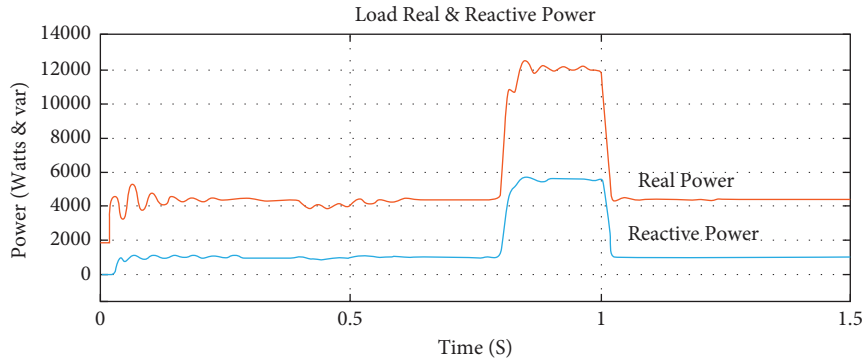
(b)

Figure 7: Continued.



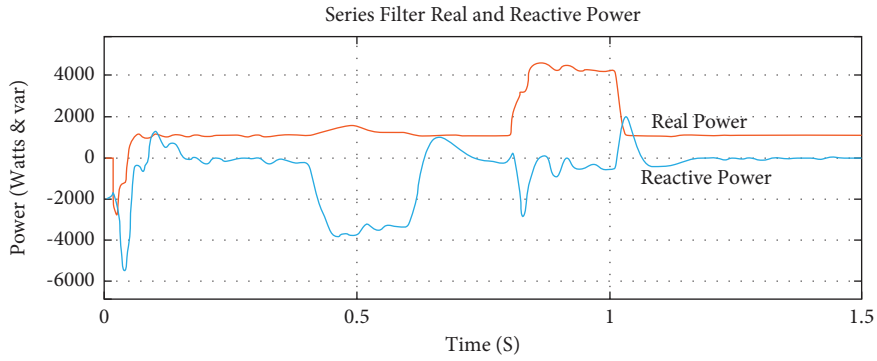
(c)

Figure 7: (a)DC link voltage, (b) MMC output voltage, and (c) source side real and reactive power.



(a)

Figure 8: Continued.



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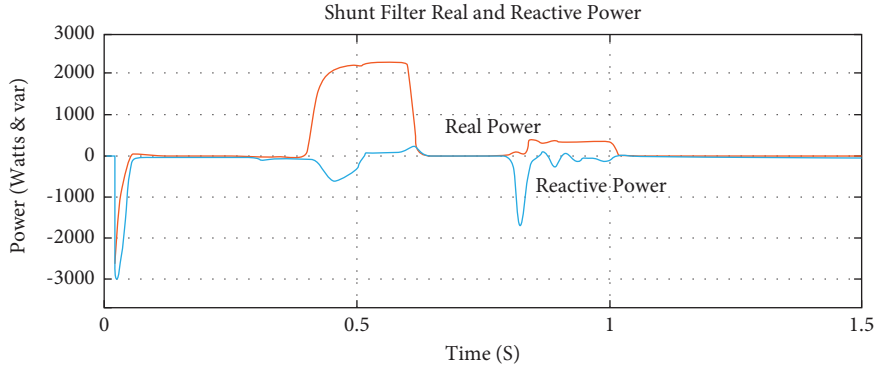


(c)

Figure 8: (a) Load side real and reactive power, (b)power absorbed by the series converter, and (c)injected shunt converter power.

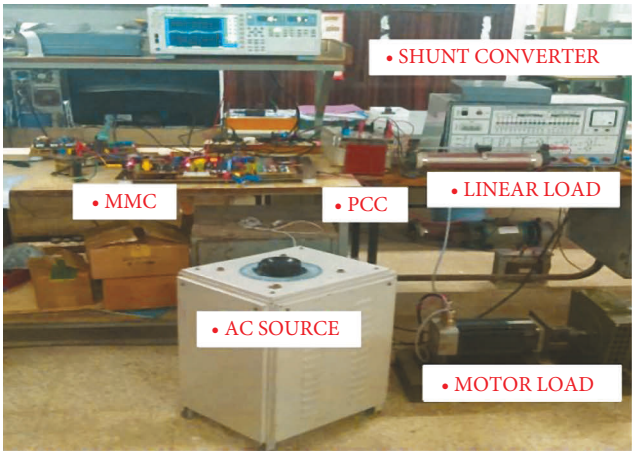
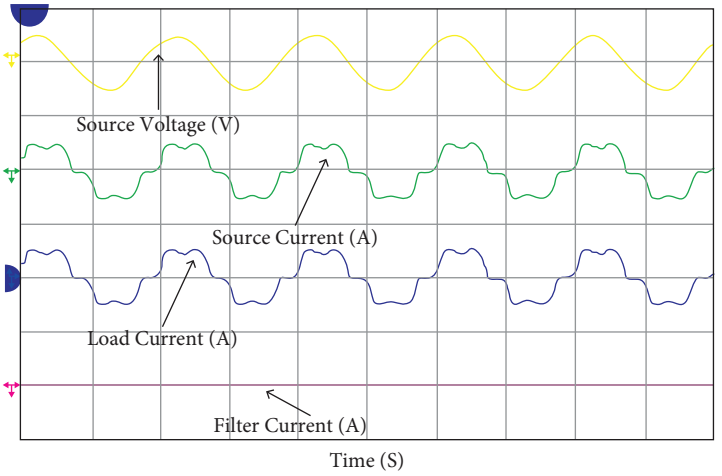
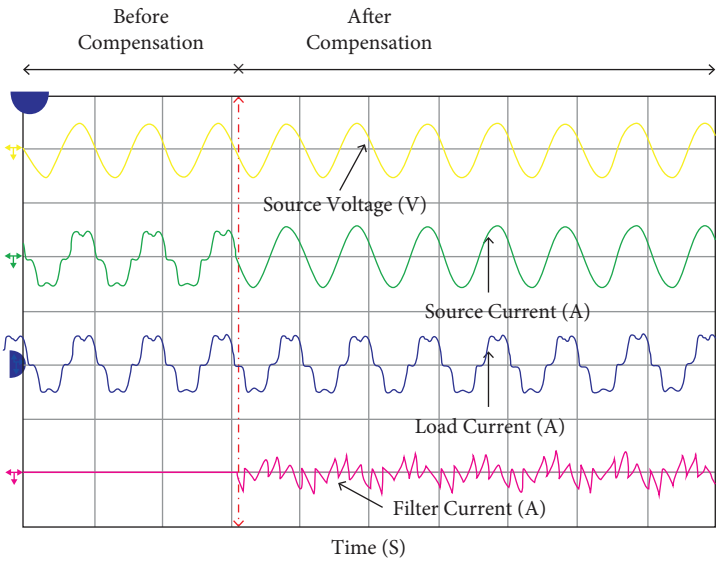


Figure 9: Hardware implementation of the MMC-based UPQC.



(a)



(b)

Figure 10: Continued.

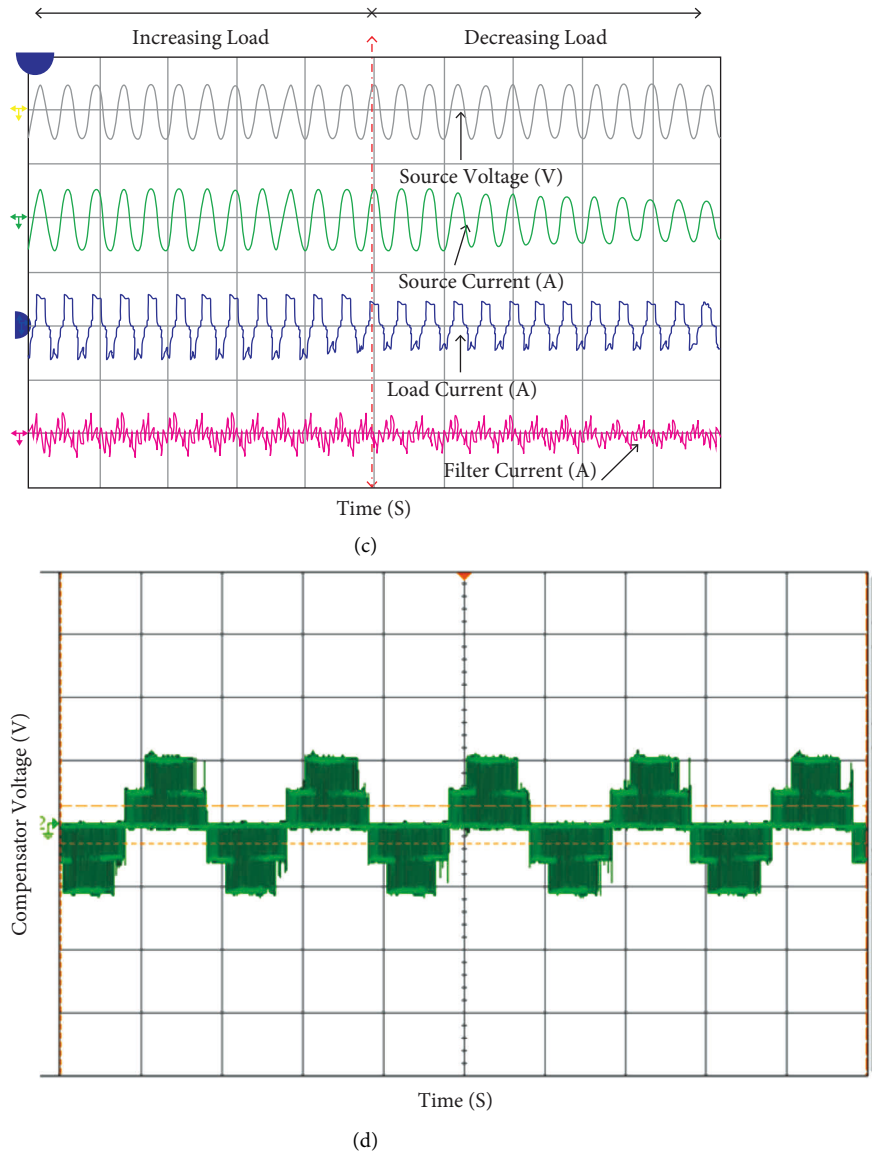


Figure 10: (a)Waveform of voltage and current before compensation, (b)waveform of voltage and current after compensation, (c)waveform of voltage and current for varying load conditions, and (d) waveform of filter voltage.

proposed system compensates the voltage and current harmonics at the source side with the shunt compensator. Figure 10(c) shows the voltage and current for varying load conditions after the compensation is added to the system. The filter voltage is shown in Figure 10(d). Thus, the hardware results obtained for the proposed system shows that the change in input voltage due to some external factor under various load conditions are mitigated effectively.

5. Conclusion

The implementation of modularity in the multilevel inverter with enhanced performance of multilevel voltage has been achieved in this proposed method. A modified unified power quality conditioner based on the modular multilevel converter has been implemented, and the supply voltage and current related power quality issues are also mitigated. From the simulation and hardware results obtained for the MMC-based UPQC system, the system is able to do the following:

(i) Compensate the voltage sag

(ii) Reduce the source current harmonics to 2.87%

(iii) Regulate the voltage at PCC during unbalanced and varying loads

(iv) Reduce the voltage harmonics to 3.89%.

The results concluded that when the multilevel inverter is used for compensation, the performance of the filter is improved in both the steady state and dynamical conditions.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon reasonable request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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