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Research Article

Switched Capacitor Based High Step-Up Multilevel Inverter with Self-Balancing Ability and Low Switching Stress

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In this article, the switched capacitor (SC) based high step-up multilevel inverter is proposed with self-balancing capability. The proposed SC inverter topology is to step up the high output voltage from the very low input voltage without any bulky transformer. This proposed inverter generates single-phase AC voltage with a frequency of 50 Hz from a very low DC input voltage of 50 V with any intermediate DC-DC conversion stage. Hence, the proposed SC inverter is highly suitable for fuel cell, photovoltaic (PV) applications, and shunt active power filter (SAPF). To control the SC inverter, a multicarrier pulse width modulation (PWM) technique is engaged in the inverter. The high step-up voltage level can be achieved by the charging and discharging process of the SC. Furthermore, the stress voltage of the switches does not exceed the applied voltage and the total standing voltage of the inverter is greatly reduced without H-bridges. The comparative analysis of the proposed SC inverter is made for the components, peak inverse voltage (PIV), total standing voltage (TSV), boosting ability, and voltage balancing of capacitors. The main theme of the paper is producing a thirteen-level sinusoidal current with acceptable total harmonic distortion (THD) at different loads, low PIV, TSV, high boosting ability, and self-balancing of capacitors with fewer passive components. The whole system is examined by using MATLAB/Simulink.

1. Introduction

The researcher and industrialist focus on the high-quality output voltage for various applications due to the advancement of power electronics converter topologies and their benefits. For both domestic and industrial applications, there is a rising demand for high-quality and reliable electricity essential especially in aerospace industries. The design of an inverter unit is a very crucial task with a high-quality output voltage for grid-connected applications [1]. Two ways are applied to convert DC-AC conversion. In most of the applications, the intermediate stage is involved for DC-DC conversion and it is followed by DC-AC conversion [2]. But, the problem in the two-stage conversion is the involvement of passive components, dc-link voltage problem, and boosting ability limitations. But, a single-stage converter is failed to enhance the output voltage required levels. In the above conversion process, two or three-level inverters are used and are unable to generate high voltages without adding harmonics, switching losses, and operating limits. Voltage stress, harmonics, capacitor voltage balancing, and total standing voltage are all issues that MLIs face

[3]. A self-balanced SC-based MLI is designed to resolve these issues. MLIs have become very popular in industrial applications because they result in less THD than a conventional two-level inverter. MLIs are used in a wide range of applications, including energy conversion, hybrid cars, and uninterruptible power supplies [4]. In the face of their popularity, classical MLIs have many issues, including the need for more switches, gate driver circuits, capacitor voltage, and balancing for multiple output levels [5]. Researchers and industry leaders are concentrating on new topologies that address the issues with traditional MLIs. They are primarily focused on reducing the number of switches, driver circuits, voltage balancing, and complexity requirements [6]. MLI topologies are designed using a diversity of features, including DC sources, capacitors, semiconductor switches, modularity, output levels, peak inverse voltage (PIV), and total standing voltage (TSV) [7]. MLIs based on switched capacitors have been used for a few years to solve problems with classical inverters. Conferring to the literature [8], five-level SC inverters with self-balancing capacitor voltages have been developed. In [9], discusses a seven-level SC-based inverter topology with boosting capability. In [10], presents a nine-level switched-capacitor-based inverter with quadruple boosting capability. In [11], proposes a self-balanced nine-level SC inverter that uses two DC sources that can be boosted. Four DC sources are used in [12] to create a 13-level inverter, which is quite expensive for DC voltage sources. Furthermore, the authors investigated 13-level inverters by using two DC sources and a few power switches as well in [13]. In [14] complexity and cost of a fifteen-level inverter with four DC sources are debated. Due to H-bridges, the multiport SC-based multilevel inverter has high switching stress and total standing voltage. An SC-based 13-level inverter with a high step-up boost and self-balancing capacity is proposed to resolve the shortcomings of conventional MLIs. In the aero industry, size and weight are a serious concern, which is why designs that realize the same efficiency with smaller volumes are favored in many applications, even with their higher cost. These inverters are suitable for SAPF applications.

1.1. Motivation and Research Questions. According to the study, in many applications, a traditional PWM inverter is used to transform DC to AC voltage. In such operations, a conventional inverter generates the higher harmonic content in the output and also requires a large DC-link voltage. To reduce the harmonic content, a passive filter is applied at the output side and the inverter is subjected to a higher operating frequency. Furthermore, a VSI inverter is developed with an intermediate stage (DC-DC converter) for aerospace applications. From the disputes, the conventional VSI generates more harmonic content and a passive filter is required to compensate for it. On the other hand, intermediate stage-based VSI generates the high output voltage from the low input DC voltage. The problem is more losses due to the additional DC-DC conversion stage. To overcome the inadequacies of the conventional inverter, MLIs topologies are proposed by the researchers. The conventional MLI topologies are producing staircase waveforms and are also able to operate at higher operating frequencies. However, the conventional MLIs are required more DC-link capacitors, several switching devices for constructing higher level MLIs, and voltage balancing issues. For many applications, the quality of the voltage and size, as well as weight, is needed to consider while designing inverter circuits. Therefore, the design of the inverter is a very curial task. In this proposed work, a switched-capacitor-based high step-up inverter is proposed without any DC-DC converter from the very low input voltage. The proposed topology has a simple structure, easy to analyze, and low cost due to a single DC source, a simple gate driver circuit, and no additional DC-DC conversion stage. The proposed inverter is designed to generate single-phase AC voltage with a frequency of 50 Hz from low-power DC sources. The additional feature of the proposed topology has a voltage that gains 5 times of applied voltage. The multicarrier phase disposition PWM control scheme is used to drive the gate pulses of the proposed inverter. The capacitors charge and discharge the voltages by the self-balancing process. The blocking voltage of each switch used in this topology has the same voltage which equals the applied voltage.

2. Multilevel Switched-Capacitor Inverter

A multilevel-based high step-up switched-capacitor inverter is proposed. Figure 1 shows the single-stage conversion which converts DC voltage into AC voltage with any intermediate stage. To generate 230 V, 50 Hz, an SC-based high step-up multilevel inverter is designed for various applications without any intermediate stage. The proposed switched-capacitor inverter circuit consists of five switched cells and each switched cell has one switched capacitor. A thirteen-level SC inverter is formed by connecting the five switched cells in sequence and it is depicted in Figure 2.

The main idea of a switched capacitor is to increase the output voltage from a very low DC input voltage. The input DC voltage comes from low-power sources including batteries, solar panels, and fuel cells.

During charging of the capacitor, the input DC source is connected in parallel to the capacitor through the switches S_{a2} and S_{a5}. The charges in the capacitor will be discharged positively by conducting the switches S_{a2} and S_{a3} i.e., $+V_{dc}$. Similarly, switches S_{a1} and S_{a4} will be conducted to discharge the capacitor negatively, which is equal to $-V_{dc}$. It is observed that the switching pairs (S_{a1},S_{a2}) and (S_{a3}, S_{a4}) are operated complementary for turn-on and turn-off processes. Initially, the five capacitors are completely charged, which equals the input DC voltage by connecting in parallel with the input DC source. To obtain the required staircase output, the charged capacitors will be discharged in series at the desired switching frequency. Table 1 shows the various modes of operation and the states of the capacitor.

3. Carrier-Based PWM Control

In terms of regulating output voltage and reducing harmonic content, PWM control techniques are essential.

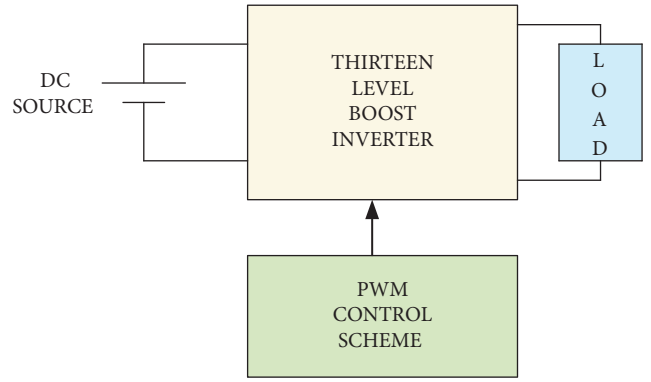

Figure 1: A single-stage voltage source inverter (VSI).

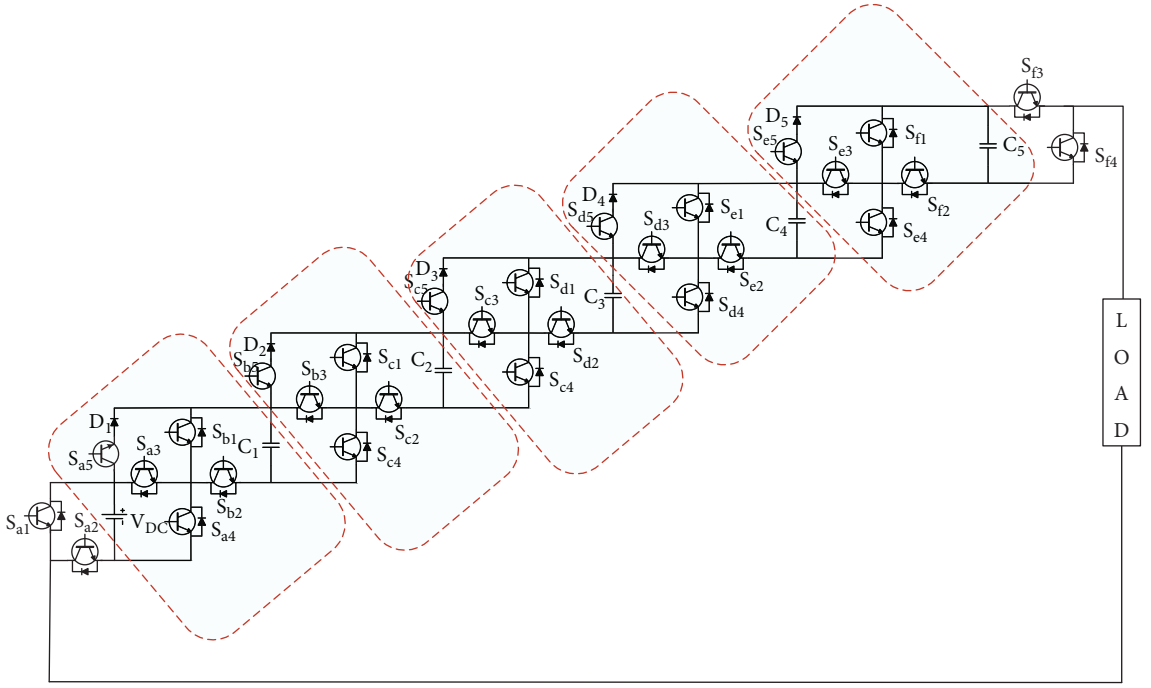

Figure 2: A high step-up SC multilevel inverter.

Furthermore, a harmonic reduction is in line with the switching frequency. In carrier PWM control, the magnitude and frequency of all carriers are equal. (N-1) carriers are decided for the N-level inverter for realizing the N-level inverter output voltage. Among the carrier-based PWM, PD is generating high-quality output voltage [15]. To generate the gate pulses for the high step-up SC inverter, a multi-carrier-dependent Phase Disposition PWM scheme can be used. As shown in Figure 3, the amplitude of high frequency twelve carrier triangular signals (C_1–C_{12}) is compared with the magnitude of the fundamental frequency sinusoidal reference signal. At timing instants, t_1–t_6 produces positive voltage levels, and the timing instants t_{13}–t_{18} produce negative levels of output. For the carrier signal amplitude $A_{Ci} = 1$, reference signal magnitude $A_r = 5.9$, $f_r = 50$ Hz, and $F_s = 20$ KHz, then the timing instants are given as follows:

$$t_i = \frac{\sin^{-1}\left(A_{ci}/A_r\right)}{2\pi f_r}, \tag{1}$$

where, i = time instants 1, 2, 3. . ..

$$t_1 = \frac{\sin^{-1}\left(1/A_r\right)}{2\pi f_r}, \qquad t_2 = \frac{\sin^{-1}\left(2/A_r\right)}{2\pi f_r}, \tag{2}$$

$$t_3 = \frac{\sin^{-1}\left(3/A_r\right)}{2\pi f_r}. \tag{3}$$

The flowchart of the switching strategy is given in Figure 4. Initially, the sinusoidal reference signal (V_r),

Table 1: Modes of operation and state of capacitors.

Voltage level	Conduction of switches	Conduction of diodes	State of capacitors				
			C_1	C_2	C_3	C_4	C_5
$+V_{dc}$	S_{a3}, S_{b2}, S_{c2}, S_{d2}, S_{e2}, S_{f2}, S_{a2}	S_{b4}, S_{c4}, S_{d4}, S_{e4}, S_{f4}	↑	↑	↑	↑	↑
$+2V_{dc}$	S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{d2}, S_{e2}, S_{f2}, S_{a2}	S_{c4}, S_{d4}, S_{e4}, S_{f4}	↓	↑	↑	↑	↑
$+3V_{dc}$	S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{c3},S_{d2}, S_{e2}, S_{f2}, S_{a2}	S_{d4}, S_{e4}, S_{f4}	↓	↓	↑	↑	↑
$+4V_{dc}$	S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{c3},S_{d2}, S_{d3}, S_{e2}, S_{f2}, S_{a2}	S_{e4}, S_{f4}	↓	↓	↓	↑	↑
$+5V_{dc}$	S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{c3},S_{d2}, S_{d3}, S_{e2}, S_{e3}, S_{f2}, S_{a2}	S_{f4}	↓	↓	↓	↓	↑
$+6V_{dc}$	S_{a3}, S_{b2}, S_{b3}, S_{c2}, S_{c3},S_{d2}, S_{d3}, S_{e2}, S_{e3}, S_{f2}, S_{f3}, S_{a2}	—	↓	↓	↓	↓	↓
$-6V_{dc}$	S_{a1}, S_{f4}, S_{f1}, S_{e4}, S_{e1},S_{d4}, S_{d1}, S_{c4}, S_{c1},S_{b4}, S_{b1}, S_{a4}	—	↓	↓	↓	↓	↓
$-5V_{dc}$	S_{a1}, S_{f4}, S_{e4}, S_{e1},S_{d4}, S_{d1}, S_{c4}, S_{c1},S_{b4}, S_{b1}, S_{a4}	S_{f2}	↓	↓	↓	↓	↑
$-4V_{dc}$	S_{a1}, S_{f4}, S_{e4}, S_{d4}, S_{d1}, S_{c4}, S_{c1},S_{b4}, S_{b1}, S_{a4}	S_{f2}, S_{e2},	↓	↓	↓	↑	↑
$-3V_{dc}$	S_{a1}, S_{f4}, S_{e4}, S_{d4}, S_{c4}, S_{c1},S_{b4}, S_{b1}, S_{a4}	S_{f2}, S_{e2}, S_{d2}	↓	↓	↑	↑	↑
$-2V_{dc}$	S_{a1}, S_{f4}, S_{e4}, S_{d4}, S_{c4}, S_{b4}, S_{b1}, S_{a4}	S_{f2}, S_{e2}, S_{d2}, S_{c2}	↓	↑	↑	↑	↑
$-V_{dc}$	S_{a1}, S_{f4}, S_{e4}, S_{d4}, S_{c4}, S_{b4}, S_{a4}	S_{f2}, S_{e2}, S_{d2}, S_{c2}, S_{b2}	↑	↑	↑	↑	↑

↑ = Charging; ↓ = Discharging.

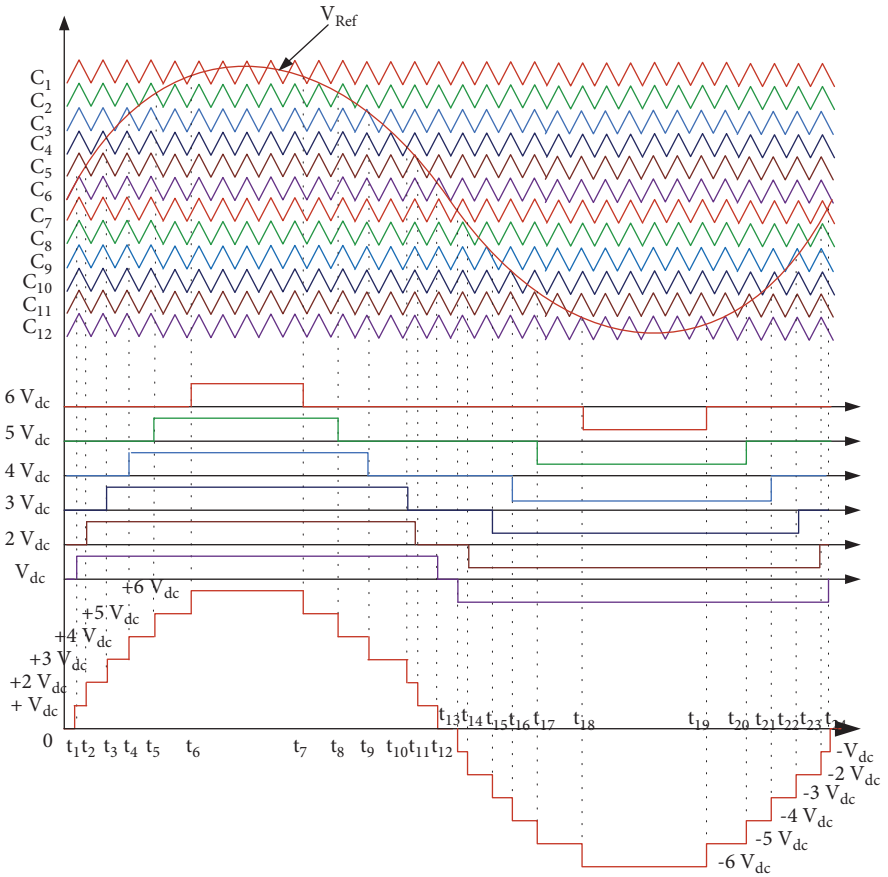

Figure 3: PWM control logic.

positive carrier signal (V_{cp}), and negative carrier signal (V_{cn}) are initialized. At first, the sinusoidal reference signal (V_r) is compared with the positive carrier signal (V_{cp}) i.e., if $V_r > V_{cp}$ is satisfied, then the pulses are given to the switches S_{a1},S_{b1}, S_{c1}, S_{d1}, S_{e1}, and S_{f1}, and if $V_r > V_{cp}$ is not satisfied, then the pulses are given to the switches S_{a2},S_{b2}, S_{c2}, S_{d2}, S_{e2}, and S_{f2}. Similarly, the negative carrier signal (V_{cn}) is compared with a sinusoidal reference signal (V_r), i.e., if $V_r < V_{cn}$ is satisfied, then the pulses are given to S_{a3},S_{b3}, S_{c3}, S_{d3}, S_{e3}, and S_{f3}, and if $V_r < V_{cn}$ is not satisfied, then the pulses are generated to the switches S_{a4},S_{b4}, S_{c4}, S_{d4}, S_{e4}, and S_{f4}. The modulation index (MI) for the proposed high step-up 13-level inverter is represented in the following equation:

$$\mathrm{MI} = \frac{A_r}{6A_C}. \tag{4}$$

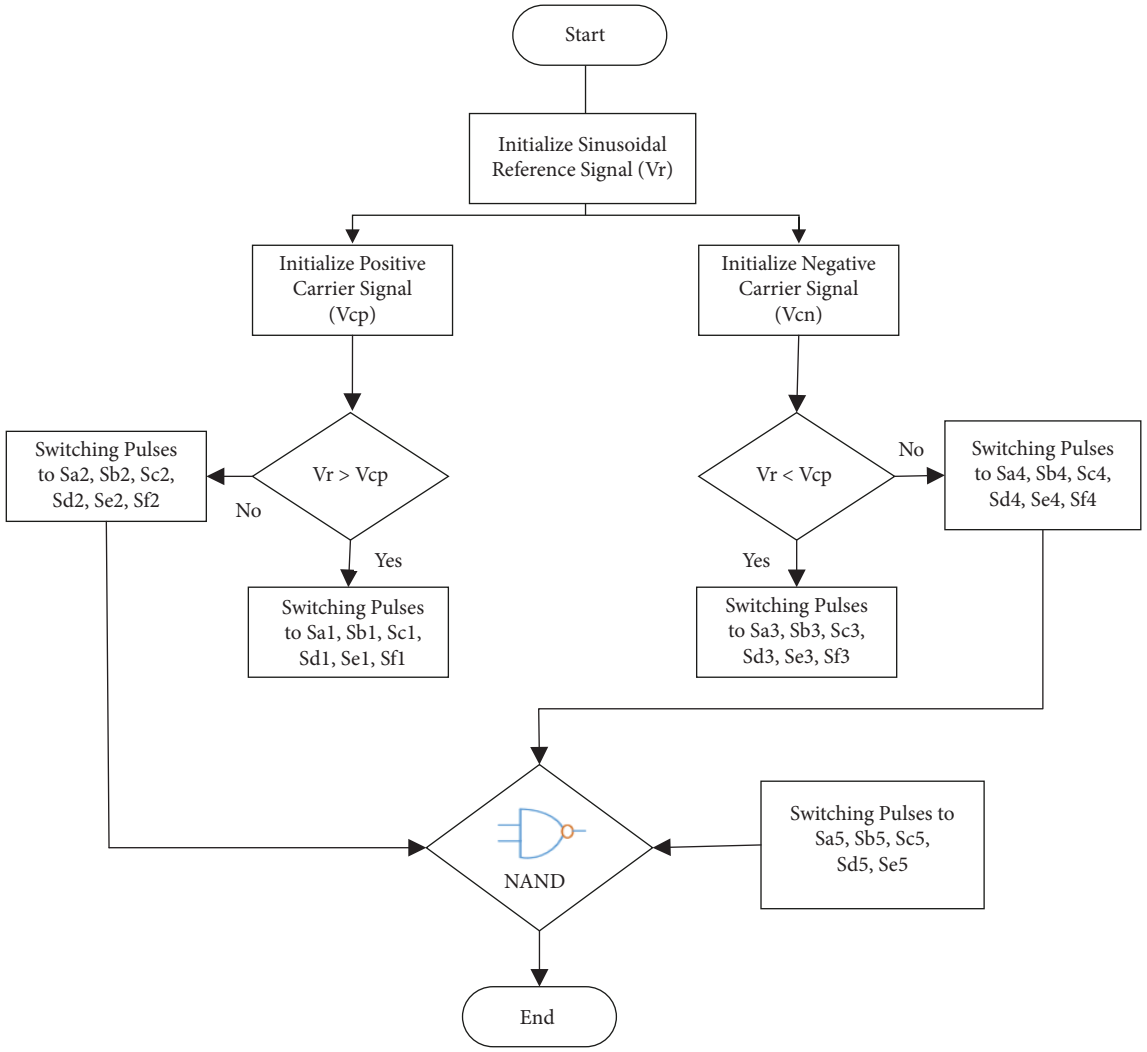

Figure 4: Switching logic implementation.

4. Simulation Results

For the validation of the findings, the proposed high step-up thirteen levels SC inverter is implemented in MATLAB/SIMULINK. They can withstand the voltage of input source V_{DC}. The output voltage of the inverter is approximately five times the applied input voltage, which may derive from the PV, fuel cell and battery, and others. To synthesize 13-level output voltage, the phase disposition PWM technique is implemented by comparing 20 kHz carrier wave and 50 Hz reference frequency. The switches can withstand the voltage during the turn-on and turn-off processes. Moreover, the switching stress across each switch is equal to applied input DC (50V) as shown in Figure 5 and Table 2.

The proposed topology has five capacitors with a value of 1000 μF each. The switched capacitors are charged and discharged using a self-balancing process. When the capacitor is connected in parallel and series with the input DC voltage, as shown in Figure 6, each capacitor charges and discharges a voltage of 50 V.

The capacitor ripple voltage always does not exceed 10% of the capacitor voltage. From Figure 7, the capacitor ripple voltage is 3 V, which is not exceeding 10% of the capacitor voltage of 50 V.

The simulation of the proposed topology is carried out at the input voltage $V_{DC} = 50$ V and the load $R = 0.4$ KΩ. The output voltages at different modulation indices of 0.99, 0.7, and 0.5 with the voltages of 280 V, 230 V, and 150 V respectively, are shown in Figures 8, 9, and 10. Similarly, for the load $R = 25\ \Omega$ and $L = 400$ mH, at modulation index, MI = 0.99, the input voltage V_{DC} is 50 V, frequency is 50 HZ, and the capacitor is 1000 μF, then the proposed inverter produces the thirteen-level output voltage and a current of 280 V and 2.1A respectively, as shown in Figure 11.

The output voltage and level of the inverter are changed by varying the modulation index. For MI = 0.7, the proposed inverter generates the output of eleven levels with the load voltage and current of 230 V and 1.7 A respectively as shown in Figure 11. Similarly, for MI = 0.5, the proposed inverter

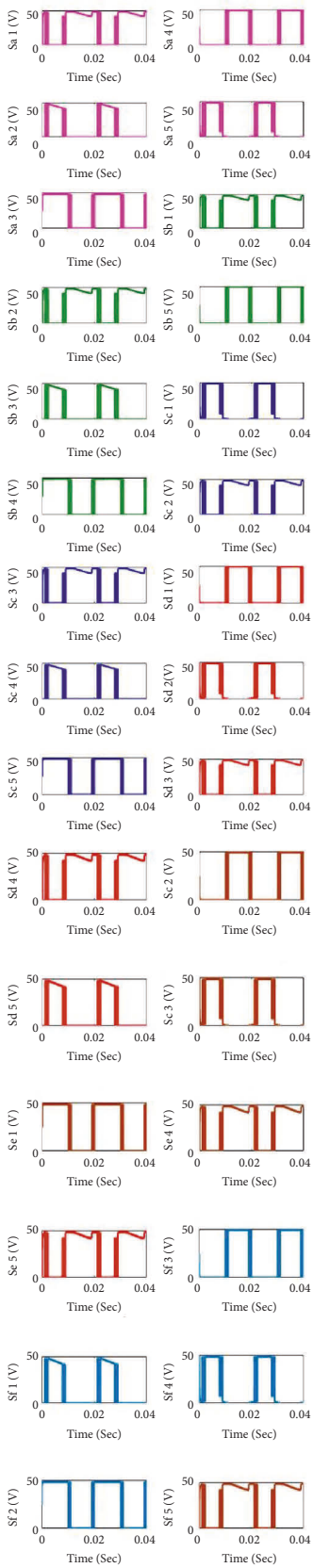

Figure 5: Withstanding voltages of switches.

Table 2: Specifications for the proposed inverter.

Specifications	Value
Number of switched capacitors	5
Output level produced	13
Semiconductor switches required	29
Withstand voltage across the switch	V_{DC}
Switching frequency	20 KHz
Input voltage	50 V
Output voltage	280 V
Output current	2.1 A
Resistor	25 Ω
Inductor	400 mH
Peak inverse voltage (PIV)	$1V_{DC}$
Total standing voltage (TSV)	$29V_{DC}$

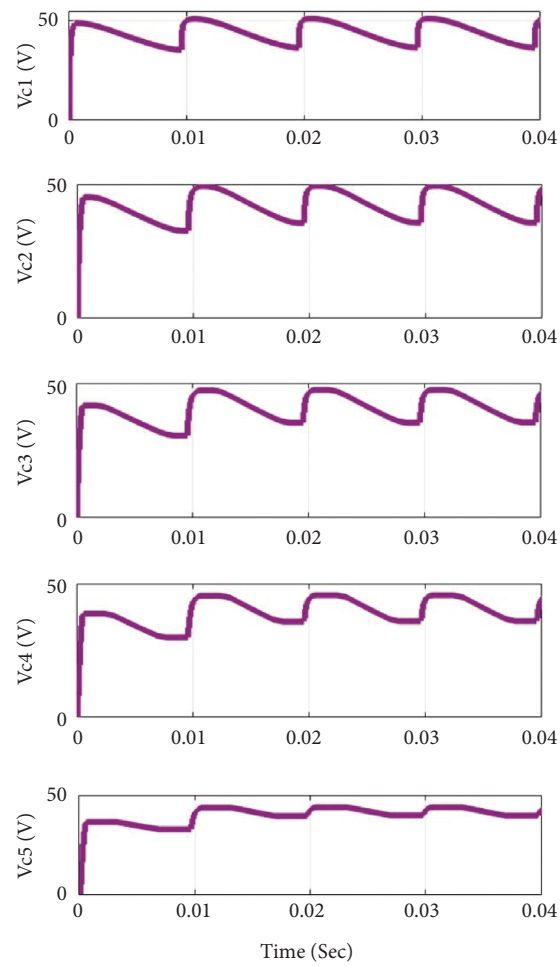

Figure 6: Withstanding voltages of switches.

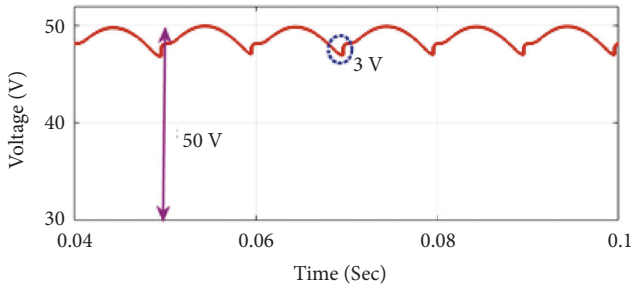

Figure 7: Capacitor ripple voltage.

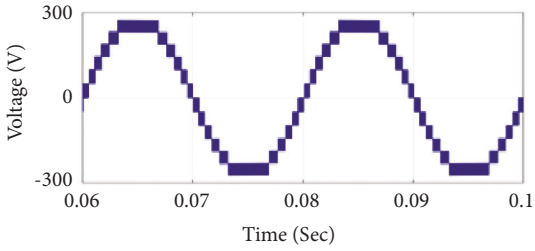

Figure 8: MLI output voltage (MI-0.99).

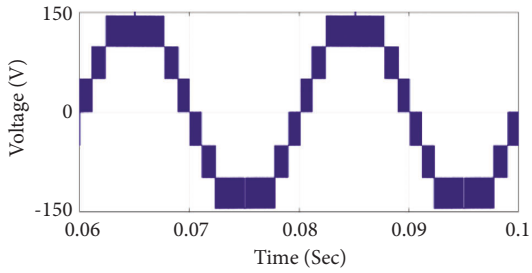

Figure 9: MLI output voltage (MI-0.5).

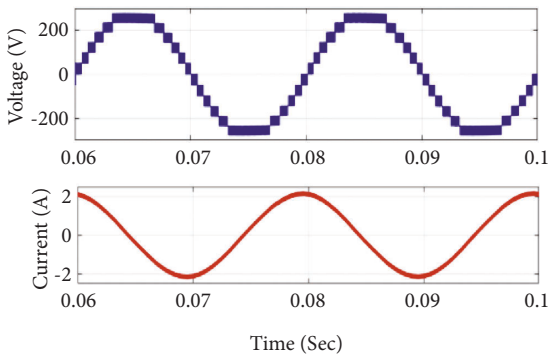

Figure 10: MLI output voltage (MI-0.7).

produces the seven-level output with the voltage and current of 150 V and 1.3 A respectively, as shown in Figure 12.

High harmonic distortions are generated as the modulation index varies, e.g., for MI = 0.99, the THD is 18.07%; for MI = 0.7, the THD is 24.63%; and for MI = 0.5, the THD is 37.77%. Table 3 shows the output of the proposed inverter at various modulation indexes. The generated voltage and

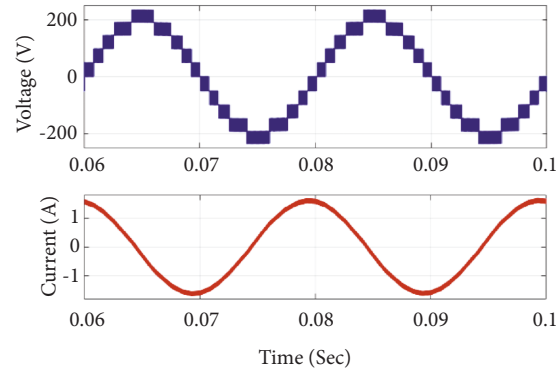

Figure 11: Output voltage and current (MI-0.99) and (MI-0.7).

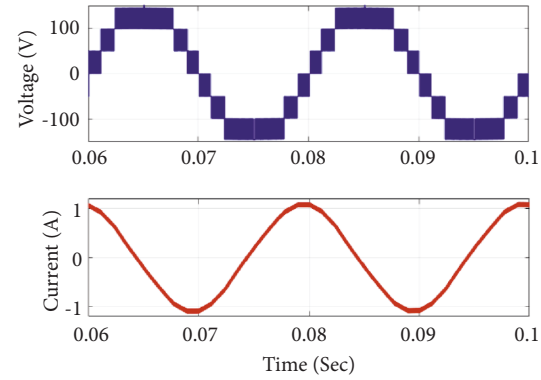

Figure 12: Output voltage and current (MI = 0.5).

current of 275.4 V and 2.1A respectively, at MI = 0.99 with thirteen-level output is obtained with voltage and current THD's of 10.59% and 5.07% respectively. At MI = 0.7, the eleven-level output is obtained with the voltage THD of 14.66% and current THD of 7.65%. The voltage and current THD at MI = 0.5 is 21.58% and 10.94% respectively.

The proposed inverter has voltage and current harmonic distortions of 10.59% and 5.07%, respectively, at MI = 0.99, as shown in Figure 13. Similarly, the proposed inverter's voltage and current harmonic distortion analysis at MI = 0.7 is 14.66% and 7.65%, respectively, and at MI = 0.5 is 21.58% and 10.94% as shown in Figures 14 and 15.

5. Comparative Analysis

To recognize the performance of the proposed inverter, the proposed thirteen-level inverter is compared with the well-known existing topologies in terms of boosting ability, the number of switches, DC sources, and total standing voltages. Table 4, shows that the proposed topology has many advantages in terms of total standing voltage, boosting ability, and peak inverse voltage. Moreover, the proposed inverter has 5 times of boosting ability compared to other topologies.

The NPC- MLI topology [16] have 24 switches, 12 capacitors, and a single DC source that produces the high TSV of 24 V_{DC}. In this topology, the self-balancing

Table 3: Result summary.

Modulation index (MI)	Generated output level	Voltage magnitude (V)	Current magnitude (A)	Voltage THD (%)	Current THD (%)
0.99	13	275.4	2.09	10.59	5.07
0.7	11	201.4	1.57	14.66	7.65
0.5	7	142.8	1.11	21.58	10.94

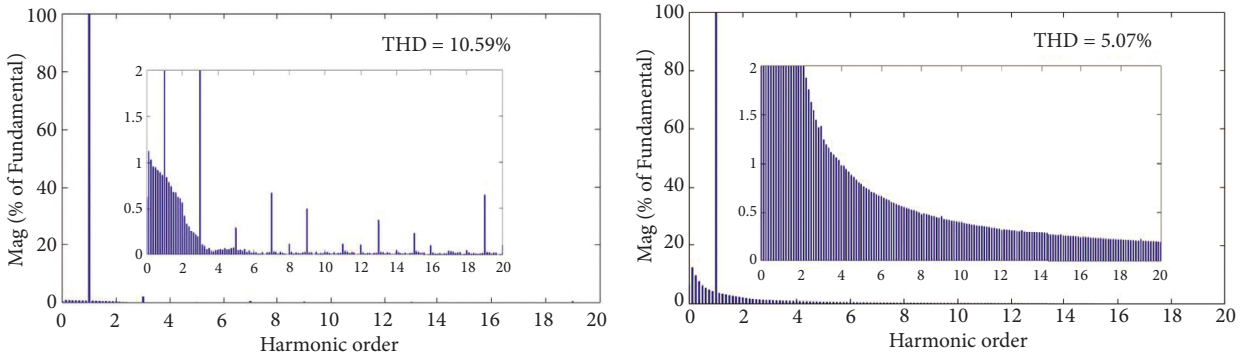

Figure 13: THD analysis (MI-0.99). (a) Voltage THD, (b) current THD.

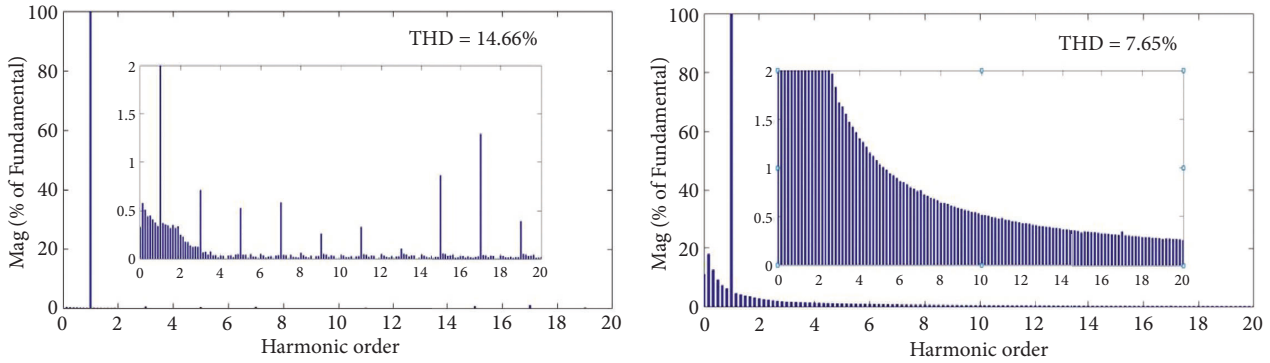

Figure 14: THD analysis (MI-0.7). (a) Voltage THD, (b) current THD.

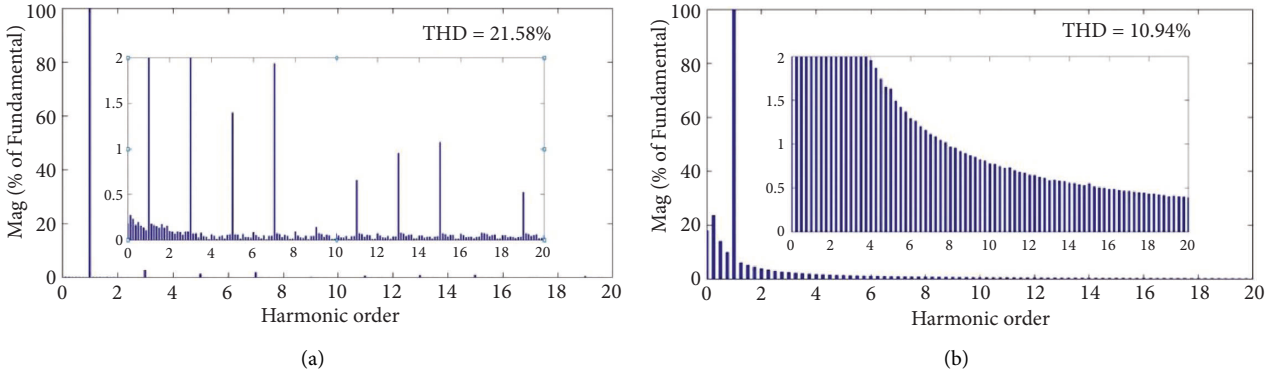

Figure 15: THD analysis (MI-0.7). (a) Voltage THD, (b) current THD.

Table 4: Comparison results between existing topologies and the proposed topology.

MLI	Switches	DC sources	Capacitors	Self-balancing	Boosting ability	H-Bridge circuit	PIV	TSV
[16]	24	1	12	No	No	No	V_{DC}	$24V_{DC}$
[17]	36	6	7	Yes	2 times	Yes	$6V_{DC}$	$36V_{DC}$
[18]	16	6	0	No	2 times	Yes	$6V_{DC}$	$41V_{DC}$
[19]	8	2	0	No	2 times	No	$3V_{DC}$	$32V_{DC}$
[20]	9	3	3	No	2 times	No	$6V_{DC}$	$20V_{DC}$
[21]	18	6	0	No	No	No	$2V_{DC}$	$45V_{DC}$
[22]	10	4	0	No	2 times	No	$5V_{DC}$	$28V_{DC}$
[13]	22	1	6	No	5 times	Yes	$6V_{DC}$	$48V_{DC}$
[14]	12	2	2	Yes	2 times	Yes	$3V_{DC}$	$21V_{DC}$
Proposed thirteen-level boost inverter	29	1	5	Yes	5 times	No	V_{DC}	$29V_{DC}$

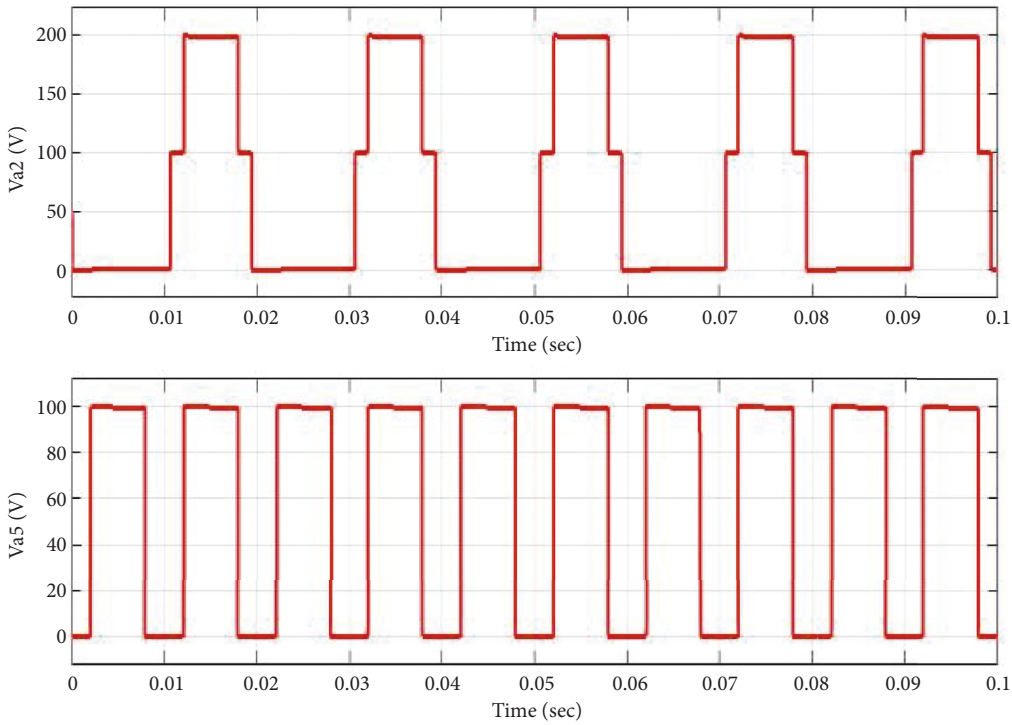

Figure 16: Voltage stress across the switches in [22].

capacity is not possible whereas the topologies [14, 17] and proposed thirteen-level boost inverter have the self-balancing ability.

The topologies [14, 17], and [13] have H- bridge configuration, which results in the high voltage stress on the switches, whereas the proposed thirteen-level boost inverter does not have H- bridge configuration, which results in the low voltage stress on the switches that result in the low PIV and TSV.

The topologies [14, 17] have boosted the ability by 2 times of input voltage, whereas the proposed thirteen level boost inverter topology has to boost the ability by 5 times of input voltage.

The topologies [18], and [21] required 6 DC sources, the topology [22] requires 4 DC sources, the topology [19, 20] needs 3 DC sources, and the topology [14] requires 2 DC sources, whereas the proposed thirteen-level inverter requires only a single DC source, which results in the low cost of the topology.

The number of capacitors required for topologies [16, 17], and [13] are 12, 7, and 6 capacitors respectively. The proposed thirteen-level boost inverter topology requires 5 capacitors and the capacitor voltages are charged and discharged by the self-balancing process. The proposed thirteen-level boost inverter has the advantage of the self-balancing ability, which reduces the need for balancing circuits in the topology.

The voltage across the switches will play a major role in choosing the topology. The voltage stress of the switches in topologies [16,22] is different as shown in Figures 16 and 17, which results in the need for a high amount of filter circuits and high cost of the topology, whereas the proposed

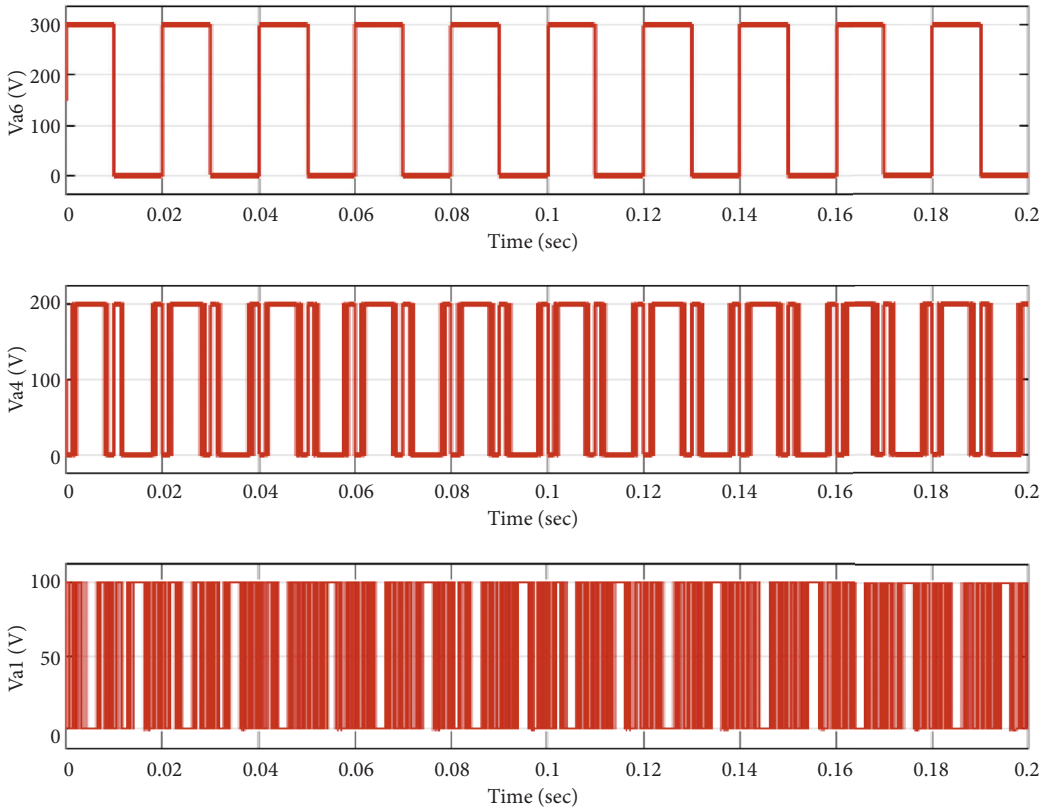

Figure 17: Voltage stress across the switches in [16].

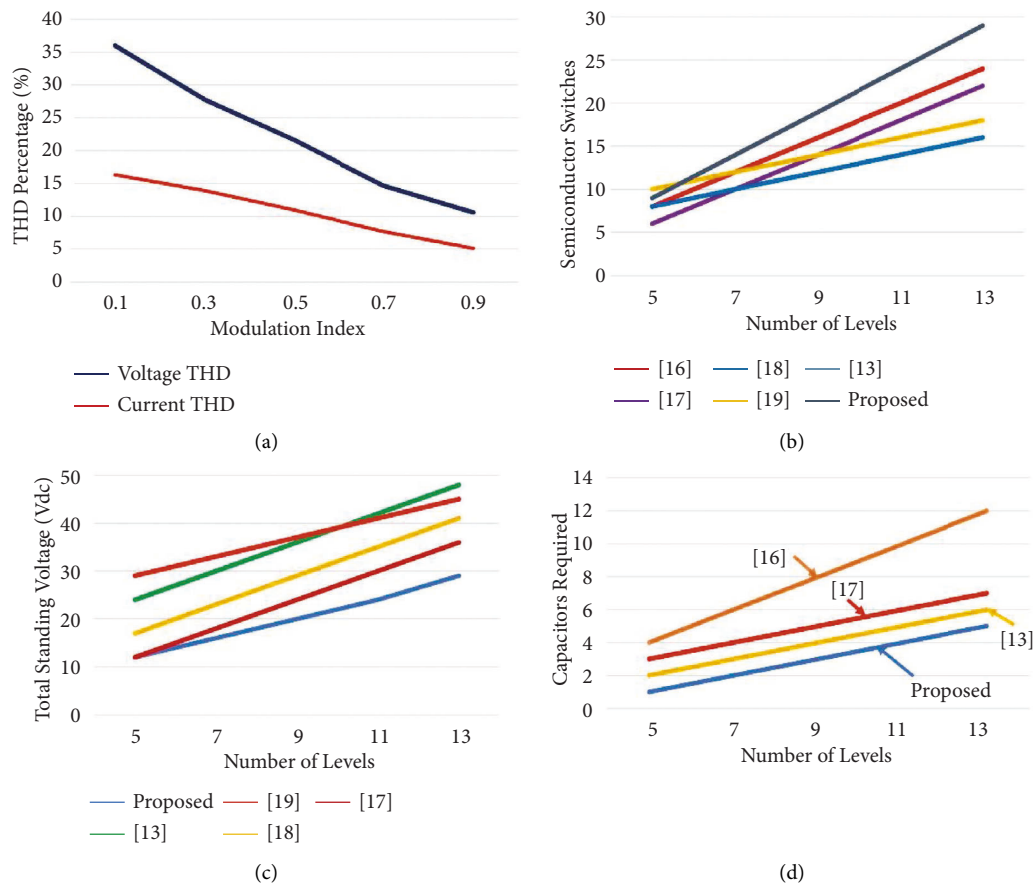

Figure 18: Comparison of expansions. (a) THD percentage, (b) semiconductor switches, (c) total standing voltage, and (d) capacitors required.

topology has the same voltage stress, which is equal to the applied input source as shown in Figure 5. So, the proposed inverter topology does not require any additional filtering circuits, which reduces the cost of the topology.

The topology [13] has switches of 22, which have different voltage stress voltages, which result in a high TSV of $48V_{DC}$. The topologies [18,21] have high TSV of $45V_{DC}$ and $41V_{DC}$ respectively. The 36 switches used in the topology [17] have PIV of $6V_{DC}$ results and a high TSV of $36V_{DC}$. The proposed thirteen-level boost inverter has 29 switches and all switches have equal voltage stress, which is equal to the input DC voltage. Therefore, the proposed thirteen-level boost inverter has low PIV of V_{DC} and low TSV of $29V_{DC}$ compared to the existing topologies.

The voltage and current harmonic distortions at different modulation indices are shown in Figure 18(a). Though the proposed topology has many advantages, the requirement of semiconductor switches is more than the existing topologies for a greater number of levels as shown in Figure 18(b). The proposed inverter topology has low TSV as compared to existing topologies [13, 18, 21], and [17] as shown in Figure 18(c). The usage of capacitors is more in References [16, 17] than the proposed topology, which leads to very expensive as shown in Figure 18(d).

6. Conclusion

The proposed SC inverter topology is set up with high output voltage from the very low input voltage (50 V) with any bulky transformer and is also able to generate different magnitudes. To control the SC inverter, a multicarrier PWM technique was engaged to the inverter. Furthermore, without H-bridges, the switches' stress voltage does not exceed the applied voltage, and the total standing voltage of the inverter is greatly reduced. This proposed inverter generates a single-phase AC output voltage with a frequency of 50 Hz from a very low DC input voltage of 50 V with any intermediate DC-DC conversion stage. As a result, the traditional inverter's size and weight have decreased. As a result, the proposed SC inverter is ideal for various SAPFs. MATLAB/Simulink was used to check the simulation performance.

Data Availability

The data used to support the findings of this study are included within the article. Should further data or information be required, these are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest regarding the publication of this paper.

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Disclosure

The research was performed as a part of the Employment Hawassa University, Ethiopia.

References

[1] A. Bughneda, M. Salem, A. Richelli, D. Ishak, and S. Alatai, "Review of multilevel inverters for PV energy system applications," *Energies*, vol. 14, no. 6, p. 1585, 2021.

[2] M. A. Barrios, V. Cárdenas, J. M. Sandoval, J. M. Guerrero, and J. C. Vasquez, "A cascaded DC-AC-AC grid-tied converter for PV plants with AC-link," *Electronics*, vol. 10, no. 4, p. 409, 2021.

[3] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, and M. A. Memon, "A new multilevel inverter topology with reduce switch count," *IEEE Access*, vol. 7, no. 99, pp. 58584–58594, 2019.

[4] R. A. Rana, S. A. Patel, A. Muthusamy, C. W. Lee, and H. J. Kim, "Review of multilevel voltage source inverter topologies and analysis of harmonics distortions in FC-MLI," *Electronics*, vol. 8, no. 11, p. 1329, 2019.

[5] S. TarmiziTarmizi and M. K. Mat Desa, "Design and Verification of improved cascaded multilevel inverter topology with asymmetric DC sources," *Journal of Power Electronics*, vol. 19, no. 5, pp. 1074–1086, 2019.

[6] S. H. Latifi Majareh, F. Sedaghati, M. Hosseinpour, and S. R. Mousavi-Aghdam, "Design, analysis and implementation of a generalised topology for multilevel inverters with reduced circuit devices," *IET Power Electronics*, vol. 12, no. 14, pp. 3724–3731, 2019.

[7] S. G. Basha, V. Mani, and S. Mopidevi, "Single-phase thirteen-level dual-boost inverter based shunt active power filter control using resonant and fuzzy logic controllers," *CSEE Journal of Power and Energy Systems*, 2020.

[8] W. Peng, Q. Ni, X. Qiu, and Y. Ye, "Seven-level inverter with self-balanced switched-capacitor and its cascaded extension," *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 11889–11896, 2019.

[9] J. Liu, X. Zeng, and J. Zeng, "A seven-level inverter with self-balancing and low-voltage stress," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 685–696, 2020.

[10] M. Fahad, M. Tariq, M. Faizan, A. Ali, and A. Sarwar, "A dual source switched-capacitor multilevel inverter with reduced device count," *Electronics*, vol. 11, no. 1, p. 67, 2021.

[11] M. S. O. Yeganeh, P. Davari, A. Chub, N. Mijatovic, T. Blaabjerg, and F. Blaabjerg, "A Single-phase reduced component count asymmetrical multilevel inverter topology," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 6, pp. 6780–6790, 2021.

[12] E. Samadaei, M. Kaviani, M. Iranian, and E. Pouresmaeil, "The P-type module with virtual DC links to increase levels in multilevel inverters," *Electronics*, vol. 8, no. 12, p. 1460, 2019.

[13] M. Siddique and N. Mekhilef, "A new multilevel inverter topology with reduce switch count," *IEEE Access*, vol. 7, pp. 58584–58594, 2019.

[14] S. R. Raman, Y. C. Fong, Y. Ye, and K. W. Eric Cheng, "Family of multiport switched-capacitor multilevel inverters for high-frequency AC power distribution," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4407–4422, 2019.

[15] M. Muñoz-Ramírez, H. Valderrama-Blavi, M. Rivera, and C. Restrepo, "An approach to natural sampling using a digital sampling technique for spwm multilevel inverter modulation," *Energies*, vol. 12, no. 15, p. 2925, 2019.

[16] E. Gowgani and S. S. Gowgani, "Hybrid multilevel inverter using switched capacitor units," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 9, pp. 4614–4621, 2014.

[17] R. Jain and S. Jain, "Multilevel inverter for interfacing renewable energy sources with low/medium- and high-voltage grids," *IET Renewable Power Generation*, vol. 11, no. 14, pp. 1822–1831, 2017.

[18] H. Samsami, A. Taheri, and R. Samanbakhsh, "New bidirectional multilevel inverter topology with staircase cascading for symmetric and asymmetric structures," *IET Power Electronics*, vol. 10, no. 11, pp. 1315–1323, 2017.

[19] M. Saeedian, J. Adabi, and S. M. Hosseini, "Cascaded multilevel inverter based on symmetric-asymmetric DC sources with reduced number of components," *IET Power Electronics*, vol. 10, no. 12, pp. 1468–1478, 2017.

[20] S. P. Gautam, L. Kumar, and S. Gupta, "Single-phase multilevel inverter topologies with self-voltage balancing capabilities," *IET Power Electronics*, vol. 11, no. 5, pp. 844–855, 2018.

[21] S. Sonti and V. Sonti, "A highly efficient and reliable inverter configuration based cascaded multilevel inverter for PV systems," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 2865–2875, 2017.

[22] Y. Koizumi and H. Koizumi, "A switched-capacitor inverter using series/parallel conversion with inductive load," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 878–887, 2012.